BNL-101843-2014-TECH
AD/RHIC/RD/61;BNL-101843-2013-IR

RHIC Timeline System

C. R. Conkling

August 1994

Collider Accelerator Department
Brookhaven National Laboratory

U.S. Department of Energy
USDOE Office of Science (SC)

DISCLAIMER

AD/RHIC/RD–61

RHIC PROJECT

Brookhaven National Laboratory

RHIC Timeline System

C. R. Conkling Jr. and B. R. Oerter

August 1993

1.0 RHIC EVENT TIMELINE SYSTEM - RHIC EVENT TIMELINE SYSTEM

1.1 INTRODUCTION

A modern accelerator must synchronize the operations of equipment over a wide area. To facilitate this synchronization the RHIC event system will provide a highly reliable, serial timing link to all equipment locations. Timing events and clocks from this link will be used to initiate hardware operations including changes in settings, state changes, and data acquisitions. Events may also be required by software running on systems not directly coupled to accelerator hardware. A standard clock frequency of 10 MHz, as presently used in the AGS and Booster, will provide adequate resolution for timing events in the RHIC acceleration and collision processes.

Two mechanisms are available for generating events on the RHIC timeline, direct hardware inputs and software initiated commands. Optically isolated TTL-level inputs are provided for each of the 256 possible event codes. Event sequences to initiate waveforms, fire kickers, and acquire data during the acceleration cycle, tune measurements, etc. will be implemented by cascading programmable delays. Clocks that are of a general interest, such as the 720 Hz clock generated by the main magnet power supply system will also be available on the RHIC timeline. Externally generated events may also come from other systems sensing unusual conditions with the beam. In the case of a beam abort, the abort event can be used to freeze circular buffers in digitizers for post-mortem analysis.

An example of a software generated event would be one to activate new settings after they have been loaded and verified. Software generated events also provide a convenient way to commission new systems.

The probability exists that several event requests could occur simultaneously, or overlapped in time. Since only one event can be processed at a time, priority resolution will be an integral part of the central encoding facility. Event contention is handled in hardware with highest priority given to input 0 and lowest given to input 255. It should be pointed out, however, that lower priority events being processed will not be interrupted by the arrival of a higher priority event request.

The RHIC central event encoder is to be located in the 4 o'clock equipment house. The event encoder, its input modules, and supporting host computer interface will occupy a single VME chassis. Each input module can support 16 inputs. The event system interconnections are point-to-point, differential TTL. The event encoder modules are isolated from the receiving modules by transformer coupling at the receiving module input. The event encoder initially drives a fanout/repeater module which provides multiple buffered, TTL differential outputs. Some outputs will be used locally within the 4 o'clock house, and others will drive fiber-optic transmitters for transmission to remote RHIC equipment locations.

At each RHIC equipment location, the optical transmission is converted to single-ended

TTL, regenerated (restoring wave shape and timing), and buffered as differential TTL. Again the fanout/repeater is used to produce multiple outputs. General purpose decoder/delay modules may be located in these remote locations, as well as other specially designed modules having direct timeline inputs (e.g. the waveform generator).

The decoder/delay modules accept the RHIC event timeline transmission, decode selected event codes, and generate TTL compatible event pulses following individually programmable delay intervals. The module outputs have 50 ohm drive capability. It is recommended that equipment using these event pulses provide optical isolation to eliminate ground loops.

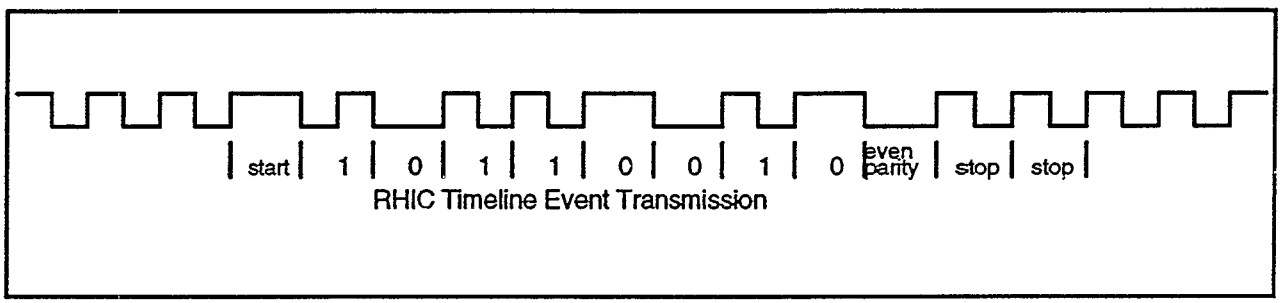

Figure 1.1-2
RHIC Timeline Event Code Transmission

The event codes are transmitted using a serial modified Manchester code (bi-phase-mark). The transmission rate is 10 Mbits/sec, and 1.2 usec are required to transmit an event code. The event timeline contains a continuous bi-phase-mark "ones" transmission during idle periods. A single event code transmission is shown in figure 2.1-2.

There is a 1.3 usec event code transmission delay built into the event encoder system. This assures that very high priority events will be transmitted with minimum time jitter (-0, +100 nsec). If a higher priority event trigger is received while a lower priority event trigger is being delayed, the delay is reset, and the high priority event code will be transmitted before the low priority event code.

RHIC event codes can be permanently assigned without regard to their timeline transmission priority level. The event encoder module contains an event trigger to event code translation table. This table allows an event code trigger priority level to be adjusted relative to other event codes without changing the event code.

1.2 EVENT ENCODER MODULE

The event encoder module is used to transmit RHIC event codes on the RHIC timeline. The encoder module is connected to a 16-position event input module bus. An event input module determines the relative priority of its 16 event trigger inputs. If triggered, the event input module delays 1.3 usec, and attempts to place its highest priority event trigger on the input module bus. However, the event input modules are part of a serial, daisy chain, priority scheme. Thus, if other event input modules have been triggered, the event input module must have position priority (closest to the encoder module) in order to place its event trigger code on the bus.

The event trigger with the least numeric value has the highest priority. The event encoder module converts event trigger inputs into RHIC event codes in a translation table. The event code is input to a serial non-return-to-zero to bi-phase-mark converter for transmission on the RHIC timeline.

When the event encoder module receives an event trigger available from an event input module the following occur:

a. The event trigger code is loaded into a temporary buffer.

b. The event trigger code translated into an event code.

c. The event encoder module sends a BUSY signal to the highest priority event input module, disabling the priority chain while the transmission is in process.

d. The translated event code is input to a serial non-return-to-zero to bi-phase-mark converter. As the code is serialized, a "zero" start bit is added, and code parity (even) is generated. The output of the bi-phase-mark converter is transmitted over the RHIC timeline.

e. The BUSY signal is terminated at the end of the event code parity bit transmission. This allows the event input module priority system time to determine the next event trigger (if any) to be transmitted by the encoder module, and maintain minimum headway.

f. The minimum inter-event code transmission headway is two bit times (two bi-phase-mark "ones").

1.3 EVENT INPUT MODULES - EVENT INPUT MODULES

Each event input module accepts up to 16 event trigger inputs, and determines their relative priority. Event input module channel 0 has the highest priority and channel 15 the lowest priority. Sixteen input modules are required to support 256 events.

Event triggers can originate from two sources:

a. The event input module can have a trigger written to it via the VME bus interface.

b. An event input module external trigger input (front panel LEMO connector or rear VMEbus P2 connector user pins)

It is possible for a low priority trigger to be delayed by higher priority triggers. In this case there may be several transmission increments (1.2 usec/increment) from the trigger until the event is transmitted on the RHIC timeline.

As a result of event trigger priority processing, it is possible to have an extended delay before a low priority event trigger is processed. Therefore, it is possible for a low priority channel to be re-triggered before a previous trigger is processed. In this case the event input module will generate a VMEbus interrupt. The interrupt indicates that one or more event triggers have been lost. During interrupt service, the event host CPU can determine which event trigger channel caused the interrupt.

Inputs are optically isolated. Event triggers must have a minimum pulse width of 1 us and be capable of driving 2 volts into a 50 ohm load.

2.0 DECODER/DELAY MODULE - EVENT DECODE MODULE

2.1 Introduction

The RHIC timeline Decoder/Delay module is a standard VME 6U module. Each module contains eight event output channels with programmable triggers (RHIC timeline event code, previous event output channel, or external), delay times, and delay clock (1 MHz and external).

The module has provision for a direct connection to the RHIC or AGS/Booster event timelines. The timeline events are transmitted short distances, point-to-point, using a twin-axial cable.

The front panel connections are:

a. RHIC timeline twin-axial connector with:

- Transformer coupling for galvanic isolation.
- Watchdog circuit to detect timeline failures.
- Red LED indicating timeline clock failure.
- Green led indicating timeline event data detected.

b. Eight event channels, each having:

- Event output pulse connector
- External event trigger input connector
- External clock input connector
- Green LED indicating each output pulse (pulse stretched for visibility)

Note:

1. All front panel connectors are LEMO NIM-CAMAC coaxial connectors, except the twin-axial RHIC timeline connector.

2. All event channel front panel connections are repeated on the VMEbus P2 connector user pins.

2.2 Decoder/Delay Module Functions - Event Decode Module Functions

a. Synchronizes to the RHIC timeline and detects the RHIC clock and timeline event codes.

1. Detects the RHIC timeline clock, 10 MHz.
2. Detects RHIC timeline event codes.
3. Each RHIC timeline event code is parity and frame checked. If an error is detected, the event is not processed.
4. Derives a 10 MHz clock from the RHIC timeline clock. 5. Derives 1 MHz, 100 KHz, and 10 KHz clocks from the 10 MHz clock. The 1 MHz, 100 KHz, and 10 KHz clocks may be synchronized to the RHIC timeline Master Reset event code.

b. Detects specified event codes on the timeline and:

1. Initiates an event channel programmable delay.

- Event channels may be programmed to respond to one or more timeline event codes.

2. The delay is developed in a 32-bit counter, programmed to count down.

- The minimum delay is 1 count
- The maximum delay is 2^{32} counts, 430 seconds at 10 MHz or 4300 seconds (70 minutes) at 1 MHz

3. The channel delay clock may be selected from:

- The 10 MHz clock derived from the RHIC timeline.
- The 1 MHz clock derived from the RHIC timeline.
- A external clock. If an external clock is used, the maximum frequency is 5 MHz.

4. Event channel trigger options are:

- RHIC timeline event(s)
- The preceding event channel trigger (an external trigger coupled by an external cable in the case of channel 1)
- External trigger

5. At the end of the delay, an event channel output pulse is developed:

- The pulse width is developed in a 16-bit counter, programmed to count down.
- The minimum pulse width is one delay clock period.
  0.1 usec using the internal 10 MHz clock.
  1 usec using the internal 1 MHz clock.
  $1/f_{ext}$ using an external clock.
- The maximum pulse widths are:
  6.5 msec using the internal 10 MHz clock.
  65 msec using the internal 1 MHz clock.
  65535 x $1/f_{ext}$ using an external clock
- The pulse is capable of driving a 50 ohm load.
- Minimum pulse level at the event decode module output is +3V.
- Event channel outputs may be wire 'ORed'.
- Event channel outputs are available on the front panel and rear VMEbus P2 user pins.

All triggers, timeline event, VMEbus, or external are synchronized to the selected clock (external or internal) before the delay count down begins.

Each decoder/delay module is completely self supporting, once initialized. There can be more than one decoder/delay module in a VME chassis. The module driver software should be capable of supporting a full chassis of 16 decoder/delay modules. Each module requires three tables to be initialized for proper operation. Once the tables are initialized, no further support is required for normal operation. The tables are;

a. Event code, 256-bytes.
b. 8-channel counter control and delay registers, 128-bytes.
c. 8-channel clock and trigger control registers, 4-bytes.