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Direct Digital Phase Shift by DDS rf Source

A. Pei

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Collider Accelerator Department
Brookhaven National Laboratory

U.S. Department of Energy

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AD/RHIC/RD-57

RHIC PROJECT

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As direct digital synthesizers with built-in high resolution digital phase modulator become available (eg. Stanford Telecom's STEL-75 series), it is possible to use the digital phase modulation function to replace conventional analog phase shifters in many accelerator applications. A block diagram of such a synthesizer is shown in Fig.1(a).

Other than saving additional parts which results in lower cost and higher reliability, there is a wide array of additional benefits.

Wideband phase-shifting is automatically guaranteed by the digital phase-modulator. In the analog scheme, unless a signal is originally obtained in quadrature format, precise 90 degree phase shifter has to be used. Although much progress have been made in recent years, it is still difficult to have very wide band operation of 90 degree phase splitting.

Another critical component, the analog multiplier, is also eliminated. The amplitude dependence and overall linearity of an analog phase shifter depend on the precision of both the 90 degree phase splitting and the multiplication operation. Thus with the digital PM inside DDS, the overall linearity is improved and there is no parasitic amplitude modulation.

The analog trig function generator chips used in the analog phase shifters are both precise and easy to use. However, its range is limited to $\pm 2\pi$, resulting in a phase shifter that has the same range limitation. In the digital direct synthesizers, we can let the PM register overflow. By 2π modulus of the PM register, the correct phase value will be automatically reached by the phase table warping. This extended range is particularly useful in locking two rf systems of different frequencies in which division of phase by rational

numbers is involved.

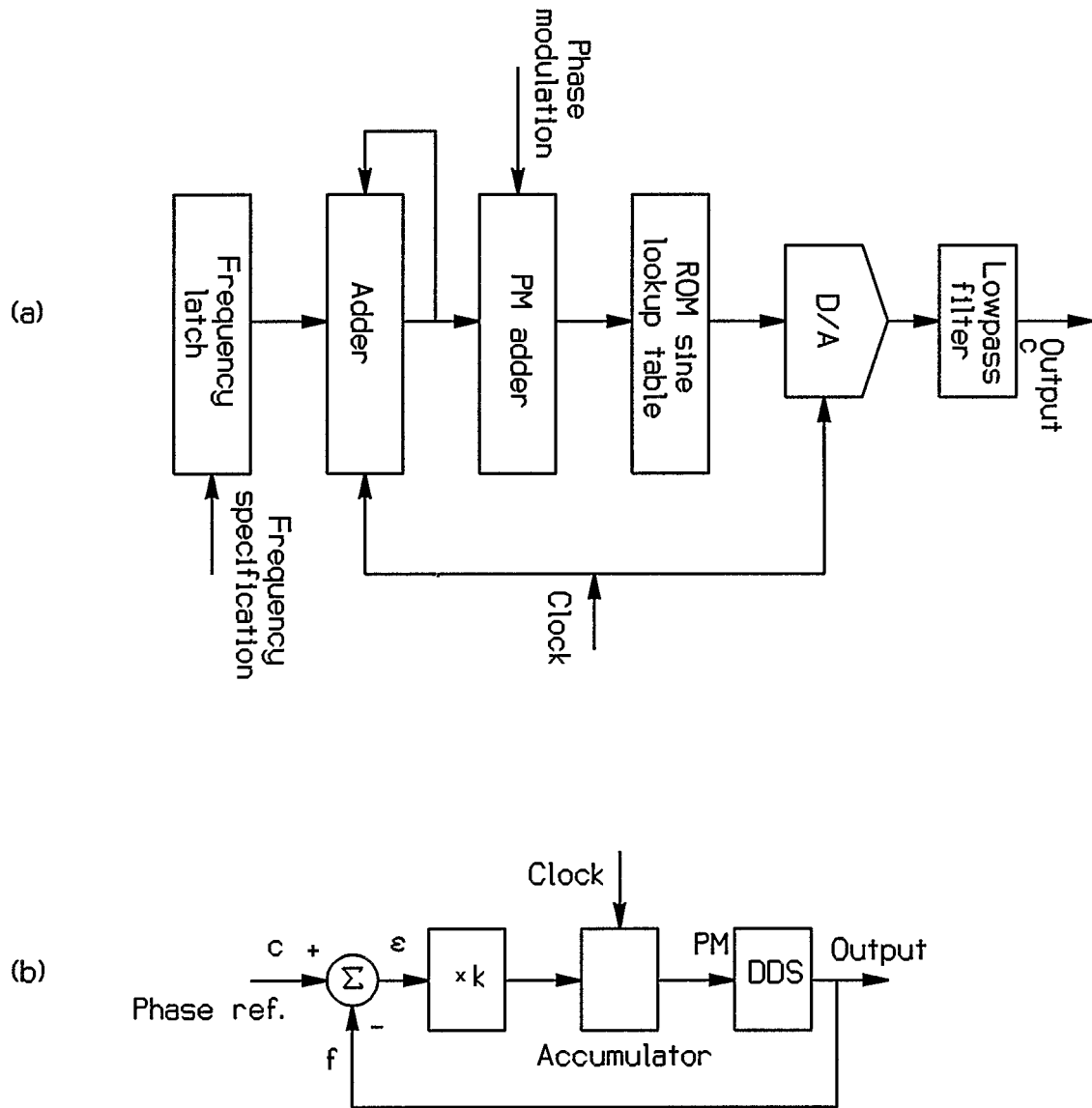


Fig.1 (a): Block diagram of DDS with phase modulation. (b): A simple phase lock feedback system employing such a DDS.

The following is a discussion of design approaches using built-in DDS PM.

The DDS PM register is interfaced with an accumulator. The accumulator's function is much the same as an integrator in analog circuits. It can be described by the following difference equation:

$$y(n)=y(n-1)+x(n-1) \quad (1)$$

where x and y are input and output of the accumulator respectively. The quantity n and $n-1$ corresponds to the n th and $(n-1)$ th clock of the system.

For a simple system that requires phase lock to a reference, we have the block diagram of Fig.1(b).

If the control is steady, the error signal will have the following homogeneous difference equation:

$$\varepsilon(n+1)+(k+1)\varepsilon(n)=0 \quad (2)$$

whose solution is:

$$\varepsilon(n)=C (1-k)^n \quad (3)$$

where C is an initial condition dependent constant.

We thus see that for $0 < k < 2$ the system is stable. The convergence or the speed of the loop can be adjusted by varying the coefficient k .

A general loop can include cavities and other delay elements. The difference

equations will be more complicated and the z transform and bilinear transformation from s to z domain are useful tools.