BNL-101838-2014-TECH

AD/RHIC/RD/56;BNL-101838-2013-IR

Numerically Controlled Phase Locked Loop Using Direct Digital Synthesizer

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April 1993

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USDOE Office of Science (SC)

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A direct digital synthesizer is a highly stable digitally controlled frequency generator that outputs high spectrum purity rf signals. Because of the all digital design, it is immune to various environmental disturbances (mechanical, temperature, etc) that plague conventional LC based VCOs. As a result, a PLL based on DDS can achieve high spectrum purity with very narrow tracking bandwidth.

A basic concept of phase locked loop based on the direct digital synthesizer is shown in Fig.1. The output of the direct digital synthesizer is compared to the reference signal phase r by a phase comparator. The phase error signal ϵ is scaled by a multiplier k and is added to an accumulator. The accumulator in turn directly controls the frequency f_i of the DDS. With the frequency controlled by a phase error signal, the DDS output phase is the time integration of the input of the DDS. The whole system is updated by a clock with a period of ΔT. The PLL is essentially a discrete digital system with a sampling period of ΔT.

To evaluate the performance of such a system, let's denote n as the nth system clock and write down the difference equations.

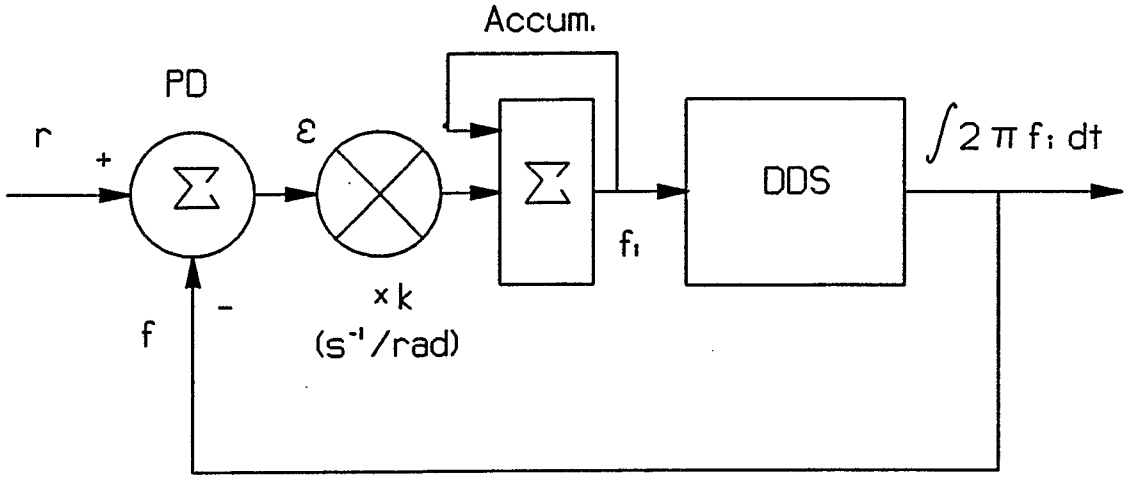

Fig.1 Block diagram of a digital PLL with DDS

The DDS output, which is also the feedback signal f, is the integration of the error signal and can be written as:

$$f(n)=f(n-1)+2\pi\Delta T\, A(n-1) \tag{1}$$

The accumulator is characterized by the following difference equation:

$$A(n)=A(n-1)+k\varepsilon(n-1) \tag{2}$$

The error signal at the nth clock is simply

$$\begin{aligned}\varepsilon(n)&=r(n)-f(n)\\&=r(n)-[f(n-1)+2\pi\Delta T\, A(n-1)]\\&=r(n)-r(n-1)+\varepsilon(n-1)-2\pi\ \Delta T\ [A(n-2)+k\varepsilon(n-2)]\end{aligned} \tag{3}$$

Using Eq.1 again, we get:

$$\varepsilon(n)-2\varepsilon(n-1)+(1+2\pi\Delta T\,k)\varepsilon(n-2)=r(n)-2r(n-1)+r(n-2) \tag{4}$$

This is a second order difference equation in ϵ and the homogeneous solution is:

$$\varepsilon(n)=C_1(x_1)^n+C_2(x_2)^n \tag{5}$$

where

$$x=1\pm i\sqrt{2\pi\Delta T\,k} \tag{6}$$

and C_1 C_2 are initial condition dependent constants. From the above we see that the system is unstable. The absolute value of x is always greater than unity for $k>0$ and the error has exponential growth.

This is not surprising as both the accumulator and the DDS act as ideal integrator and the error signal is phase shifted 180 degrees by the double integration. The negative feedback thus turns into positive feedback!

To achieve stability we let part of the error signals control the DDS directly as shown in Fig.2. The difference equation of the DDS output is now:

$$f(n)=f(n-1)+2\pi\Delta T\,[A(n-1)+\alpha\varepsilon(n-1)] \tag{7}$$

where α is the fraction of error that directly controls the frequency of the DDS.

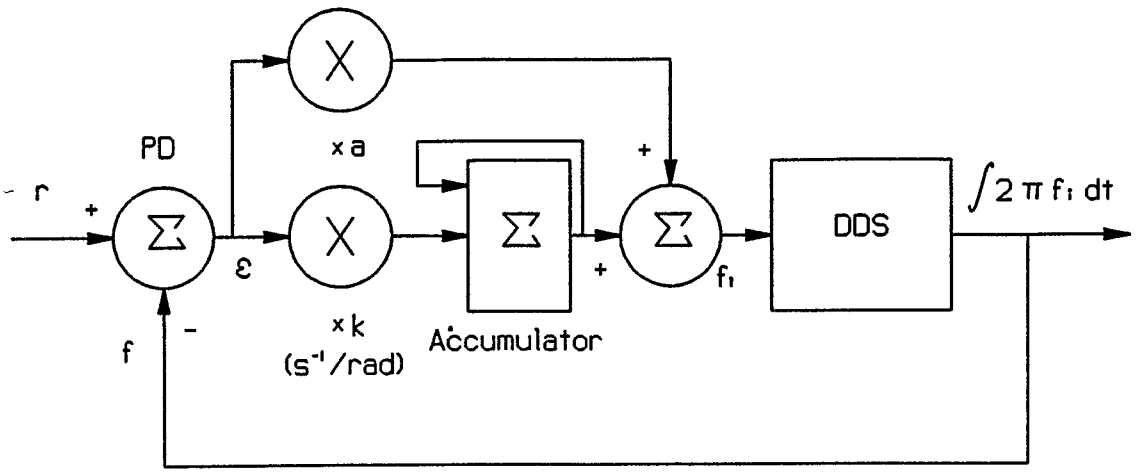

Fig.2 A digital PLL block diagram with improved stability.

The error difference equation is now:

$$\varepsilon(n)-2(1-\pi\Delta T\alpha)\varepsilon(n-1)+[1+2\pi\Delta T(k-\alpha)]\varepsilon(n-2)=r(n)-2r(n-1)+r(n-2) \tag{8}$$

The solution to the characteristic equation is:

$$x=(1-\pi\Delta T\alpha)\pm\sqrt{(\pi\Delta T\alpha)^2-2\pi\Delta Tk} \tag{9}$$

For real solutions it can be shown that for

$$0<\alpha<\frac{1}{\pi\Delta T}, \quad k<\frac{\pi\Delta T\alpha^2}{2} \tag{10}$$

this system is stable. If we include complex solutions the condition of stability can be further relaxed.

An important consideration for accelerator application is the PLL's tracking

capability with a changing reference. To examine this we rewrite the RHS of Eq.8 as follows:

$$r(n)-2r(n-1)+r(n-2)=[r(n)-r(n-1)]-[r(n-1)-r(n-2)] \tag{11}$$

Divide Eq.8. by ΔT the RHS now becomes:

$$\frac{\Delta\phi_r(n)}{\Delta T}-\frac{\Delta\phi_r(n-1)}{\Delta T}=\omega_r(n)-\omega_r(n-1) \tag{12}$$

where ϕ_r and ω_r are the phase and frequency of the reference signal.

This is an important result. It shows that if the reference rf frequency ramps linearly, Eq.12 will be a constant and thus the RHS of Eq.8 will be constant. It is not difficult to see that a constant special solution for Eq.8 exists for the error function. Since the special solution is the steady state response of the system, we have just shown that the PLL is able to follow a linear frequency ramp of reference signal with a fixed phase error.