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Considerations for the Design of the Beam Current Monitor System for the SNS

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March 2002

Collider Accelerator Department

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC)

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Considerations for the Design of the Beam Current Monitor System for the Spallation Neutron Source (SNS)

BNL/SNS TECHNICAL NOTE

NO. 104

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UPTON, NEW YORK 11973

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Rev1- March 5, 2002

The Spallation Neutron Source to be built at ORNL is comprised of a source of H^- particles (FE), a medium energy beam transport (MEBT), a linear accelerator (Linac), a high energy beam transport (HEBT), a stripper changing the H^- to H^+ and an accumulator ring (Ring), a ring to target beam transport (RTBT), and a target. Current wave shapes will vary at different places along the system. The source will generate charge bunches that will have an amplitude near 50ma peak (38ma peak in the MEBT,Linac, and HEBT), and bunch widths of 300ns to 645ns (defining a mini-pulse). The bunches are repeated at the revolution period about 945ns. This provides a "gap" time of about 300ns used by the ring to kick the beam out to the target. The pulses are accumulated by the ring for 1ms (about 1060 mini-pulses) after which the entire ring is dumped to the target. The process is repeated at a 60Hz rate. The 1 ms pulse duration constitutes a "macro-pulse". An RF micro-structure of 402.5MHz is generated by the accelerator RF.

The beam current will vary in amplitude from the near 50ma peak pulses with a pulsing duration of 1ms (chopper rise time about 10ns) in the MEBT, Linac and HEBT to a ramping pulsed current of near 50Amp peak and duration of 1ms in the Ring, and about a 50Amp 645ns pulse in the RTBT. This represents a dynamic range of 1000:1. Adding some resolution at the low end easily exceeds this by a factor of about 100. It is desired to provide a system capable of 1% accuracy with a resolution of 0.5% (resolution was relaxed from 0.1% to 0.5% in the Ring and RTBT to avoid excessive gain changing –see EMAIL from Fedotov 4/20/01).

AP Requirements (3/2001):

MEBT-to-HEBT:		
Range	15mA – 52mA	
Accuracy	1%	
Resolution	0.1%	
Data Structure	Inside mini-pulse	
Comments	----------	
RING-RTBT:		
Intensity	5E10 – 2E14	
Range	15mA – 100A	
Accuracy	1%	
Resolution	0.1%	resolution relaxed to 0.5%?
Data Structure	Turn-by-turn	
Comments	All are Fast Current Transformers	

Desired capabilities of this system are:

- **a comfort display output,**
- **calculation of average current and charge per macro-pulse,**
- **calculation of average current and charge per mini-pulse,**
- **ability to provide detailed signal wave shape of mini-pulse current and charge,**
- **ability to permit detailed analysis of the mini-pulse (examine the chopper characteristics),**
- **a representative analog version of each mini-pulse sent to the machine protection system (MPS).**
- **ability to store a minimum of 10 macro-pulses of raw data in a circular buffer for analysis upon demand (goal is 1 seconds worth of data),**
- **a self calibration capability**
- **remote and local operation**

In an effort to try to find a common design the choice of current transformer has been compromised to balance sensitivity for the lower currents and droop for the longer duration macro-pulse. It is felt that droop could be compensated using digital compensation techniques justifying this approach. Such a technique and initial simulation results will be presented later.

OVERALL CHALLENGES:

- **Providing capability to analyze the chopper edge (10ns), and still provide accurate measurements for the longer 1ms macro-pulse (choice of transformer)**
- **Dealing with large dynamic range – Gain change requirements with minimal loss of turn information**
- **Handling potentially large input voltages – selection of components and component protection**
- **Computation accuracy/resolution and selection of ADC and sampling rate**
- **Calibration pulse generator and techniques**

Transformer selection:

A number of approaches were considered before arriving at the Bergoz® FCT. The requirement to be able to analyze the edge of the mini-pulse requires a rise time less than 0.3 times the pulse rise time (3ns) to maintain a 10% rise time measurement. This is a bandwidth near 0.35/3*10E-9 or 100MHz. A transformer rise time less than 1ns (providing better than 1% measurement accuracy) was made a requirement. It is also desirable to have less than 0.1% droop during the 1 ms macro-pulse to maintain good pulse height accuracy. This requires a transformer time constant (L/R) corner greater than 1000*0.001s or >1 second (lower cut-off frequency of <0.159Hz). Thus, the transformer that would meet these requirements would have a lower cut-off of <0.159Hz and an upper cut-off >350MHz.

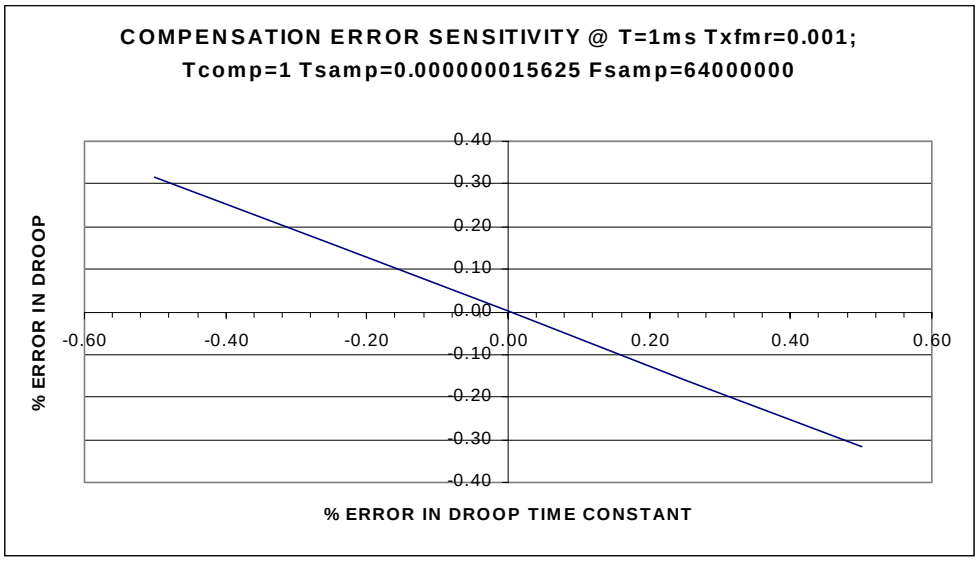
An initial attempt to design such a transformer achieved a lower cut-of 0.2Hz and upper cut-off at about 10MHz. This was abandoned, and an alternate approach pursued. The concept of utilizing two or more different transformers was addressed. This was

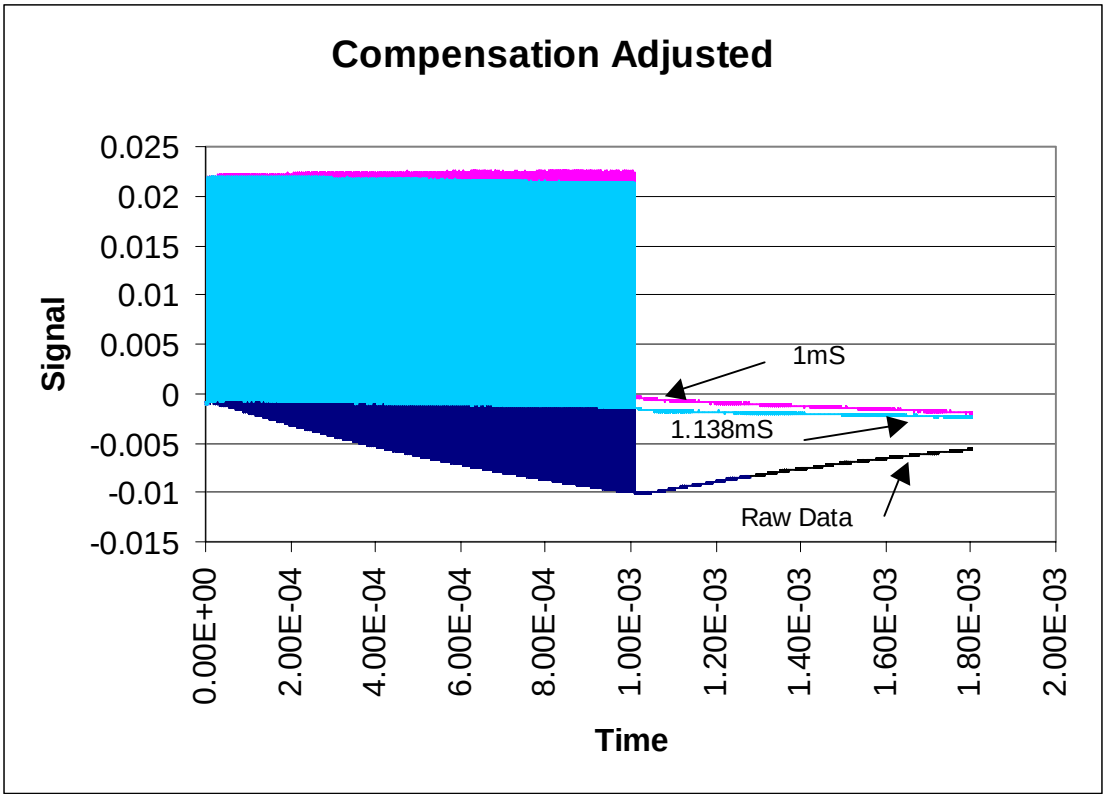
undesirable from a "common solution" point of view. The purchase of commercially available current transformers capable of 1ns rise time focused on transformers of the Bergoz® FCT type. Such transformers could provide a good compromise for sensitivity and droop for the short mini-pulse but suffered from considerable droop for the macro-pulse (0.1%/μs). The requirement to observe the rise time of the chopper was left to a fast digitizer/scope type acquisition system, while the slower macro-pulse information was addressed with a rise time near 50ns due to Ring beam dispersion after a number of turns. Communications with Bergoz and others led us to conclude that the FCT would work well in the high speed domain, while digital compensation could restore the low frequency corner to near 0.16Hz.

Bergoz was approached to design a balanced transformer (100:1), capable of driving a 78 Ohm balanced coaxial line. It was thought that such a configuration would minimize noise pick-up along the long (100 m) cable. The initial prototype transformer suffered from transient anomalies, and the balanced line suffered from a limited choice of cables and large losses at the higher frequencies. This concept was abandoned in favor of a more conventional 50 Ohm transformer with many cables to choose from to minimize cable distortion. A prototype transformer with 50:1 turns ratio and an additional winding of 10 turns for calibration injection was tested and performed well. This transformer provides a nominal 25 mV signal for a 50mA input current (suffers about 0.5dB loss due to internal resistors used to improve transient response and match the transformer to the coax), <1ns rise-time, and <0.1%/μs droop. Success with the prototype, an ability to obtain rad-hard transformers and an excellent working relationship with Julian Bergoz has prompted us to designate this transformer universally for the SNS. The MEBT has installed two small diameter units that appear to be working well.

The Digital Compensation Scheme:

To utilize the FCT in our application it is necessary to provide DC restoration and digital compensation of the transformer droop. An algorithm to accomplish this has been tested and appears to work quite well. It requires a good estimate of the transformer droop time constant (0.16% error in droop time constant for 0.1% error in droop) and DC restoration. The algorithm is based upon an IIR filter with a zero to cancel the transformer low cut-off pole, and replacement of the transformer low cut-off pole with a new pole at 0.159Hz. The DC restoration requires a measurement of the DC level just prior to the pulse. This is subtracted from the data set to restore the DC value to zero. The concept requires some averaging of the data to achieve good estimates of the offset and transformer droop time constant. This is accomplished with numerous readings and least square estimate calculations.





ie: $H(s)= (s+1/\tau_1) / (s+1/\tau_2)$

Where; $1/\tau_1$ is the transformer lower cut-off radian frequency,
$1/\tau_2$ is the desired new transformer lower cut-off radian frequency

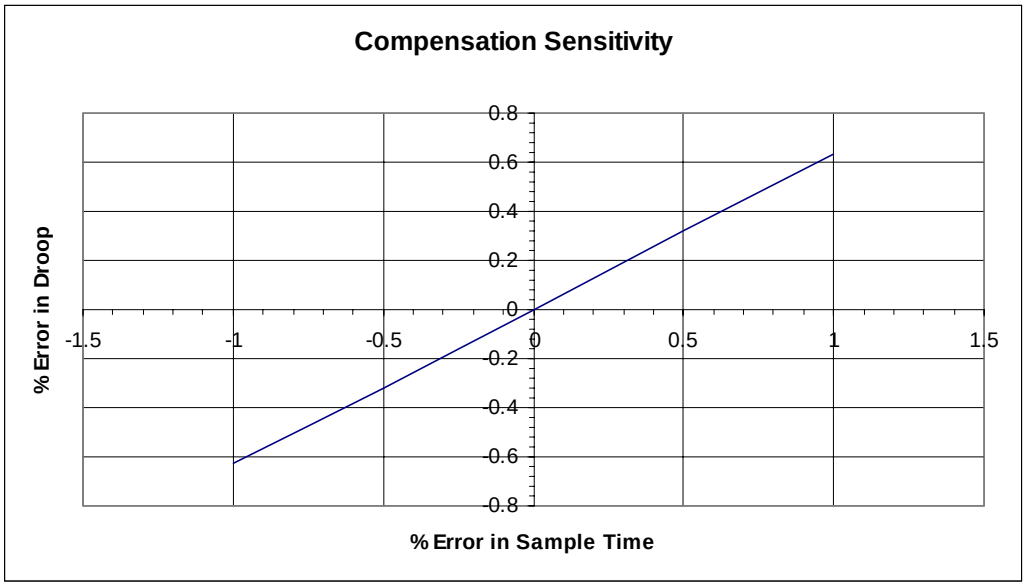
The Bilinear transform substitutes for s to obtain H(Z);

$$s= (2/T)*(1-Z^{-1}) / (1+Z^{-1})$$

Where; T is the sampling time interval

Yielding:

$$Y(n)=\{1/(2/T+1/\tau_2)\}\{y(n-1)\ (2/T-1/\tau_2) + x(n)\ (2/T +1/\tau_1) + x(n-1)\ (-2/T +1/\tau_1)\}$$



DC RESTORED AND DROOP COMPENSATED
CALIBRATION PULSE AND BURST
12-4-01
BCM single shot acq.vi
Raw Data
Filter Output
Time
Card
Immediate
Size
16384
Offset
Values read
Single shot
DC Restoration
points to skip at begining
points to average
Calc X-former time constant
points to skip at begining 2
points to process
amplitude
XFMR time constant
standard deviation
Calculated DC Offset
time constant
Sample Frequency (Hz)
IIR Filter Cluster
filter structure
Reverse Coefficients
Output Array

A screen dump of LabVIEW code that acquires data from the BCM electronics is shown above. Data was sampled at 40MHz, and only a short section of the simulated burst was available in the 16K FIFO acquisition board used to collect this data (a total of about 400us is stored and displayed). Another acquisition board received later with 64K FIFOs was capable of storing some zero offset data (about 50 uS, 2000 points), the calibration pulse (about 250uS, about 10000 points), the 1 millisecond burst (40000 points) and some of the recovery "tail" for analysis of time constant. Of particular interest is the ability to make slight adjustments to the droop compensation. This permitted very careful adjustments to be made, and by inserting a calibration pulse just prior to the simulated beam burst, the droop is calculated on the relatively large calibration pulse.

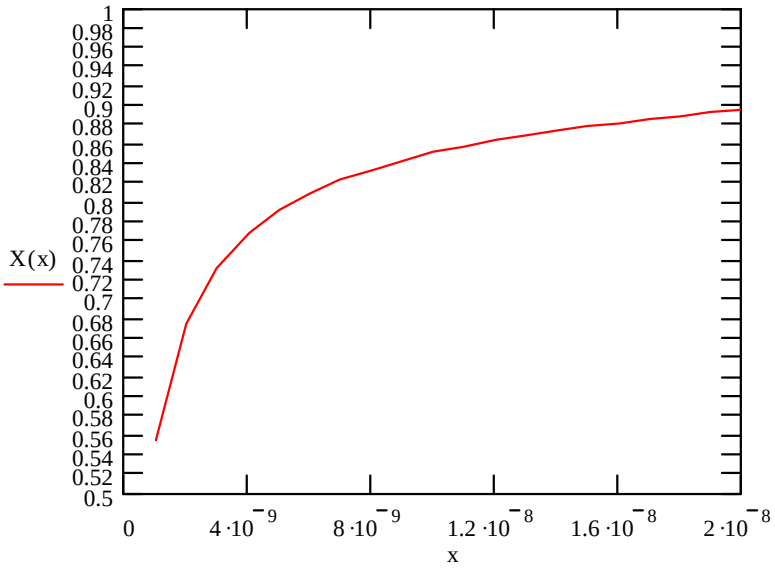
It has been observed that very small differences in compensated DC level are observable between the start and end of the macro-pulse when setting the compensation to the time constant calculated from the calibration pulse. A slightly different time constant is calculated when using the tail of the burst response (burst=0.001111, cal=0.0011376). The best response is obtained by using the "tail". It is felt that there is a slight calibration pulse time constant that we are seeing. This may be due to cable distortion, the pulse generator, or a DC offset error. This brings to light some subtle things that could cause slight compensation errors. The response of the cable to the signal during the tail is also a consideration, and since there is a difference in calculated time constants this affect would exist in both cases, and is not thought to be the main cause for the difference. DC offset errors and pulse shape are more likely at the root of the discrepancy. DC offset measurements based upon a 1900 point average yielded changing offset answers from run-to-run (-156 +/- 20 counts). A more careful investigation of this revealed a ground loop problem between the calibration pulse generator and the transformer ground. Just touching the grounds together produced a DC offset change in the output of the electronics. Grounding the cable shield to the electronics directly provides no change in offset. With the calibration pulse generator removed, DC offset calculations varied only –246 +/- 0.2 counts for a 1900 point average (note shift in offset). The calculation of transformer droop time constant varied about 0.001103 +/- 0.000002. The final version of transformer ordered for this system was requested with isolated calibration windings, permitting measurement of current into this winding on the return line, and avoiding a ground loop problem.

Using a calibration pulse before the beam arrives is advantageous due to the fact that this is the more quiet time. The more accurate calculation, it seems, is made during the beam tail, however, this could be during a relatively noisy time (after the kicker etc.). The software has been written to permit adequate control to set the desired window for this calculation. In addition, small changes could be made to the compensation time constant to achieve the droop desired.

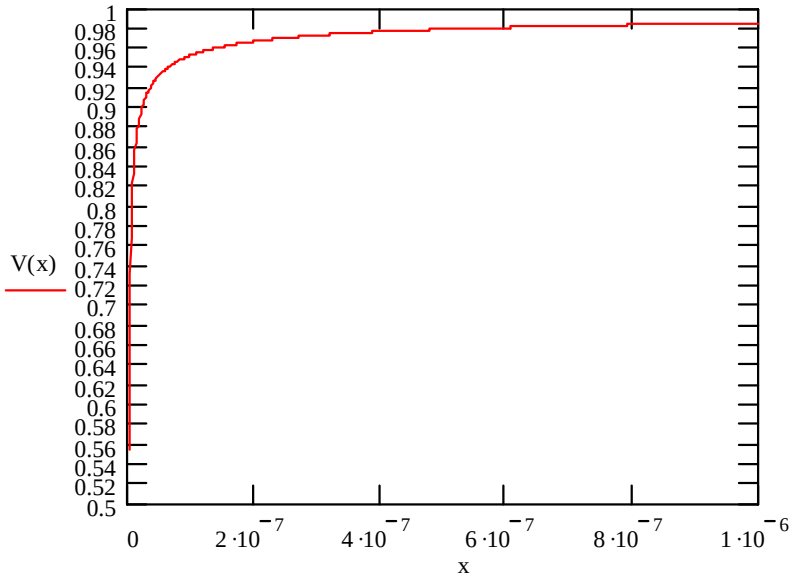
Cable Distortion:

A Mathcad analysis was performed using parameters of a ¼ inch Heliax Cable #456 to estimate the affect of distortion on a step input. The results are shown in the figures below comparing 1/4", 3/8", and ½" Heliax.

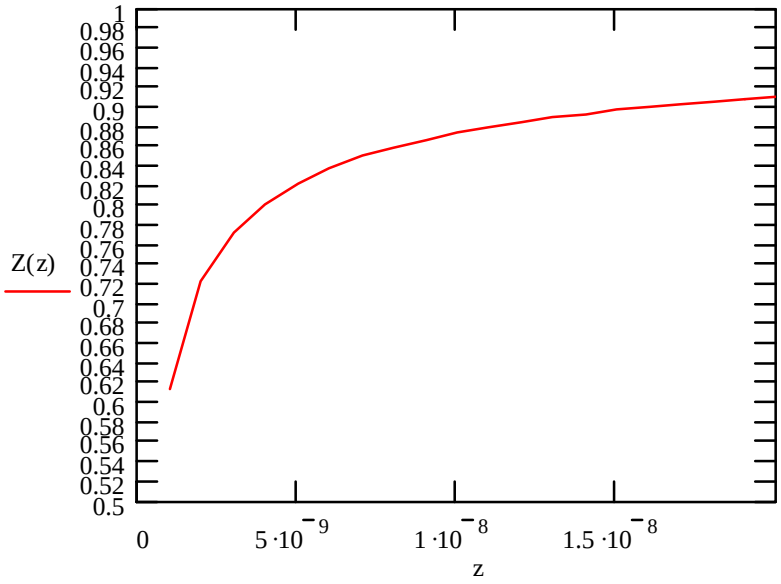
100m - 1/4 inch Heliax Cable (type 456 w/2.20dB loss per 100m @ 30MHz) response to a step



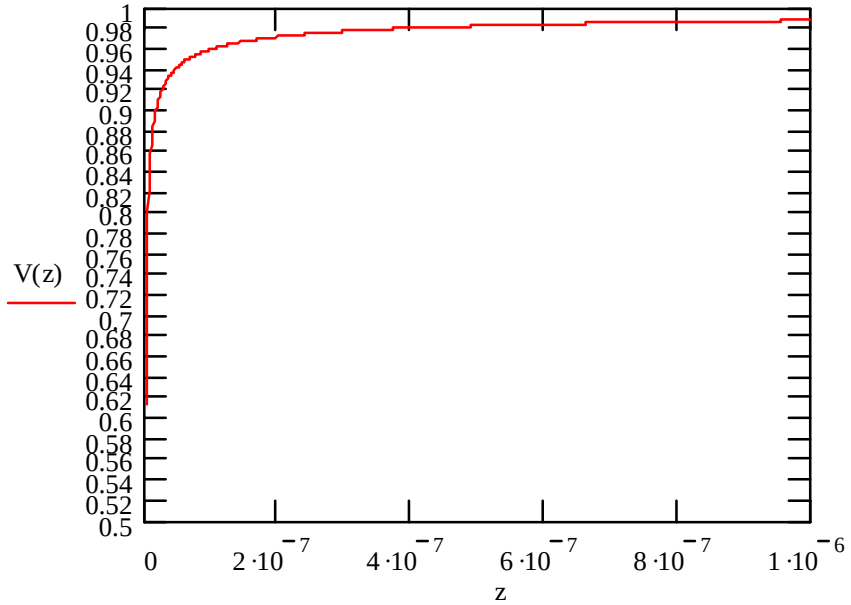
100m - 1/4 inch Heliax Cable (type 456 w/2.20dB loss per 100m @ 30MHz) response to a step



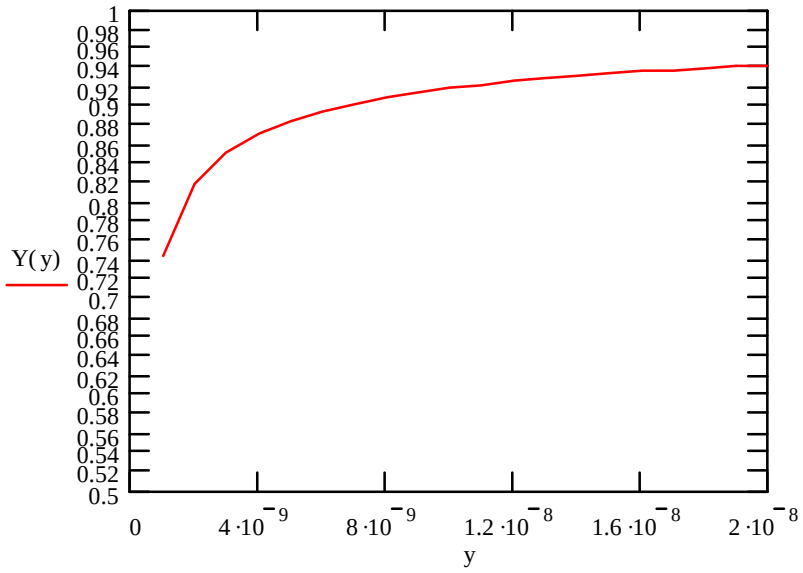
100m - 3/8 inch Heliax Cable (type 458 w/1.87dB loss per 100m @ 30MHz) response to a step



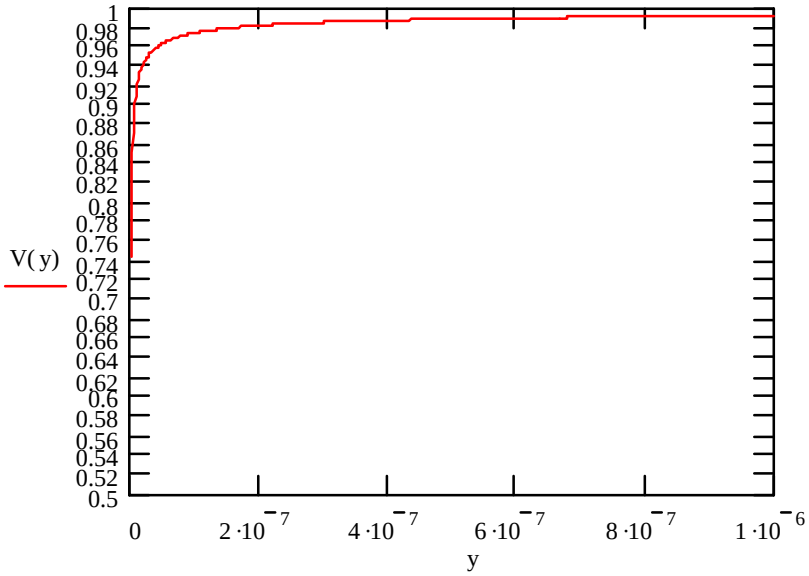
100m - 3/8 inch Heliax Cable (type 458 w/1.87dB loss per 100m @ 30MHz) response to a step



100m - 1/2 inch Heliax Cable (type 461 w/1.21dB loss per 100m @ 30MHz) response to a step



100m - 1/2 inch Heliax Cable (type 461 w/1.21dB loss per 100m @ 30MHz) response to a step



The response to a step for the ¼ inch Heliax indicates that the signal is in error of about 3% after 300ns and 1.6% after 1us. Therefore, there will exist an error in accuracy that must be corrected during the calibration cycle. One can see from the plots above that the 3/8 inch Heliax and ½ inch Heliax have improved transient response. The 3/8 inch providing 1% error at 1us, and the ½ inch 0.5% at 1us. The rise times also improve, with the time to 90% of 22.25ns for the ¼ inch, 16.075ns for 3/8 inch and 6.73ns for ½ inch. Based upon this analysis, the 3/8 inch Heliax is a preferred choice since the rise time is near 1/3 the rise time of the 7MHz filtering.

In addition, the response exhibits a slope that will modify the droop response during calculation of the droop time constant. To examine more closely this effect, the analysis was expanded to include up to 10us and the axes were scaled to measure the slope. It was found that the amplitude was 0.99527 and the slope 2.6E-4/us (0.026%/us). Therefore waiting for 10us before performing a calculation of droop time constant should provide sufficient time for the cable to stabilize sufficiently for accurate calculation of time constant.

Bandwidth, and Filter consideration:

There are two signal bandwidths to consider. To examine the chopper edges, a bandwidth in excess of 100MHz is required. This is expected to be done by a separate high speed digitizing system like a scope. The second requirement is to analyze the general shape of the mini-pulse and macro-pulse. The system will be capable of following the mini-pulse, however, due to beam dispersion after a number of turns in the ring, the edge is expected to deteriorate to near a 50ns rise-time. To observe this a bandwidth of about 0.35/50E-9 = 7MHz is required. Therefore, a 7MHz Gaussian filter will shape the signal before it goes to the ADC. This will limit the noise bandwidth and provide a system response that suffers no overshoot. In addition, The response of the filter must return to baseline between mini-pulses (300ns max). A 5 pole Gaussian filter will return to baseline to within 0.1% in about 6 time constants (use 6.2 for Gaussian). Therefore, the smallest bandwidth filter that must be considered is about $6/2\pi(300E\text{-}9)$ = 3.2MHz. Such a filter has a rise time (0.1 to 0.9) of about 2.12*50ns = 106ns (use $2.135*\tau_c$ for a Gaussian). The estimated rise time for a 7MHz Gaussian filter is 2.12*22.7ns = 48ns (Duration of impulse response and Rise time of 5 pole Gaussian was estimated from curves for impulse and step response in Zverev, “Handbook of Filter Synthesis”, Wiley 1967, pg. 406; the Gaussian numbers in parenthesis were derived from a table of the integral of the Gaussian distribution providing probability information and the transform pair $\exp(-\alpha t^2) \leftrightarrow \exp(-\omega^2/4\alpha)*\sqrt{(\pi/\alpha)}$ where $\alpha=1/2\sigma^2$ and σ is the standard deviation). Resulting signal rise time is expected to be sqrt(48^2 +50^2)=69ns.

The ADC sampling near 65MHz has a potential bandwidth of 32.5MHz (preferably synchronized to the revolution frequency by operating at 4 times the reference clock frequency of about 16MHz), and since the analog part of the ADC is wide-band for under sampling applications the signal bandwidth should be limited. This is accomplished by the AD602 variable gain amplifier which has a bandwidth of 35MHz, and by placing a 5-pole 7MHz Gaussian filter just before the AD8138 ADC driver. The 5 pole Gaussian filter provides attenuation at $5*f_c$ (35MHz) of about –43dB, the AD602 adds another –3dB for a total of about –46dB. At about $8*f_c$ (65-7=58MHz) the signals are attenuated by about –68.3dB (-63dB for the filter and –5.3 for the amplifier). This will attenuate all

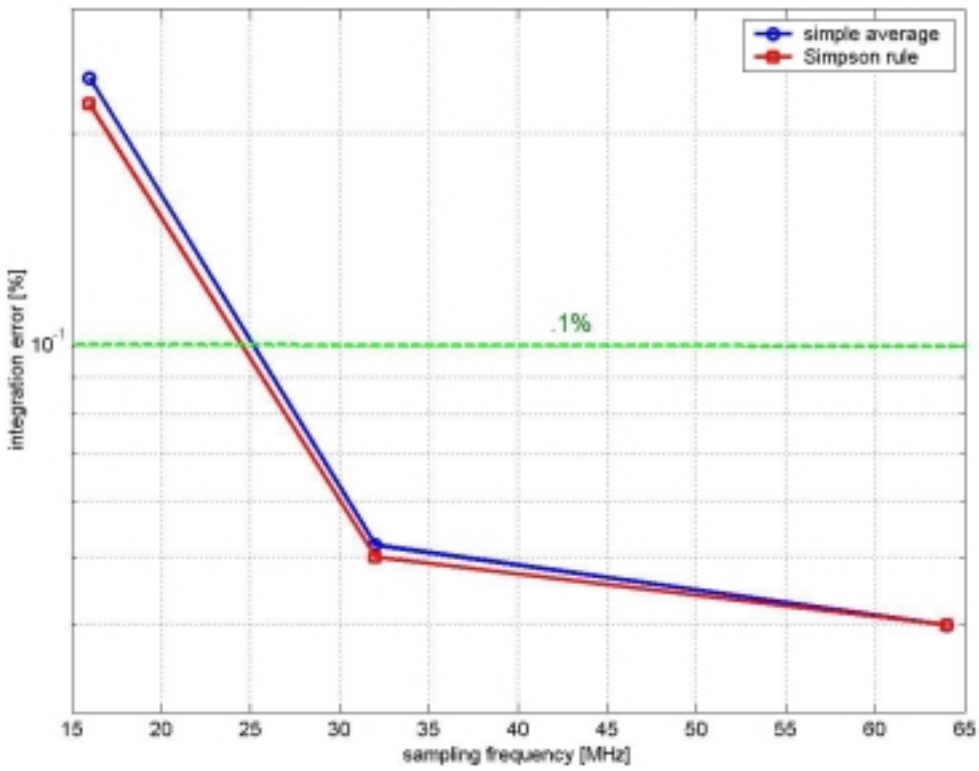
aliased information in the passband of the filter by –66dB which will cause corruption of the data by < 0.04% in the 7MHz passband of interest.

Beam pulse power at high frequencies can corrupt the data due to aliasing. To minimize this, an additional 5 pole 0.01dB Chebyshev filter with corner at 17MHz. This filter will provide an additional –37dB at about 32MHz. The result is in excess of –80dB at the Nyquist frequency. Therefore, beam spectral power aliased to base-band will be attenuated by more than 1 part in 10,000 or 0.01% (1 lsb for a 14 bit ADC with sign and 13 bit magnitude).

The sampling rate selected will also affect the computation of charge since it is a digital integration of the current signal. A simulation of a Simpson's Rule integration algorithm, and a simple sum was conducted (by M. Kesselman (BNL), and independently by Alexander Aleksandrov "Sasha" (ORNL)). This simulation places a typical HEBT current pulse through a 5-pole 7MHz Gaussian filter, and computed the error in the charge calculation.

Three sampling rates were analyzed, 16MHz, 32MHz, and 64MHz. One can see from the plot below that to achieve <0.1% error in the integral one must sample at more than 25MHz. It is also interesting to note that the error converges after 65MHz providing no advantage to using the more computer intensive 3 point Simpson's rule. The difference is not very much at lower sampling rates indicating that the simple sum can be used with minimal loss of error. This analysis included time shifting the input pulse to obtain the largest error.

Therefore, the choice of a 32 or 64MSa/s rate (at 2 or 4 times the reference signal of about 16MHz) seems justified.



Anti-aliasing:
The characteristics of the Gaussian filter or a Bessel filter are quite broad, and offer about -43dB for the Gaussian, -47dB for the Bessel at 32MHz. To provide better filtering at the Nyquist frequency, a 17MHz - 5 pole 0.01dB Chebyshev filter has been added. This provides an additional –37dB attenuation at 32MHz, for a total of >-80dB. Additional attenuation due to other amplifier stages further attenuates the signal at 32MHz. This will yield better than 10,000:1, or more than 13 bits, and provide adequate anti-aliasing.

Gain Change:
The large dynamic range requires a method to address signal amplitude variation. Having finalized the transformer sensitivity to about 25mV per 50mA peak current mini-pulse, yields a transformer output that could go to 25 Volts in the Ring and RTBT. In addition, we need to allow some “headroom” which has arbitrarily been established as a factor of two to accommodate peaked pulse profiles (or maximum input voltage of 50V).

Initially we looked into switches to change gain. These switches must handle the potentially large input voltage (50V). This narrowed our search to relays, since fast semiconductor switches start to distort near +30dBm. Relays suffer from slow response time, and are not well suited to switching in nanoseconds. Alternate approaches were investigated including:

- Ping-pong amplifier schemes – changing gain in one path while viewing the output of the other,
- Building our own analog switches,
- Providing protected input amplifiers in lieu of disconnecting with switches
- Dual amplifier digitizer paths with digital multiplexing of ADC outputs
- Switched amplifiers – sometimes used in fast analog multiplexers, or power conservation circuits.

The ping-pong approach is a good approach to avoid losing a turn of information. The semiconductor switches have proven to have voltage, distortion and DC transmission problems. The relays are too slow. Separate digitizer paths are too costly in board real estate, power and money. The concept of protected amplifiers with switched amplifiers was pursued.

An initial investigation of the number of gains required yielded 7 or 8 gains for 0.1% resolution. The resolution was relaxed to permit 4 gains. Based upon a noise estimate for an AD6644 ADC (a +/- 1.1V, 13 bit plus sign, 65MSa/s unit), ADC worst case noise is estimated at –72dB below 0.98V (-1dB Vmax) or 0.246mVrms, the minimum input signal to the ADC should be 200 times (1/.005 for 0.5% resolution) the noise or 49mV (a ratio of 10.2 to achieve a peak signal of 0.5V or half scale). If a half scale signal for 50Amps (25V input) is assumed, gain settings can be estimated as follows:

TURN	INPUT		OUTPUT	GAIN
Turn 1000	50A	25V	ADC input = 0.5V	Gain=0.02
Turn 98	4.9A	2.45V	ADC input = 0.049V	Gain=0.02
Turn 97	4.85A	2.425V	ADC input = 0.5V	Gain=0.1031
Turn 19	0.95A	0.475V	ADC input = 0.049V	Gain=0.10316
Turn 18	0.9A	0.45V	ADC input = 0.5V	Gain=1.1111
Turn 2	0.1A	0.05V	ADC input = 0.0555V	Gain=1.1111
Turn 1	0.05A	0.025	ADC input = 0.5	Gain=20

These initial estimates of gain were modified slightly (see below) after considering amplifier protection circuitry noise and other amplifier noise which modifies the initial estimate.

Amplifiers and noise estimates:
ADC Pre-amp;
The ADC6644 requires a differential input signal and an offset to about 2.5V since the ADC is a single supply device. The recommended driver is an AD8138 which handles the DC shift and single ended to differential drive conversion. It is matched to the ADC and delivers a wide bandwidth (300MHz to match the ADC analog front-end) and low distortion. This drive scheme improves noise immunity by the inherent common mode rejection of the differential drive, and reduces harmonic distortion. The differential amplifier is operated at unity gain to minimize additional noise. The amplifier has a voltage noise of 5nV/rtHz and when used with 4 - 500 Ohm resistors, the output noise expected is about sqrt((5E-9^2+5.7E-9^2)*(300E6))=131E-6V.

Adjustable Gain Amplifier;

Logarithmic amplifiers were eliminated due to their nonlinear transfer function. It is desirable to have a linear system since we will be doing digital processing. Although fixed gains will be used, the AD600, AD602, and AD603 adjustable gain amplifiers were considered for computer control of gain for flexibility. These amplifiers utilize a well-controlled variable input attenuator with a fixed gain amplifier at the output. This configuration works nicely providing variable gain without affecting frequency response. The AD603 is a single 95MHz-bandwidth device, while the AD600 and AD602 are dual 35MHz bandwidth devices. The 35MHz bandwidth is more matched to our needs. The AD602 provides -10dB to +31dB gain per stage, and the AD600 provides 0dB to 41dB gain per stage. They are pin compatible. These amplifiers have a constant output noise due to the constant amplifier gain, with known input ladder network impedance. The equivalent input noise of 1.4nV/rtHz at the highest gain setting (or 158nV/rtHz at the output) is expected. This will yield about 418uV noise at the amplifier output for a 7MHz bandwidth.

Protection;
With signal inputs potentially as large as 50 V, one must consider protecting the amplifiers. The AD600/AD602 has a maximum input voltage limit of +/- 2V continuous and +/-Vsupply for 10ms. This amplifier is difficult to protect with diodes since the diodes will distort input signals as they get large. Attenuating the input to assure the signal does not exceed +/- 2 volts requires an attenuation gain of 0.04. A single turn providing about 25mV peak signal will be attenuated to 1mV peak, and when amplified by the AD600 (G=100) will yield only 100mV which provides an output s/n ratio of only about 200. This is marginal.

Placing a protected amplifier with known output limits, in front of the AD600/AD602, will assure proper input voltage control. A protected amplifier configuration incorporates low capacitance back-to-back diodes at the input terminals of the amplifier to assure that the differential input voltage does not exceed allowable limits (signals are held near ground during normal operation). The input amplifier should be low noise, provide a bandwidth commensurate with a 50ns rise time, and provide good transient behavior. In addition, it is clear that the gain-changing scheme will require attenuators. The attenuators must not be affected by the changes in loading as the protection diodes saturate with increased voltage. To accomplish this a number of amplifier circuits were simulated using Pspice. The result was a need to limit clamping diode currents to avoid exceeding diode and amplifier differential input voltage limits. This lead to using a series 1K Ohm resistor to a low capacitance HSMS2812 dual Schottky diode (2pF). This large value of input resistance will generate significant noise, and must be included in the noise estimates (see noise section).

To estimate the attenuator loading changes we assume the diode will drop about 1 Volt, and a 3dB 150 Ohm pad is used to isolate the load from the source. The pad is an 866-52-866 Pi pad. This is loaded at the source end with two 150 ohm pads and a 50 ohm terminated line (the transformer), and at the output by an appropriate 150 ohm load made up from 176 Ohms and 1K plus diode as a load.

From “Reference Data for Radio Engineers” for a pad:

$\Delta Z/Z = 2(\Delta Z_2/Z_2) / [2N+(N-1)(\Delta Z_2/Z_2)]$; N is power ratio from input to output

Therefore, for N=2 (3dB);

$$\Delta Z/Z = 2(\Delta Z_2/Z_2) / [4+(\Delta Z_2/Z_2)]$$

or: $\Delta Z_2/Z_2 = k*4/(2-k)$; where k is a fractional error in the input impedance.

For the case of 0.1% ie: k=0.001, we get $\Delta Z_2/Z_2 = 0.002$ or 0.2% change in load impedance will yield 0.1% change in input impedance. Since there are three paths in parallel defining the load on the coax line, this sensitivity is relaxed by a factor of 3.

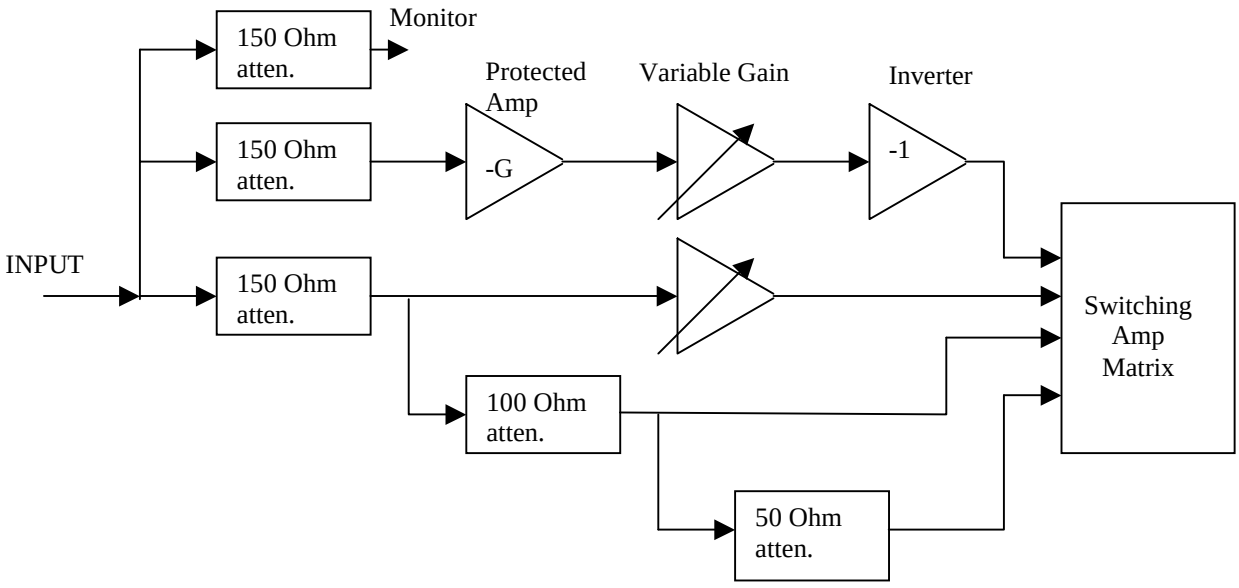
For resistors R and R_L in parallel;

$$(\Delta R_p/R_p) = R/(R+ R_L) (\Delta R_L/R_L)$$

The load on the 3dB pad can vary as much as 0.6% and maintain a 0.1% change of coax match.

For 35 Volts out of the 3dB pad (50 volts input), a one volt drop across the diode will modify the effective input resistance $R[V/(V-V_{diode})]$. The effective resistance change is about $R(V_{diode}/V)$ or R/35 (2.857%). From this we can determine the resistors we should use for the amplifier input. The minimum amplifier resistor is 713 Ohms with a pad terminator of 190 Ohms to achieve a maximum delta resistance of 0.1% for the 50 Ohm cable termination.

The protected amplifier should provide a gain that would tend to dominate the noise at this stage. It will also provide a maximum output signal of about 4 volts requiring an attenuator of about 0.5 limiting the signal to 2 volts as required by the AD600. A block diagram is shown below.



Analog Block Diagram

Switching amplifier matrix:
The switching amplifier scheme uses a TI/Burr-Brown OPA680 series amplifier. This amplifier can be switched off in 100ns and on in 25ns. When this is used in a positive gain of two configuration, the feedback and input resistors are effectively disconnected from the amplifier, and the amplifier output can be represented as a 4pF capacitor. If this feeds a summer, we can implement a fast switching amplifier selector switch. The "Gap" time of 300ns in the signal with edges of about 50ns leaves a period of about 200 ns to achieve proper switching without the loss of a turn of data. The output capacitance and resistor load will yield a time constant in the 6 ns range, which is far less than the switching time. For this reason the OPA680 series has been considered as the switching device. Each switching amplifier constitutes a separate gain path for the signal. For the simplest data reduction afterwards, separate offset adjustments to balance accumulated DC offsets in each path are recommended. DC offset measurements should be made for each gain path.

Input attenuation;
An input attenuator scheme was selected that distributed signals to three major signal processing paths. The paths were chosen to have a 150 Ohm input impedance to yield a 50 Ohm match to the signal cable and current transformer. One path delivers a sample of the signal to an output port for high-speed data acquisition. A second delivers signals to the high gain single turn signal path through a 150:150 ohms 3dB pad. This feeds a protected amplifier since signals are expected to be as high as 35V (0.707 * 50V = 35V). The third path is an attenuator chain that provides sufficient attenuation to permit using an AD600/AD602 with no protection. This requires an attenuation gain of <0.04; a gain of 0.03886 was selected yielding 1.94 Volts maximum. The amplifier will make up the attenuator loss and provide a gain near 28. This path is attenuated about 6dB (G=0.018868) to achieve a full scale output for 53V input (1060 turns @ 100ma per turn).

Max Gain of AD600/AD602 and Noise at ADC:
If we assume unity gain through out all amplifier sections following the AD600/AD602, we require a gain of 20/.707 = 28.3 (29dB) in the AD600/AD602. Noise from the protected amplifier (see later, approximately 8.4nV/rtHz) will be amplified to 8.4*28.3 = 238nV/rtHz. This added to the noise out of the AD602 is 285nV/rtHz. (sqrt(158^2 +238^2)). This noise when limited by a 7MHz Gaussian filter yields 755μVrms. The ADC noise has been estimated at 246μVrms. The resulting noise at the ADC is 794μVrms. The signal will be 0.025*20=0.5 V for S/N ratio of 630 or a resolution of 0.16%.

The protected amplifier:
The higher gain paths will require protected amplifiers to assure that the input levels are not exceeded. As pointed out earlier, the diode protection requires about a 1K series resistor to assure that the diode voltage and currents are kept low (for a BAS70 it is 1V at 17 ma; for an HSMS2812 it is 1V at 35ma). This assures the diodes would properly limit, and can support the signal levels.

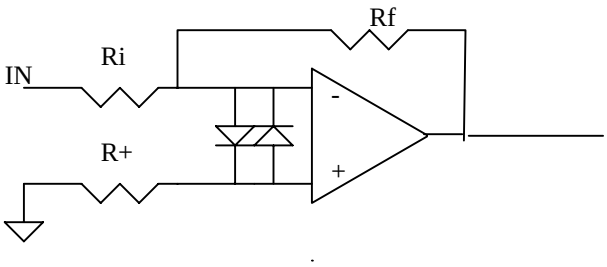
The OPA 680 and OPA 620 voltage mode amplifiers were considered for a protected amplifier stage. They are inexpensive, come in packaging of 1 (OPA680/OPA 620), 2 (OPA2680), or 3 (OPA3680) per IC, and provide relatively wideband response (200MHz GBWP). The wide bandwidth is good to allow a separate Gaussian filter to do most of the signal shaping later on in the signal flow path.

Noise associated with the input resistor, and feedback resistor is considerable with such large values as 1K for Rin and 4K for Rf (G=-4).

Noise associated with the 1K current limiting resistor, at 300 K, will yield
E_{1k} = sqrt(4KTR)/rtHz

E_{1k} = 4.07nV/rtHz

The output noise of the amplifier is :



E_{no}^2 = (E_{Ri}*A_v)^2 + (e_{n*}(1+ A_v))^2 + (i_{n-}*R_f)^2 + [(i_{n+}*R_+)^2 + (E_{R+})^2]$_*$(1+ A_v)^2 + E_{Rf}^2

For; A_v = R_f/ R_I ; K=1.38E-23 ; q=1.6E-19 ; f_c=noise bandwidth
E_{Ri}=sqrt(4KT$R_I f_c$) ;
E_{R+}= sqrt(4KT$R_+ f_c$) ;
E_{Rf}= sqrt(4KT$R_f f_c$) ;
e_n= amplifier equivalent input voltage noise ;
i_{n-}= amplifier equivalent inverting input current noise =sqrt(2q$I_{bias-} f_c$) ;
i_{n+}= amplifier equivalent inverting input current noise =sqrt(2q$I_{bias+} f_c$)

For the OPA680 – Operating at an inverting Gain of 4 with R_i =1K, R_f =4K and R_+=0; (noise= 6nV/rtHz, GBW=200MHz, 3.5pA/rtHz) voltage mode amplifier:

Optimum noise figure at Rs=En/In=1.7K Ohms

E_{no} = E_{2k}*A_v + e_{n*}(1+ A_v) + i_n(R_f) = sqrt[(4.07*4)^2 + (6*(1+4))^2 + (0.0035*4000)^2 + 8.2^2]

E_{no} = 37.8nV/rtHz

For the OPA620 – Operating at an inverting gain of 4 with R_i =1K, R_f =4K and R_+=0; (noise=2.3nV/rt Hz, GBW=200MHz, 2.3pA/rtHz) voltage mode amplifier;

Optimum noise figure at En/In=Rn=1K Ohms

E_{no} = sqrt[(4.07*4)^2 + (2.3*(1+4))^2 + (0.0023*4000)^2 +8.2^2]

E_{no} =23.4nV/rtHz

The OPA620 will provide about 2/3 the noise of the OPA680 when these large resistor values are used and will be considered as the preferred choice. The noise is amplified by the variable gain amplifier, which has an inherent output noise near 158nV/rtHz, even though the gain will be near 7.07 (28/4). It produces sqrt(165.5^2 + 158^2)= 229nV/rtHz at the output of the AD600/AD602 set for a gain of 7.07 (total gain= .707*4*7.07=20). For a bandwidth of 7MHz the resulting noise due to the preamplifiers to the ADC system can be expected to be about 0.605mV. This is added to the ADC noise of 0.246mV for a total of 0.653mV. Therefore at this gain setting one would like to see a signal at the ADC of about 200 times 0.65mV, or 130mV minimum.

From a noise consideration point of view, the protected amplifier arrangement with a total gain of 20 will develop about 653uV noise including the ADC. If we include an attenuator near 0.04, the protected amplifier can be eliminated reducing the estimated noise to about 485uV for the variable gain amplifier and ADC. As the total gain requirement falls below 0.04 the variable gain amplifier can be removed reducing the estimated noise to just that of the ADC or 246uV.

The single turn is expected to be about 25mV for a 50ma pulse providing a signal to the ADC of 0.5V (20*0.025). This provides a s/n ratio of 769 or 58dB. The minimum input level of 15ma will provide about 7.5mV and will yield an ADC signal of 150mV or a s/n ratio of 230. Therefore, the gain of 20 will work well for the first turn, and throughout the MEBT, Linac and HEBT.

For use in the Ring, the variable gain amplifier gain can be reduced to provide a s/n ratio of about 200 for the single turn case. This will require a gain of 5.224 total. Therefore, gain is distributed as 0.707 for the attenuator, 4 for the protected amplifier, and 1.696 for the variable gain amplifier. With this total gain, the signal will achieve a level of about 0.5 volts at the ADC after turn 4. The next gain step would eliminate the protected amplifier yielding a noise of 485uV, and requiring a total gain of 0.776. This can be 0.03886 for the attenuator, and 19.97 for the variable gain amplifier. The next gain change would occur at turn 26. Gain for turn 27 to 276 is 0.0726. This would eliminate the variable gain amplifier requiring a gain of 1.868 for the preamplifiers. The gain required at turn 277 is 0.00707 which will be useful till turn 1060, however, setting gain to 0.018868 will provide the maximum s/n at the maximum number of turns.. This is reflected in the table below.

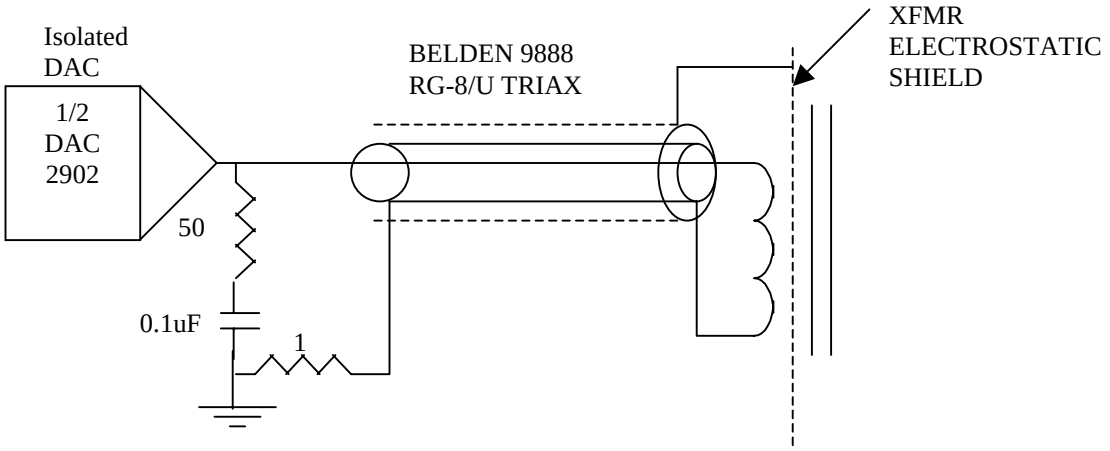
The resulting Gain Table is shown below:

TURN	INPUT CURRENT	INPUT VOLTAGE	TOTAL GAIN	ADC SIGNAL	ESTIMATED NOISE	S/N
1	50ma	25mV	20	0.5V	0.653mV	1555
1	50ma	0.025V	5.144	0.1286V	0.643mV	200
4	200ma	0.1V	5.144	0.5V	0.643mV	1555
5	.6A	0.125V	.776	0.097V	0.485mV	200
26	1.3A	0.65V	.776	0.5V	0.485mV	1040
27	1.35A	0.675V	0.0726	0.049V	0.246mV	200
276	13.8	6.9V	0.0726	0.5V	0.246mV	2032
277	13.85A	6.925V	0.018868	0.130V	0.246mV	531
1060	53A	26.5V	0.018868	0.5V	0.246mV	2032

Calibration:
The calibration winding must be terminated in 50 Ohms to correctly terminate the transformer for good transient response. A 50 ohm line is required for both windings. It is planned that a separate current calibrator will be used to generate pulses that approximate the waveshape of the beam. Due to the 10 turns, only $1/10^{th}$ of the simulated beam current is required. This is 5ma for the single turn case in MEBT, Linac and HEBT, and a ramping or equivalent current of 5A peak for the Ring. The lowest current measured on the highest range is 9.75A requiring only about 1 Amp to simulate it.

We will monitor the current with a series resistor that is 0.1% accurate. We can use Kelvin wired current shunts from Isotek Corporation, 435 Wilbur Ave., Swansea, MA 02777 (508-673-2900). Isotek makes ISA-PLAN precision resistors, of which their AN and A-H units are available in 0.1% tolerances from 1mOhm to 100 Ohms. Data can be filtered and digitized with a slow digitizer with 12 bit resolution at the revolution rate near 1MSa/s.

A TI/Burr-Brown DAC2902 (12 bit current output) has been investigated as a potential calibration source. This DAC provides 0 to 20 ma with a 1.25 volt compliance. To provide good cable termination for the calibration winding, and no error in current delivered to the winding, a 49.9 Ohm resistor in series with a 0.1 uF capacitor is used at the source end to terminate the cable. This provides a 5 us time constant that represents only 2% of the calibration signal delivered to the winding. Therefore, long calibration pulses (of the order of 250us or more), and data pulse strings suffer only slightly at the beginning. A 50 Ohm resistor in series with the output of the DAC, with zener diode protection at the DAC output, can provide DAC protection for large signals appearing on the calibration winding.



Example of calibrator circuitry

APEX manufactures high voltage, high power amplifiers. The PA92 can be powered by +/- 200 Volts and can deliver 4 Amps. The frequency response of this unit, however, is about 100KHz at these levels. Therefore, the current pulses for the higher ranges will be presented as a ramping pulse train with pulse duration of the order of 20us. The transformer will suffer some droop. The digital compensation should correct for the droop and compute appropriate currents for comparison with the calibrator. Alternatively, a current output DAC can be used to drive low currents into a terminated cable (requires about 49 Ohms in series with the calibration winding). Higher currents can be delivered by an audio amplifier and signals in the audio range used for calibration.

The 50 Ohm termination required on the calibration winding offers a problem during normal operation in the Ring and RTBT. With a 10 turn calibration winding, the voltage expected on this winding is $1/5^{th}$ the output winding voltage (10 Volts peak for 100A peak). A termination of 50 Ohms will dissipate 2 Watts peak, 0.04 Watts average.

Jullian Bergoz has pointed out that “standard” methods to deal with calibration windings is to mechanically disconnect the winding to avoid noise introduced by the calibration winding. This technique is a good one for cases not requiring continuous calibration. It is not clear how often the transformer must be calibrated, and this technique may be the best solution to the problem.

Our experience, so far, indicates the transformer is stable for low level inputs. This indicates the calibration technique is applicable for MEBT, Linac, and HEBT. We have not yet applied large effective calibration currents to determine the stability of the transformer to large currents followed by small currents. Bergoz has indicated that he expects the transformer to have residual magnetism in the core as a result of the larger currents, and that this will probably cause inductance changes. These inductance changes will affect the droop time constant.

Conclusions:
A Bergoz FCT with 50:1 turns ratio matched to 50 Ohms, with a sensitivity of 0.5V/A, a droop of 0.1%/us, and a 10 turn calibration winding, will act as an appropriate transducer when coupled with digital base-line restoration and droop compensation.

An approach involving switched gain paths must be used to accommodate the very large signal voltage levels and gain changing requirements. This method requires the use of protected amplifiers that use Schottky diode protection across their input terminals. To achieve an insignificant change to attenuator impedance as the diodes conduct and selecting low capacitance diodes required the use of large resistors and a –3dB attenuator. This results in significant noise introduced by this stage. The signal levels are estimated to be large enough to accommodate this noise when used with a gain of 20 for single turn operation or throughout the MEBT, Linac, and HEBT.

The Ring and RTBT will require three additional gain changes to maintain a near 200 s/n ratio. A gain table has been prepared indicating separate gains at turn 1, 5, 27, and 277 for the Ring, while only two gains will be used for the RTBT, one for studies and one for normal operation. These gains can be switched between macro-pulses.

A calibrator will be designed to stimulate the calibration winding. A current shunt will monitor the calibration current waveshape and amplitude. A simple current output DAC will provide signals to calibrate the two most sensitive gain paths. In addition, short circuit current will be measurable off-line to assure proper operation of the calibrator. The two high signal paths will be calibrated using an amplifier capable of delivering about 4 Amps peak. This will be done with a slower pulse.

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTES:
1: All Resistors 0.1w surface mount 1%
Unless otherwise specified
1W – 2512
1/4W – 1210
1/8W – 1206
1/10W – 0805
R65–68 ARE RESISTOR PACKS
CTS–766163101G–2%
47uF caps are 10WV

5 pole 7 MHZ filter

5 pole 17 MHZ filter

Note : Do not install R67

Note : To be placed on the
4 corners of the board

COMPANY:	BROOKHAVEN NATIONAL LAB		
TITLE:	MEBT BCM AFE CONTROL LOGIC AND CONNECTOR INTERFACE		
DRAWN: AJDP	DATE: 10/22/01	CODE:	SIZE: C
CHECKED:	DATE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATE:	SCALE:	SHEET: 1 OF 2
RELEASED:	DATE:		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTES:
1: All Resistors 0.1w surface mount 1%
Unless otherwise specified
1W - 2512
1/4W - 1210
1/8W - 1206
1/10W - 0805
R65-68 ARE RESISTOR PACKS
CTS-766163101G-2%

5 pole 7 MHZ filter

5 pole 17 MHZ filter

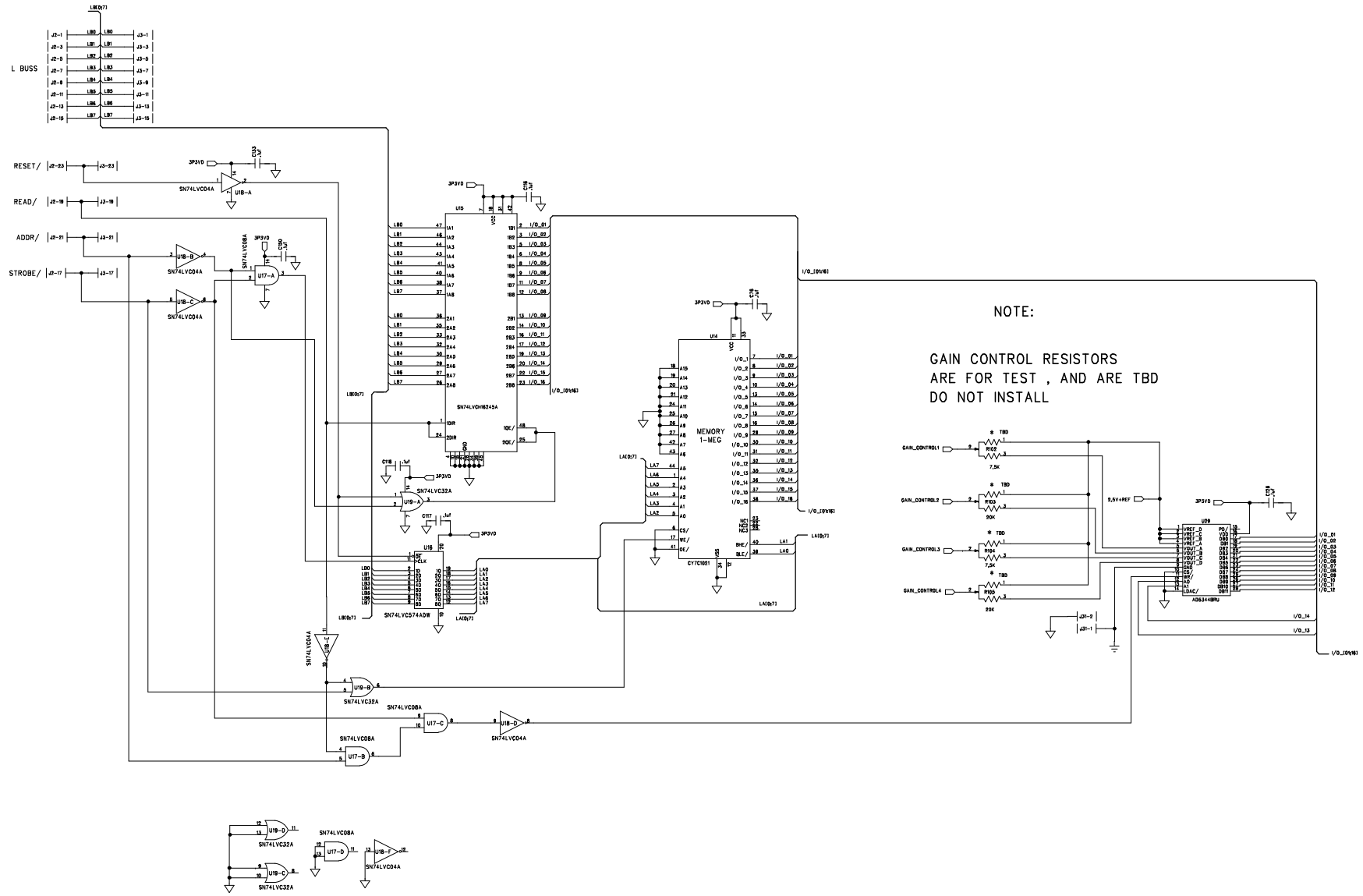
Note : Do not install R267

COMPANY:			
TITLE: BCM ELECTRONICS			
DRAWN: AJDP	DATE: 10/22/01		
CHECKED:	DATE:		
QUALITY CONTROL:	DATE:	CODE:	SIZE: C
RELEASED:	DATE:	DRAWING NO:	REV: C
SCALE:		SHEET: 2 OF 2	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE:

CHOOSE J2 or J3 for best layout



NOTE:

GAIN CONTROL RESISTORS
ARE FOR TEST , AND ARE TBD
DO NOT INSTALL

DRAWN:	DATE:	COMPANY:	
CHECKED:	DATE:	TITLE: BCM ELECTRONICS	
QUALITY CONTROL:	DATE:	CODE: / SIZE: / DRAWING NO: / REV:	
RELEASED:	DATE:	SCALE:	SHEET: 3 OF 3