BNL-105818-2014-TECH

EP&S No. 103;BNL-105818-2014-IR

16-Channel timing card with Q-BUS interface

G. Benenson

July 1983

Collider Accelerator Department

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC)

DISCLAIMER

Accelerator Department
BROOKHAVEN NATIONAL LABORATORY
Associated Universities, Inc.
Upton, New York 11973

EP&S Division Technical Note No. 103

G. Benenson
July 28, 1983

16-CHANNEL TIMING CARD WITH Q-BUS INTERFACE

I. General Description

Real-time monitoring/control systems often require that complex timing sequences be generated under micro-computer control. Standard "Pre-Det" or "Auto-Det" modules are not designed for direct computer interface; standard real-time clock/counter interface cards, such as DEC KWV11-A, are not designed to supply the multiple outputs required for complex control functions. As a result, timing problems are often "solved" through some uneasy combination of cumbersome interfacing; proliferation of modules, crates and cable; and compromise with the original requirements.

A need therefore exists for a multiple-output timing card which can be operated directly under computer control. This note describes such a module, which has been designed and tested for use in the Ionization Profile Monitor (IPM) System in the AGS main ring. The card is fully programmable from any LSI-11 microcomputer, and occupies one quad-height Q-BUS slot. A single 50-conductor flat cable handles all external communications. (See Table III).

II. User's Guide

A. Real-Time Control of Timing Sequences

The Q-BUS timing card is designed to supply 16 independent timing signals to external devices. There is no restriction on the interrelationship of these signals: they may be nonoverlapping, or partially or wholly overlapping. All outputs are normally synchronized to an external clock, which is accepted by the card as an input, via flat cable (Table III). A software "clock" may substitute for the real-time clock; the INCR and MAINT bits in the control/status registers (CSR) are used for this purpose. (See Table II.)

The incoming clock is used to increment the data counter register (DCR), which therefore contains a record of the current "time". THE MAXIMUM CLOCK FREQUENCY IS LIMITED TO 100 KHz; PULSE WIDTH MUST EXCEED 200 ns. The limitation on clock frequency makes possible the following trade-off: ANY REGISTER OR MEMORY LOCATION MAY BE ACCESSED AT ANY TIME; THERE IS NO CONFLICT WITH AN ONGOING TIMING SEQUENCE.

A timing sequence may be triggered in either of two ways, depending on the state of the MODE bit (Table II). In MODE 1, the external RESET line, also a flat cable input (Table III), automatically starts a sequence. In MODE 0, startup is under processor control. Receipt of a RESET causes the CSR ATTN bit to be set, and will also cause an INTERRUPT if the proper INTR ENABLE bits are "on" (Table II). In order to start a sequence, the processor must respond by writing to GO in the CSR. In either mode, the beginning of a sequence is signaled by an internal START pulse, and by reset of the CSR READY bit (Table II).

At the end of a sequence, the READY bit is automatically raised, indicating that the card may once again receive START. An INTERRUPT may be programmed to occur at this time. Should a START occur (via GO or RESET) in the absence of READY, there would be an attempt to begin a new sequence before the previous one had terminated. In this case, an ERROR bit is set in the CSR, and an INTERRUPT may also be enabled (see Table II). Overflow of the data counter is also indicated by ERROR.

B. How Sequences are Programmed

Programming of the timing card is achieved using a 2K x 16 bit on-board memory, with full accessibility to Q-BUS; and by two special purpose registers: The address counter register (ACR) and the word counter register (WCR). The memory is organized into two parts: the lower half stores TIME data, which determines the "time" (i.e., data count) at which output pulses will occur; the upper half contains MASK DATA, which specifies the distribution of output pulses among the sixteen lines. These two pages of memory are geared together: each word in time data memory has its corresponding word at the same 11-bit address in MASK DATA memory. (Table I). Therefore, 1K locations are available for combined time/mask data.

The large amount of available memory makes it possible to segment the memory into a number of discrete programs, each occupying a block of time/mask space. A program is then specified by two numbers: starting address and number of memory words. These two quantities are programmed by writing to the address counter register (ACR) and word counter register (WCR), respectively. Figure 1 shows the relationship between a sample program and the resulting timing sequence. Note that the ACR contains the first WORD address, i.e., the Q-BUS byte address

shifted right one position; and the word count is always expressed in two's complement representation. Both ACR and WCR actually consist of latch-counter/register combinations. At the beginning of a sequence, the counter is loaded from the latch; however, reading from Q-BUS gives the current countents of the counter (hence, the designation "counter/register"). Therefore, the ACR and WCR need not be pre-loaded before each sequence, but only when it is desired to switch to another program in time/mask memory.

From Fig. 1, it is apparent that each bit of mask memory corresponds to an output line. At any particular time, none, any or all the output lines may be activated. An active line will remain high until the "time" changes, i.e., until the next clock edge, unless the same output line is programmed "on" during the very next time data slot. Such is the case in Fig. 1 for output "0" and "7" during "5" and "6" data counts.

Two of the output lines, "0" and "1", may be programmed to produce INTERRUPTS as well as output pulses. The PROGRAM INTERRUPT ENABLE bits in the CSR are used for this purpose (Table II).

> NOTE: All time data words within a program must be in ascending order; otherwise the logic will "hunt" for a "next" data word which has already been passed by the DCR, resulting ultimately in an ERROR flag.

III. Circuit Description

Schematics for the timing card are filed as Drawing DO9-E1497-3, 1, 2 and 3 of 3. These will be referred to as P.1, P.2 and P.3, respectively. The block diagram attached as Fig. 3 indicates the relationship between the three pages. the COMPUTER INTERFACE (P.1) is concerned with driving and receiving Q-BUS, decoding register and memory addresses, and handling data transfer protocols and interrupt transactions. Data and address information are separated and applied to two bi-directional busses, which connect to the register and memory devices shown on P.3. Control logic is shown on P.2.

A. COMPUTER INTERFACE (P.1)

The connection to Q-BUS relies mainly on DEC DCK11 CHIPKIT interface devices.[1] 3A, 4A, 5A and 6A are DC005 bus transceivers, used to drive and receive Q-BUS data, and to detect addresses from the register bank (Table I). Memory bank addresses are detected by the address comparator 6B. Because of address/data multiplexing on Q-BUS, address information must be stored at BSYNCH time; this is done for register and memory addresses at 3C-2 and 1F-5, respectively. These signals are OR'ed

and gated with BSYCNH to form BUS REQUEST, 1C-8, which is an input to control logic, P.2.

The low-order 11 address bits (not including byte address, bit 0) are stored and driven on the ADDRESS BUS by register chips 3C and 5C; these form the local memory address for reading and writing to Q-BUS.

DEC interface chip DC003 (location 2A) handles the interrupt protocol; its inputs are the interrupt request and enable lines from the control section. Data transfer protocol lines BSYNCH, BRPLY, BDIN and BDOUT[2] are buffered by transceiver chip 1A; the DEC protocol chip DC004 was avoided because of its complexity and inflexibility.

B. Memory/Register Section, P.3

The block diagram shown as Fig. 2 contains the elements of the memory/register section. The memory itself is made up of two Mostek MK4802-1 2K x 8 devices, chips 4B and 8B. These devices are configured as a 2K x 16 bit memory, and connected directly to the address and data busses. The two control lines, write enable (WE) and output enable (OE) are inputs from the control logic section, P.2. (OE gates memory data onto the tri-state data bus.).

The entire address counter register (ACR), word counter register (WCR) and their respective latches are contained within 2 Am2940 bit-slice DMA controller chips (Fig. 3).[3] 10-bit addresses are produced by the address counter; the low-order 8-bits are handled by 4D; and the high-order 2 bits, byte 8D. The 6 high-order bits of 8D are not used. The 11th address bit, which selects TIME or MASK DATA page, is produced by the control logic section during real-time sequencing.

4D and 8D are labelled "address controller" on Fig. 2. They are operated in control Mode 3; i.e., both ACR and WCR are incremented together; and word count overflow (WCO) is brought out to indicate completion of a sequence.[3] Control of this device is exercised by a carry (CY) input (used to inhibit counting), three instruction lines I_{2-0}, and an OE line which gates the ACR onto the tri-state address bus.

Another pair of 2940's 4E and 8E, are used to implement the data counter register DCR; the time data register (TDR), used to store the time data word from memory at which the next pulse outputs will occur; and the comparator, which compares the two. These two chips are labelled DATA CONTROLLER on Fig. 2. The 2940 address counter is used as the DCR; the word counter is used as TDR; and the devices are operated in Mode 2, so that the TDR is never incremented, and the comparator output is brought out via the DONE pin.[3] Outputs are therefore COMPARE

(i.e., DONE, or DCR=TDR) and data counter overflow (DCO). Inputs from the control logic section are instruction bits I_{2-0} and CY. The address bus connection is not used.

Note that three of the four bus accesssed registers, WCR, ACR and DCR, are physically located within controller chips. The connection to Q-BUS for both reading and writing is made via the bi-directional data bus; and control during bus operations is exercised via the instruction bits.

Figure 2 shows two other devices attached to the data bus: these are the word generator (WG) 3H and 8H; and the output register (OR) 4H, 5H, 6H and 7H. WG is used to load constants onto the data bus; its operations include clearing the OR and DCR, and loading mode numbers into the control registers of all four controller ships. OE and 2 data bits are supplied by control logic. The output register is loaded from the mask data memory to produce the programmed pulse outputs, and cleared from WG between pulses. The WRITE ENABLE (WE) line is an input from control logic.

C. Control Logic Section, P.2

As the foregoing description suggests, there are two independent sources of control for the memory and controller devices on the timing card. Commands may be asserted by the processor, via Q-BUS; or they may be caused by real-time events entering the timing card as CLOCK and RESET. Existence of two independent sources poses two fundamental problems for the internal control logic. The two pathways must be SYNCHRONIZED (i.e., prevented from conflicting with one another) and MULTIPLEXED (i.e., a choice must be made between them in determining the active source at any particular time).

The two control pathways are shown entering the control logic schematic (P.2) from the left and right, as BUS RQST/WRITE RQST and EXT CLOCK/EXT RESET, respectively. These inputs are synchronized to a common 10 MHz master clock (MCK) which originates from oscillator 7E (P.3). Synchronization of bus and real-time inputs is performed by registers 2D and 10H, respectively. Gates 1D-3 and 10F-6 prevent more than one control pathway from being active during a MCK cycle; and use of the NOR connection at 1E-5 awards priority to the bus pathway in case of a tie.

The major outputs of the control logic section are the inputs to memory/register (P.3) discussed above. Most of these lines are produced by 3 32-bit PROM chips, 9B, 9C and 9D, with output buffer register 10B and 10C. PROM 9B is enabled by the BUS REQUEST pathway; 9C and 9D are enabled by real-time requests via JK flip-flops 10D and 9F. As discussed above, the two enables are mutually exclusive. The PROM chips are open-collector devices with pull-ups supplied by resistor pack 9A.

Unless enabled, all PROM outputs are high; however, control outputs are low-true. Six of the output lines, including memory OE and five controller I lines, may be driven from either the bus or the real-time pathway. These lines are therefore derived from the wire-OR of 9B and 9C, made possible by low-true outputs and mutually exclusive enables.

Table IV shows the program for 9B. The enable pin 9B-15 is derived from 2D-12, the BUS REQUEST line after synchronization of the five address lines. One address bit selects READ or WRITE; another selects memory or register access; and two select the particular register (Q-BUS address bits 2 and 1). The remaining line, DEL, is the ENABLE bit delayed one clock cycle. This bit is used to limit memory WE to one clock cycle in width.

Table V shows the program for PROMS C and D, concerned with real-time control. These PROMS implement the state table shown in Fig. 4. Inputs CLOCK and RESET are synchronized at 10H-15 and 10H10, respectively. The additional delay at 9H-7 and 9H-2 is used to develop a leading edge detector, 6D-8 and 6D-6, which generates a pulse 100 ns wide regardless of the original width of CLOCK and RESET respectively (except that they must exceed 200 ns, minimum). Note that MODE is a condition on RESET; and MAINT is a condition on CLOCK. These bits are brought in from the CSR (see below). Also note that GO may substitute for RESET; and INCR may substitute for CLOCK. These CSR write-only bits, already synchronized to MCK by the bus control pathway, are ORed into the CLOCK and RESET pathways at 6C-6 and 6C-3. The real-time requests are then stored by JK flip-flop 10D as STEP and START respectively. These lines are ORed, delayed one clock cycle to detect a conflict with the bus control pathway, and then used to form the enable bit for PROMS 9C and 9D.

Three of the five address bits for 9C and 9D are "next state" bits which represent an increment of the current state. The control state counter is implemented within 9D itself. The resting state is "7" due to the use of active low logic. Figure 4 shows an outer loop which is selected by START and an inner loop which executes a STEP. The choice is made in the PROMS by address bit 4. The remaining PROM address bit distinguishes betweeen match and non-match conditions within the data controller, i.e., between DCR=TDR and DCR≠TDR. This bit is used to branch within the inner loop. Note that all outputs of the PROM, including "next state" information, are deskewed by 10B and 10C before taking effect. For example, set up of the DCR, which takes place during state "7" (once the ENABLE is present) will produce control bits for the word generator and/or data controller. These bits will be loaded into the register along with the "next state" information. As set-up lines, they will be observed by the memory or register device(s) only on the NEXT edge of MCK. Thus, there is a two cycle delay between the state

information presented to the address port of PROM and the resulting register change of state.

P.2 also includes the CSR. 6F contains the STATUS bits, clocked upon leading edge detection of RESET, 6C-8. The ATTN bit is set simultaneously, provided MODE is low. This transition is set up at 9F-3 and appears at 9F-5 from which point it is gated onto the data bus via 7F-15. Any transition of the READY bit is enabled during state "2". NOTE THAT THE RAISING OF READY AT THE END OF A SEQUENCE REQUIRES ONE ADDITIONAL CLOCK BEYOND THE LAST TIME DATA WORD IN THE PROGRAM. MATCH (i.e., DCR=TDR) and ERROR are likewise clocked during state "2" and these also appear as outputs of 9E.

INTERRUPT, ENABLE, MAINT and MODE bits are stored in 3F and 5F and the INCR and GO bits are brought in via 6E-6 and 6E-12, respectively. READY, ATTN and ERROR interrupt requests are developed by gates 1H and 2C; as are program interrupts which are triggered by pulse outputs 1 and 0, and stored by flip-flop 2H.

References

1. "DCK-11-AA Program Transfer Interface," in Microcomputer Interface Handbook, Pp. 114-133, Digital Equipment Corp., 1980.

2. "LSI-11 Bus," in Microcomputers and Memories, Ch. 9, Digital Equipment Corp., 1982, see especially "Data Transfer Bus Cycles," pp. 223-233.

3. "Am2940," Bipolar microprocessor Logic and Interface Data Book, pp. 6-307--6-315, Advanced Micro Devices, 1981.

Q-BUS TIMING CARD

REGISTER FORMAT

ADDRESS	DESCRIPTION	CONTENT
7{7/6}XXX0	WORD COUNTER REGISTER	MEMORY WORD COUNT (TWO'S COMPLEMENT)
7{7/6}XXX2	ADDR COUNTER REGISTER	MEMORY STARTING ADDRESS
7{7/6}XXX4	CONTROL/STATUS REGISTER	SEE TABLE 2
7{7/6}XXX6	DATA COUNTER REGISTER	CURRENT TIME

MEMORY FORMAT

ADDRESS	DESCRIPTION	CONTENT
XX0000 : XX3777	TIME DATA MEMORY	TIME VALUES AT WHICH OUTPUT PULSES OCCUR (ASCENDING SEQUENCE)
XX4000 : XX7777	MASK DATA MEMORY	OUTPUT PATTERN OF PULSES FOR EACH TIME DATA POINT

SELECT SWITCHES

NOTE: OPEN = 0 ; CLOSED = 1

DEVICE	BIT LOCATION	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REGISTER BANK	ASSIGNMENT	1	1	1	1	1	SWITCH SELECT										*		0
	SWITCH LOC.						8A									7A			
	SWITCH #						8	7	6	5	4	3	2	1	8	7			
MEMORY BANK	ASSIGNMENT	SW. SELECT					**	LOCAL MEMORY ADDR											0
	SWITCH	7B																	
	SWITCH	6	5	4	3	2	1												
INTERRUPT VECTOR	ASSIGNMENT	0	0	0	0	0	0	0	0	0	0	0	SW. SELECT				***		00
	SWITCH												7A						
	SWITCH												6	5	4	3	2	1	

* DEVICE SELECT (SEE REGISTER FORMAT)

** PAGE SELECT (TIME DATA = 0 ; MASK DATA = 1)

*** CHANNEL SELECT (A = 0 ; B = 1)

SP 11037A

TABLE I

Q-BUS TIMING CARD

CONTROL/STATUS REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	ATTN	STATUS			INCR	MAINT	MODE	RDY	INTERRUPT ENABLE						GO
		2	1	0						ERR	RDY	ATTN	PGM B	PGM A	

BIT	NAME		TYPE	DESCRIPTION
0	GO		WRITE	SETS START; REQUIRED TO INITIATE TIMING SEQUENCE IN MODE 0.
1	INTERRUPT ENABLE	PROGRAM A	R/W	ENABLE INTERRUPT CHANNEL A ON PULSE OUT 0
2		PROGRAM B	R/W	" " " B " " OUT 1
3		ATTN	R/W	" " " A " ATTN BIT
4		READY	R/W	" " " B " READY "
5		ERROR	R/W	" " " B " ERROR "
6		MASTER	R/W	MUST BE SET FOR ANY INTERRUPTS TO OCCUR
7	READY		READ	INDICATES TIMING SEQUENCE NOT IN PROGRESS SET BY WORD COUNTER OVERFLOW OR ERROR RESET BY START·READY OR INIT
8	MODE		R/W	SELECT CONDITION FOR START: MODE=0 → USE GO TO START; MODE=1 → AUTO START ON EXT RESET
9	MAINT		R/W	DISABLE EXTERNAL CLOCK; MAINT=1 → INCR BIT MUST BE USED TO STEP DATA CTR
10	INCR		WRITE	SOFTWARE INCREMENT OF DATA COUNTER; USED FOR DIAGNOSTICS.
11	STATUS	0	READ	STATE OF 3 EXTERNAL STATUS LINES, SAMPLED AT EXT. RESET TIME
12		1	READ	
13		2	READ	
14	ATTN		READ	INDICATES EXT RESET RECEIVED IN MODE 0; WAITING FOR GO. SET BY EXT RESET · MODE; RESET BY GO + INIT
15	ERROR		READ	INDICATES FAILURE TO EXIT FROM TIMING SEQUENCE. SET BY DATA COUNTER OVERFLOW OR START · READY. RESET BY START · READY OR INIT

SP 11037A

TABLE II

Q-BUS TIMING CARD

CABLE FORMAT

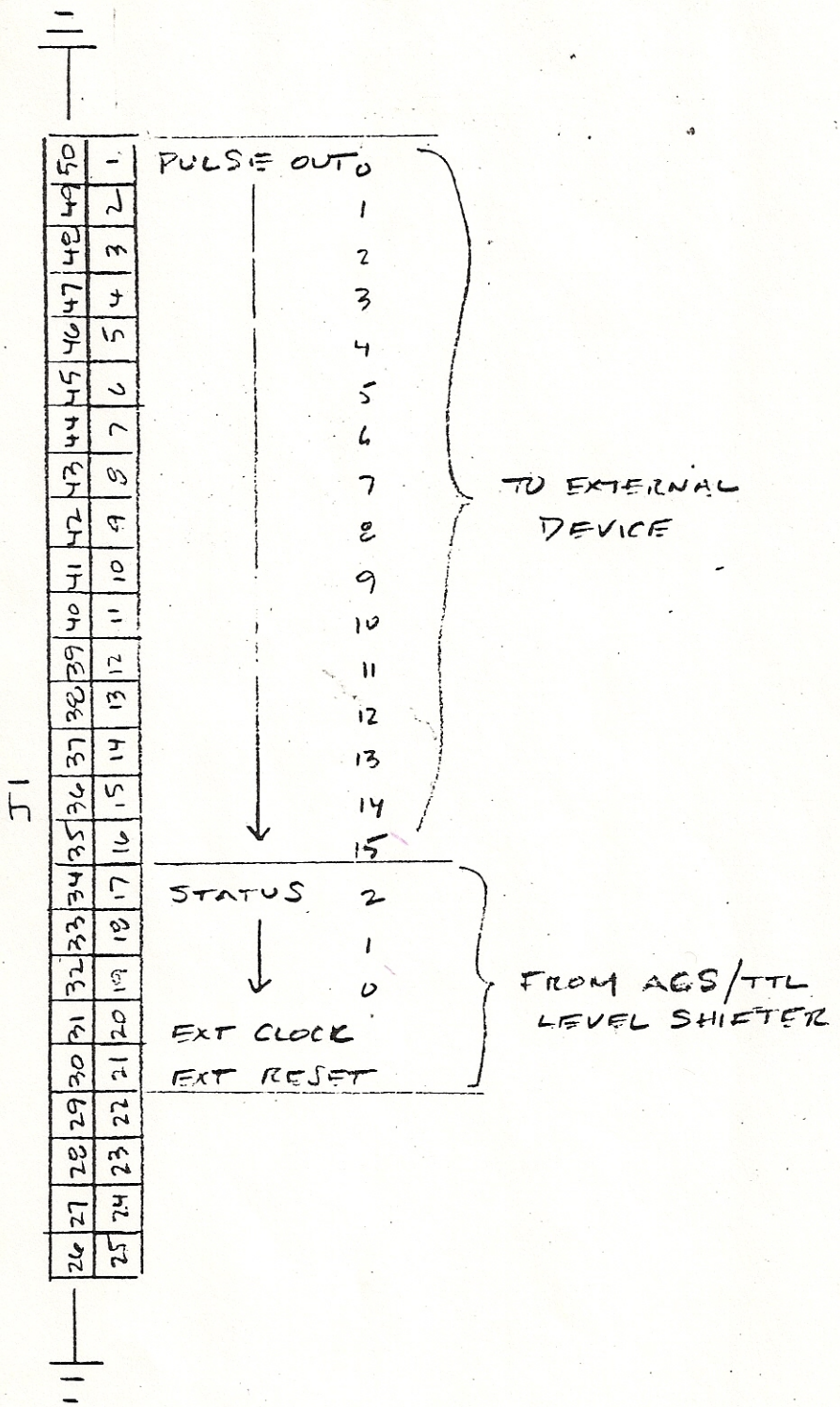


TABLE III

Q-BUS TIMING CARD - BUS CONTROL PROM

PROM-93

		R/W A4	DAL A3	MEM/REG A2	ADR2 A1	ADR1 A0	HEX ADDR.	HEX DATA	MEM OE O8	ADDR CTL I2 O7	ADDR CTL I1 O6	ADDR CTL I0 O5	DATA CTL I2 O4	DATA CTL I1 O3	CSR OE O2	CSR WE O1
READ WCR	0	0	0	0	0	0	00	AF	1	0	1	0	1	1	1	1
↓ ACR	1	0	0	0	0	1	01	BF	1	0	1	1	1	1	1	1
CSR	2	0	0	0	1	0	02	FD	1	1	1	1	1	1	0	1
DC	3	0	0	0	1	1	03	F7	1	1	1	1	0	1	1	1
	4	0	0	1	0	0	04	7F	0	1	1	1	1	1	1	1
READ MEM	5	0	0	1	0	1	05	7F	0	1	1	1	1	1	1	1
	6	0	0	1	1	0	06	7F	0	1	1	1	1	1	1	1
	7	0	0	1	1	1	07	7F	0	1	1	1	1	1	1	1
READ WCR	8	0	1	0	0	0	08	AF	1	0	1	0	1	1	1	1
↓ ACR	9	0	1	0	0	1	09	BF	1	0	1	1	1	1	1	1
CSR	10	0	1	0	1	0	0A	FD	1	1	1	1	1	1	0	1
DC	11	0	1	0	1	1	0B	F7	1	1	1	1	0	1	1	1
	12	0	1	1	0	0	0C	7F	0	1	1	1	1	1	1	1
READ MEM	13	0	1	1	0	1	0D	7F	0	1	1	1	1	1	1	1
	14	0	1	1	1	0	0E	7F	0	1	1	1	1	1	1	1
	15	0	1	1	1	1	0F	7F	0	1	1	1	1	1	1	1
WRITE WCR	16	1	0	0	0	0	10	EF	1	1	1	0	1	1	1	1
↓ ACR	17	1	0	0	0	1	11	DF	1	1	0	1	1	1	1	1
CSR	18	1	0	0	1	0	12	FE	1	1	1	1	1	1	1	0
DC	19	1	0	0	1	1	13	FB	1	1	1	1	1	0	1	1
	20	1	0	1	0	0	14	FF	1	1	1	1	1	1	1	1
WRITE MEM	21	1	0	1	0	1	15	FF								
	22	1	0	1	1	0	16	FF								
	23	1	0	1	1	1	17	FF								
	24	1	1	0	0	0	18	FF								
	25	1	1	0	0	1	19	FF								
	26	1	1	0	1	0	1A	FF								
NO-OP	27	1	1	0	1	1	1B	FF								
	28	1	1	1	0	0	1C	FF								
	29	1	1	1	0	1	1D	FF								
	30	1	1	1	1	0	1E	FF								
	31	1	1	1	1	1	1F	FF								

TABLE IV

Q-BUS TIMING CARD - REAL-TIME CONTROL PROM

OPERATION	START STATE 3	STATE 2	STATE 1	STATE 0	MATCH	HEX ADDR	PROM 9C HEX DATA	MEM OE	ADDR CTR I_2	ADDR CTR I_1	ADDR CTR I_0	DATA CTR I_2	DATA CTR I_1	WORD GEN I_1	WORD GEN I_0	PROM 9D HEX DATA	ADDR CTR MSB	ADDR CTR $\overline{CY}$	DATA CTR I_0	DATA CTR $\overline{CY}$	WORD GEN $\overline{OE}$	MEAT 2	MEAT 1	STATE 0
	A_4	A_3	A_2	A_1	A_0	ADDR	DATA	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	DATA	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
'0'→'1'	0	0	0	0	0	00	FE	1	1	1	1	1	1	1	1	F9	1	1	1	1	1	0	0	1
	0	0	0	0	1	01	FE	1	1	1	1	1	1	1	1	F9	1	1	1	1	1	0	0	1
'1'→'2'	0	0	0	1	0	02	FF	1	1	1	1	1	1	1	1	FA	1	1	1	1	1	0	1	0
	0	0	0	1	1	03	FF	1	1	1	1	1	1	1	1	FA	1	1	1	1	1	0	1	0
'2'→'3'	0	0	1	0	0	04	FE	1	1	1	1	1	1	1	1	FB	1	1	1	1	1	0	1	1
	0	0	1	0	1	05	FE	1	1	1	1	1	1	1	1	FB	1	1	1	1	1	0	1	1
'3'→'4' 0→OR	0	0	1	1	0	06	FC	1	1	1	1	1	1	0	0	F4	1	1	1	1	0	1	0	0
'3'→'4' MEM→OR; INCR MC INCR AC	0	0	1	1	1	07	7F	0	1	1	1	1	1	1	1	BC	1	0	1	1	1	1	0	0
'4'→'5'	0	1	0	0	0	08	FF	1	1	1	1	1	1	1	1	FD	1	1	1	1	1	1	0	1
'4'→'5' MEM OE; MSB=0	0	1	0	0	1	09	7F	0	1	1	1	1	1	1	1	7D	0	1	1	1	1	1	0	1
'5'→'6'	0	1	0	1	0	0A	FF	1	1	1	1	1	1	1	1	FE	1	1	1	1	1	1	1	0
'5'→'6' MEM→TDR.	0	1	0	1	1	0B	7F	0	1	1	1	1	1	1	1	5E	0	1	0	1	1	1	1	0
'6'→'7'	0	1	1	0	0	0C	FF	1	1	1	1	1	1	1	1	FF	1	1	1	1	1	1	1	1
	0	1	1	0	1	0D	FF	1	1	1	1	1	1	1	1	FF	1	1	1	1	1	1	1	1
'7'→'0' INCR DC	0	1	1	1	0	0E	FF	1	1	1	1	1	1	1	1	E8	1	1	1	0	1	0	0	0
	0	1	1	1	1	0F	FF	1	1	1	1	1	1	1	1	E8	1	1	1	0	1	0	0	0
'0'→'1' 2→DCR	1	0	0	0	0	10	F2	1	1	1	1	0	0	1	0	D1	1	1	0	1	0	0	0	1
	1	0	0	0	1	11	F2	1	1	1	1	0	0	1	0	D1	1	1	0	1	0	0	0	1
'1'→'2' 3→ACR	1	0	0	1	0	12	8F	1	0	0	0	1	1	1	1	F2	1	1	1	1	0	0	1	0
	1	0	0	1	1	13	8F	1	0	0	0	1	1	1	1	F2	1	1	1	1	0	0	1	0
'2'→'3' REIN AC	1	0	1	0	0	14	CF	1	1	0	0	1	1	1	1	FB	1	1	1	1	1	0	1	1
	1	0	1	0	1	15	CF	1	1	0	0	1	1	1	1	FB	1	1	1	1	1	0	1	1
'3'→'4' 0→OR MSB=0	1	0	1	1	0	16	FC	1	1	1	1	1	1	0	0	74	0	1	1	1	0	1	0	0
	1	0	1	1	1	17	FC	1	1	1	1	1	1	0	0	74	0	1	1	1	0	1	0	0
'4'→'5' MEM OE MSB=0	1	1	0	0	0	18	7F	0	1	1	1	1	1	1	1	7D	0	1	1	1	1	1	0	1
	1	1	0	0	1	19	7F	0	1	1	1	1	1	1	1	7D	0	1	1	1	1	1	0	1
'5'→'6' MEM OE MSB=0 MEM→TDR	1	1	0	1	0	1A	7F	0	1	1	1	1	1	1	1	5E	0	1	0	1	1	1	1	0
	1	1	0	1	1	1B	7F	0	1	1	1	1	1	1	1	5E	0	1	0	1	1	1	1	0
'6'→'7'	1	1	1	0	0	1C	FF	1	1	1	1	1	1	1	1	FF	1	1	1	1	1	1	1	1
	1	1	1	0	1	1D	FF	1	1	1	1	1	1	1	1	FF	1	1	1	1	1	1	1	1
'7'→'0' 0→DC	1	1	1	1	0	1E	F8	1	1	1	1	1	0	0	0	F0	1	1	1	1	0	0	0	0
	1	1	1	1	1	1F	F8	1	1	1	1	1	0	0	0	F0	1	1	1	1	0	0	0	0

TABLE V

Q-BUS TIMING CARD - SAMPLE PROGRAM

MEMORY

ADDRESS (OCTAL)	TIME DATA (OCTAL)	ADDR (OCTAL)	MASK DATA (BINARY) 15 8 7 6 5 4 3 2 1 0
XX2742	3	XX6742	0 1 1 0 0 0 0 1
XX2744	5	XX6744	1 0 0 0 1 0 1 1
XX2746	6	XX6746	1 1 0 0 0 0 0 1
XX2750	11	XX6750	0 0 1 1 1 0 0 1

WORD COUNTER REGISTER: 177774 = -4 (OCTAL)

ADDR CTR REGISTER: 001361 = STARTING ADDR ÷ 2 (OCTAL)

RESULTING SEQUENCE

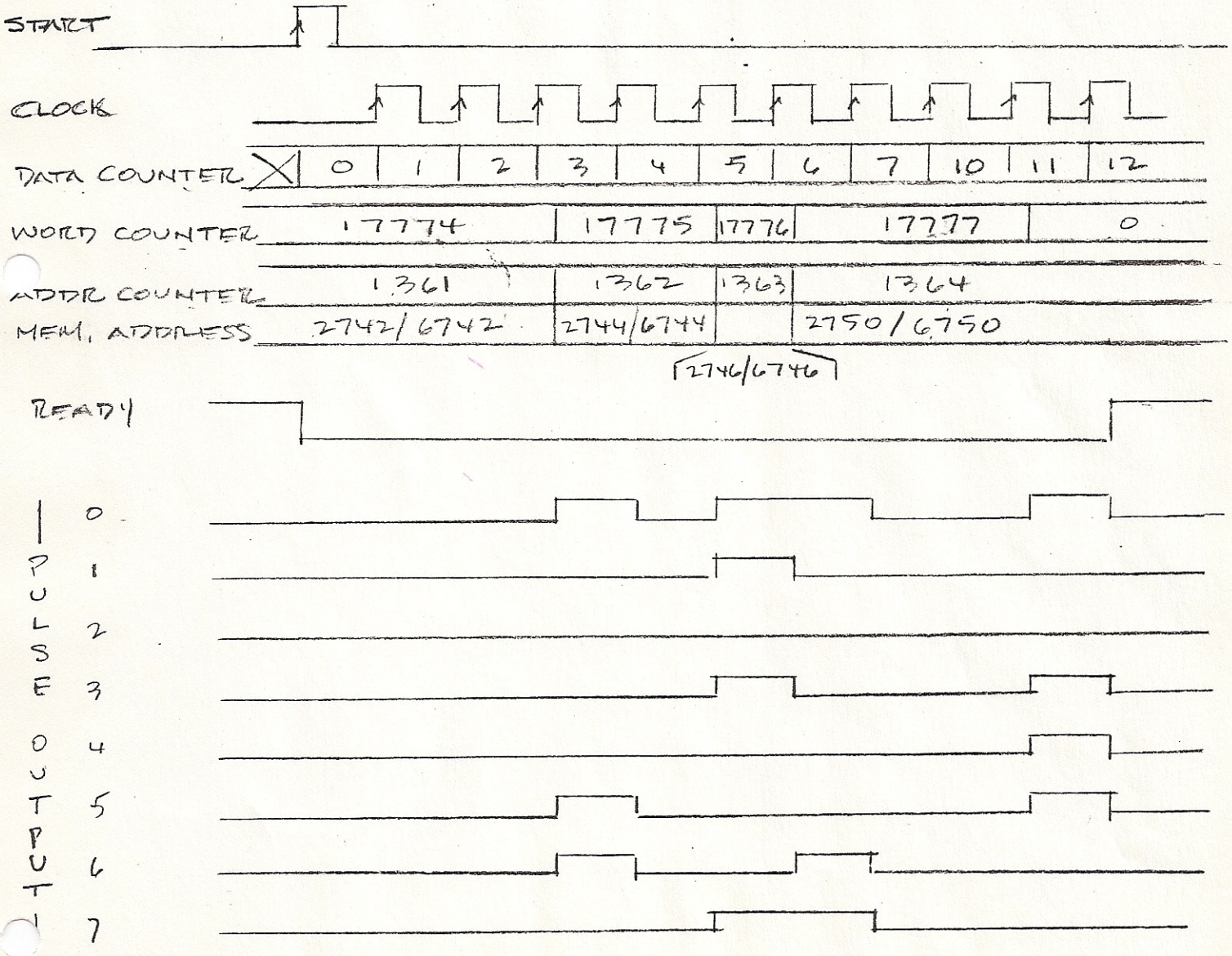
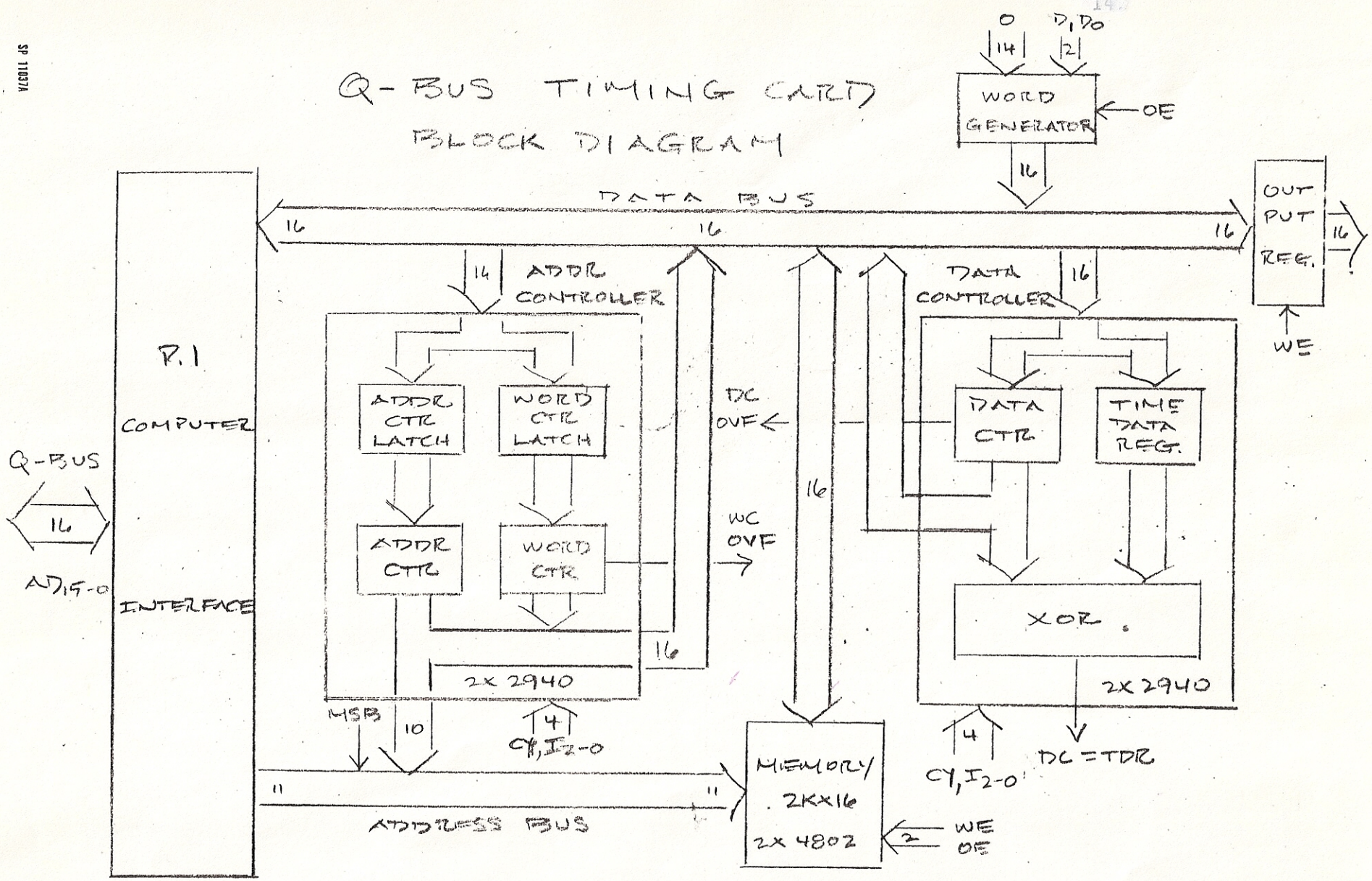


FIGURE 1

SP 11037A

Q-BUS TIMING CARD

BLOCK DIAGRAM



NOTES: 1. LABELLED ARROWS ARE CONTROL LINES FROM OR TO CONTROL LOGIC SECTION, P.2

2. EXCEPT FOR BUS INTERFACE (P.1) BLOCKS SHOWN ON THIS DIAGRAM ARE FOUND ON P.3

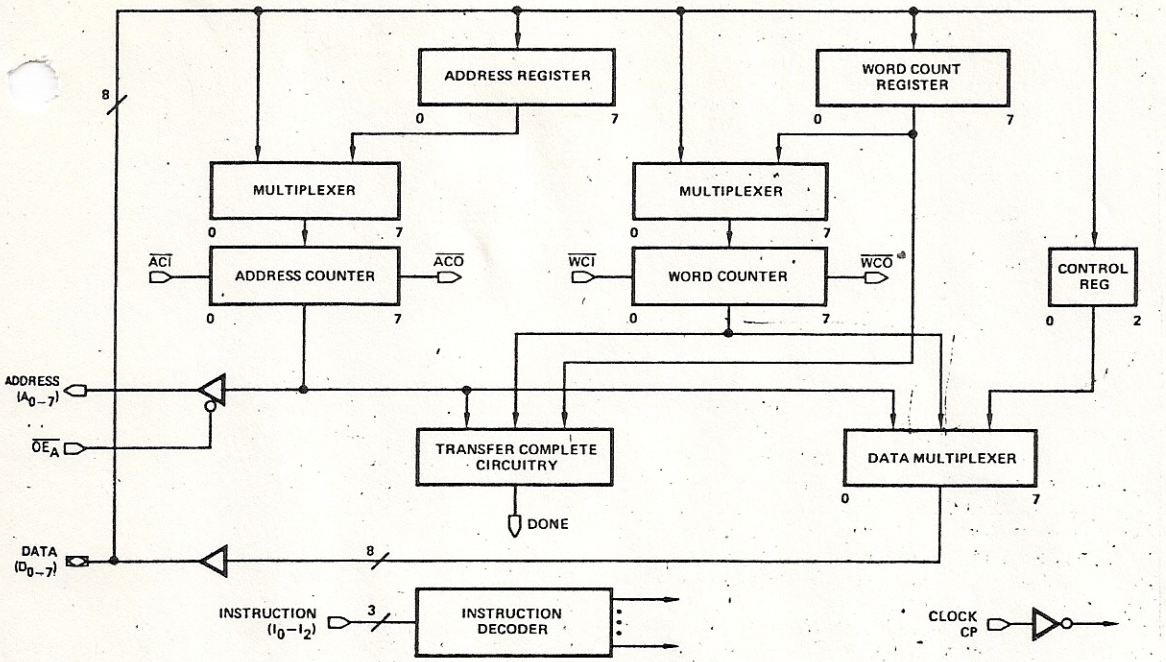
FIGURE 2

Am 2940

DMA

CONTROLLER

BLOCK DIAGRAM



Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

TABLE I. Am2940 INSTRUCTIONS

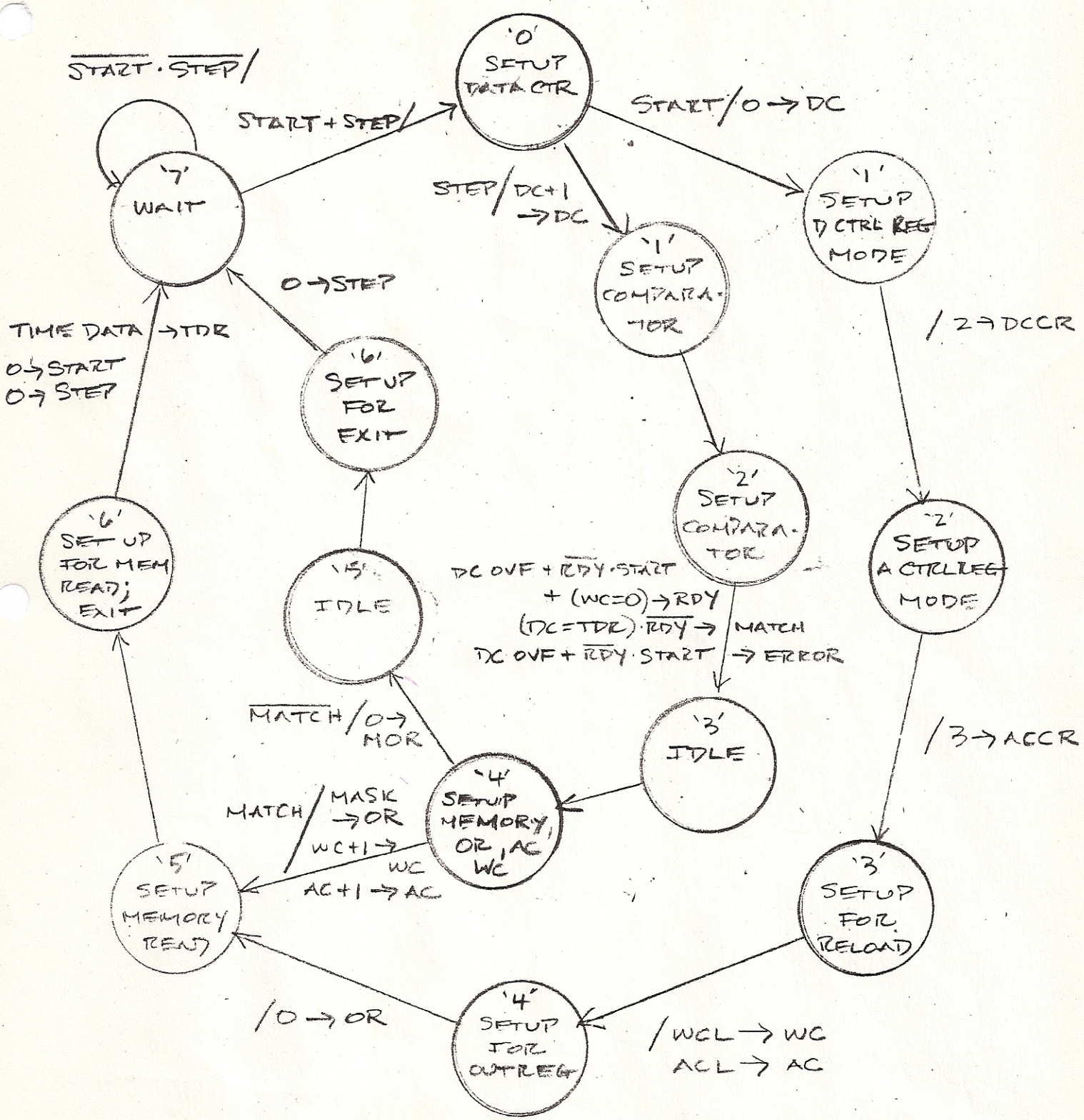
I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

Fig. 3

Q-BUS TIMING CARD - State Diagram



NOTE: CURRENT STATE INFORMATION IS TAKEN FROM PROM BUFFER REGISTER OUTPUT.

Fig. 4