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Pulsed operation of experimental magnet power supplies

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PULSED OPERATION OF EXPERIMENTAL MAGNET POWER SUPPLIES

I. INTRODUCTION

The magnetic fields in AGS experimental magnets utilized to transport the beams to the various targets are produced by direct currents. Since the magnetic fields are required only during beam spills, several advantages result if the magnets could be operated at low current values during the non-beam spill periods of the operating cycle. The first is that overall power consumption is reduced and the second, unnecessary magnet coil heating is also reduced. We therefore felt that it would be prudent to have a scheme for pulsed operation of the large AGS Experimental magnet power supplies (EMPS). In addition, it was felt that if the scheme consisted of a relatively simple modification to existing circuitry, vis-a-vis a completely new system design, it would have attractive advantages from both cost and ease of operation points of view.

II. GENERAL DESCRIPTION

There are several factors that make pulsed operation of beam transport elements difficult at the AGS. The first is that the AGS is a relatively rapid cycling accelerator with repetition times of 1.2 to 3.0 seconds between pulses and maximum flat top pulse lengths of 1.2 seconds. The second is that many of the beam transport magnets were designed for dc operation and typically have time constants up to 2.5 seconds and solid cores. Nevertheless, we have a large quantity of quadrupole and other laminated magnets, with time constants of the order of 0.5 seconds or less, to make the exercise worthwhile.

As an example, the power utilized in the quadrupoles of the C1/C3 line of the SEB is approximately 1.8 MW. If we could realize a 40 per cent duty factor on pulsing the quads, at the present BNL rates for power consumption, we would save approximately $7K/week of running.

The proposed scheme for pulsed operation of the EMPS requires an additional p.c. card and two timing triggers (T_o and T_{invert}). The operation cycle now consists of three phases: the hard turn-on referred to as the RAMP mode, the normal operating mode referred to as the REGULATION mode, and the LOW LEVEL mode for energy saving. The control between the various modes is accomplished via solid state switches (FET's). Figure 1 shows the typical AGS cycle used for SEB and defines some of the parameters of the EMPS pulsed operation relative to the AGS cycle.

III. CIRCUIT DESCRIPTION AND CONSTRUCTION

The existing EMPS output control and regulation system consists of a stabilized current feedback amplifier unit (IC amp) which has a high dc gain and very long time constants, and a voltage feedback amplifier unit (VC amp) which has a lower gain and a wider bandwidth, and hence a faster response time.

In the pulsed type system, since the existing amplifiers work very well for dc operation, we have adopted the philosophy that we should not eliminate these units and replace them with other systems which would be similar yet costly, but to perform some simple modifications to enable us to pulse and also to be able to return to the original amplifiers when we require the regulation. In order to be able to accomplish this during the pulsed mode, the IC amp, because of its long time constants, must be held at its quiescent operating value during the LOW-LEVEL and RAMP modes of the cycle, to assure a minimum recovery time to the REGULATION mode. In other words, we are attempting (by keeping its input constant) to fool the IC amp into "thinking" that it is always operating in the closed loop regulating mode. Meanwhile, we are pulsing the EMPS output via the faster acting VC amp to give us the fast response to the new operating level.

A brief but somewhat detailed description of the pulsing system will now be given in the following paragraphs. Reference is made to Fig. 2 which shows a simplified schematic/block diagram of the system. In addition, the timing control of the FET switches which is shown in Fig. 3 will aid further in the explanation of the operation.

The input amplifiers (A) and (G) + (H) (Fig. 2) normalize the EMPS shunt and DATACON D/A converter outputs to 5 V max. The output amplifiers (E) and (F) normalize the output levels to 100 mV max. and are connected to the IC amp of the EMPS and the DATACON A/D converter respectively. The amplifiers (B) and (C) serve as unit gain, 2 pole, Butterworth filters. The sample and hold (S&H) amplifiers (D) and (N) hold the quiescent current values of the IC amp unit and the A/D converter constant during the RAMP and LOW LEVEL phases.

Amplifier (I) compares the shunt output with the D/A converter value during the RAMP, and produces the primary trigger to go to the REGULATION mode.

Two monostable multivibrators (R) and (S), together with the latches (K) and a D type flip-flop (T), take care of the internal timing, and quad operational amplifier drivers (L) operate the FET switches (1) through (6).

The sequence of operation starts with a T_o trigger (which is readily available in the experimental area), plus an adjustable time delay (RAMP DELAY), at which time, T_{on} , the RAMP starts. The FET's (3) and (5) are closed and apply the driving voltage to the VC amp unit. The shunt signal of the rising current is fed through amplifier (A) and filters (B),(C) into the comparator (I), which switches the EMPS operation to the REGULATION mode when crossover with the computer reference setpoint value occurs (T_1). At that time, FET's (2),(3) and (5) open, and (1) and (6) close, thus putting the EMPS into closed loop operation via shunt amplifier (A), through FET (1) and

amplifer (E) to the IC amp unit, back through amplifier (P) and FET (6) into the VC amp unit, which drives the SCRs or the mag-amps of the EMPS. The sample and hold (S/H) amplifiers (D) and (N) are in the sampling mode. The output from the S/H (N) to amplifier (E) at this time is zero. At T_{inv} (the second trigger which must be supplied), FET's (1) and (6) open, and (4) and (5) close, and feed the LOW LEVEL signal to the VC amp unit causing the EMPS current to fall. The S/H amplifiers (D) and (N) are now in the hold mode. FET (2) is closed, thus the input to the IC amp unit remains at its previous value, which is also fed to the computer ADC converter for readback purposes. The S/H (N) is holding the previous value of the output of the IC amp unit and any deviation of this value results in negative feedback correction through amplifier (E). In this way, the IC amp unit remains at its quiescent state with very small deviations until the circuit returns to the REGULATION mode again.

The timing (see Fig. 1 & 3) of the S/H amp (D) incorporates a settling time delay of 500 milliseconds (T_1 to T_2). The minimum acquisition time (T_2 to T_3) is 50 milliseconds, but does extend until T_{inv} occurs. Should T_{inv} arrive prior to completion of the minimum acquisition time, then T_L (the start of the LOW LEVEL mode) is delayed.

For more details, reference should be made to the actual schematic diagram Dwg. EAO-DE0462-4 and to the detailed calibration and setup procedures which are given in Appendix I.

IV. TESTING AND RESULTS

A prototype wire wrap version of the pulsing circuit was constructed and tested on several EMPS systems, both mag-amp controlled and SCR controlled. The pulsing circuit after proper interfacing to the EMPS and to the computer

system, and paying very careful attention to circuit commons and grounds, performed satisfactorily in all cases. Connection of the pulsing card to the EMPS is simple, encompassing 10 low level connections to the EMPS flap door terminal strip. Figure 4 shows typical connections. For the different EMPS configurations, see Dwg. EAO-DE0463-4. Adjustments and setup take somewhat longer than this and depend on operating values, magnet time constant, power supply voltage and other parameters. The use of a scope is required. In addition, the potentiometers, P2 (comparator), P3 (ramp drive) and P4 (level compensation), as shown in Fig. 2, have to be adjusted interactively to give the best results over the entire operating range. Figure 5a shows oscilloscope photographs of the output current with the system operating on P.S. 418 at various operating currents. Figures 5b and 5c show the same waveforms at faster sweep speeds. Figure 5d shows the ac noise pickup of 1.5% on a signal of 3.31 volts (which corresponds to a current of 2650 amps) at the output of amplifier (A).

Figures 6a, b and c show the traces of the pulsed current superimposed on the steady state current at 1175, 2650 and 3525 amps respectively. Figure 6d shows the response time to recover for a current level change of 1775 amps to 3305. The EMPS required at least 3 cycles before it stabilized at the new value.

The digital readout of the flattop current shows typical short term variations of $\pm$ 0.2 per cent at load currents from 1800 to 3500 amps. Long term drift was not measured. Readings repeated after 30 minutes showed no discernible drift.

The performance of the circuit is influenced by the time constant of the magnet, the type of low level amplifier, the type of EMPS, and the ambient environment. For these reasons, it would be desirable to operate several units simultaneously to evaluate the long term operation of this save-a-watt pulsing circuit and to observe other interacting problems which may arise with the rest of the equipment on the AGS experimental floor.

APPENDIX I

Calibrations and Adjustments

There are 5 externally adjustable dial type potentiometers:

P1 - determines the ramp delay interval, which is subject to the machine cycle. The maximum delay is 500 ms.

P2 - is the fine adjustment of the comparator (I) level. (Start with the pot. at midscale).

P3 - Ramp drive signal (increase pot. from zero).

P4 - Level compensation of ramp. It adjusts the gain of amplifier (Q) and serves to compensate the non-linear characteristic of the ramp at different levels. (Start with pot. at midscale. Fine tuning between P3 and P4 is required.)

P5 - Low level signal during low level mode. (Increase pot. from zero.)

All the above potentiometers have to be set with the circuit connected to the operational EMPS. The use of a scope is required. In addition, there are bench adjustments of trim potentiometers (R1 thru R6) of the circuit required before hookup to the EMPS. Note that all 6 trim pot. adjustments are to be made in the sampling mode.

Set R1 (offset) of the sample and hold amplifer (D) so that the voltage at TP14 equals the one at TP15. Also note that TP13 must be shorted to (TP 9) ground for all adjustments R1 through R4.

Set R2 (offset) on ampl. (E) with TP1 and TP2 shorted so that the output voltage at TP5 reads zero.

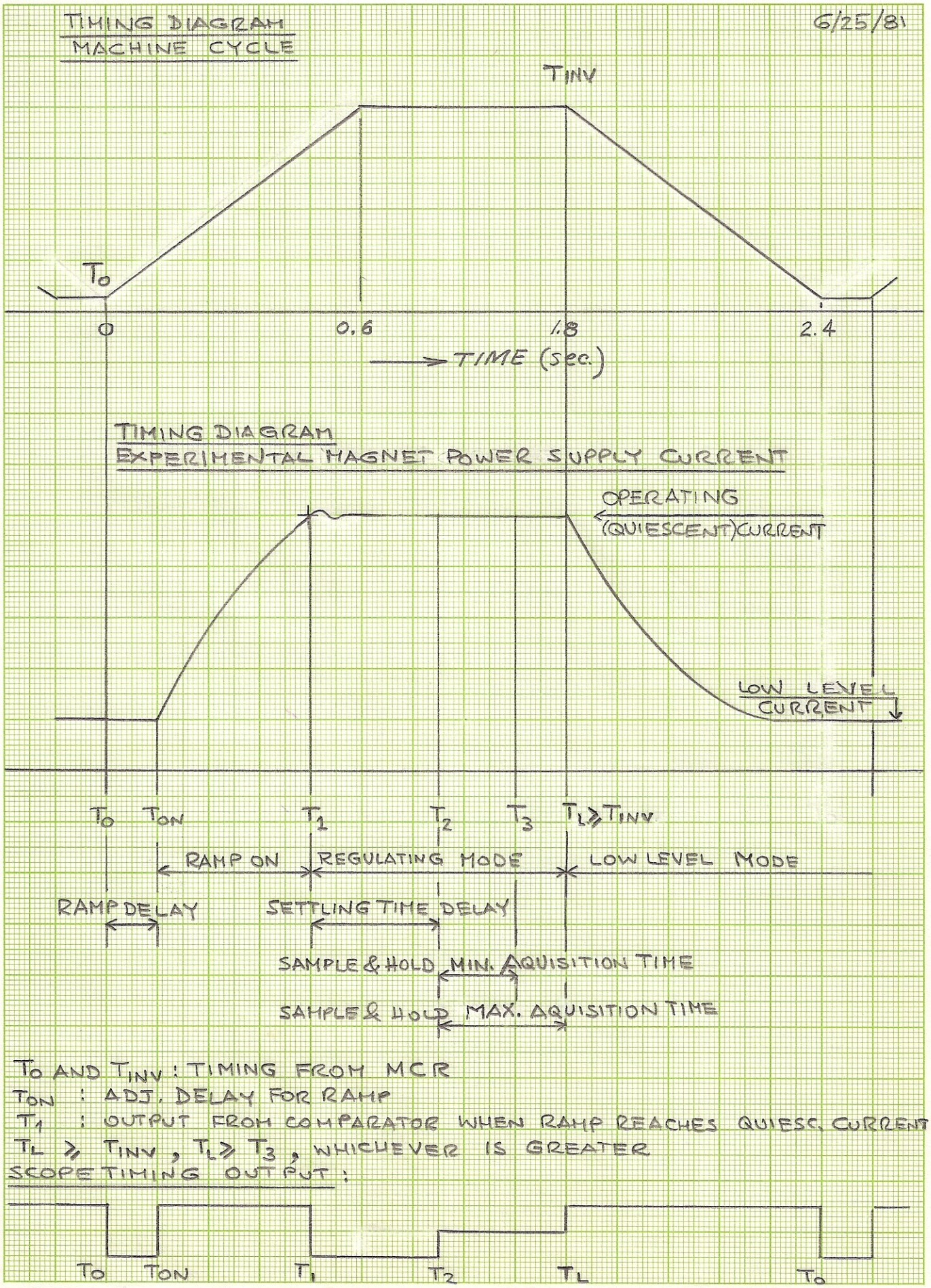
Set R3 (gain) on ampl. (E) with -100 mV applied between TP1 and TP2 until output at TP5 equals -100 mV.

Set R4 (offset) on ampl. (F) so that the input TP15 equals output TP6.

Set R5 (offset) on the sample and hold amplifier (N) with TP7 grounded so that TP13 reads zero.

Set R6 (gain) on sample and hold amplifier (N) with 5 V applied TP7 so that TP13 reads zero again.

FIGURE 1



T_O AND T_{INV} : TIMING FROM MCR
T_{ON} : ADJ. DELAY FOR RAMP
T_1 : OUTPUT FROM COMPARATOR WHEN RAMP REACHES QUIESC. CURRENT
$T_L \geq T_{INV}$, $T_L \geq T_3$, WHICHEVER IS GREATER

SCOPE TIMING OUTPUT :

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FIG. 2

BY HULLIGER DATE 12/1/81

CHKD. BY _____ DATE _____

SUBJECT BLOCK DIAGRAM OF PULSING CIRCUIT FOR EMPS

DEPT. OR PROJECT _____

SHEET No. _____ OF _____

JOB No. _____

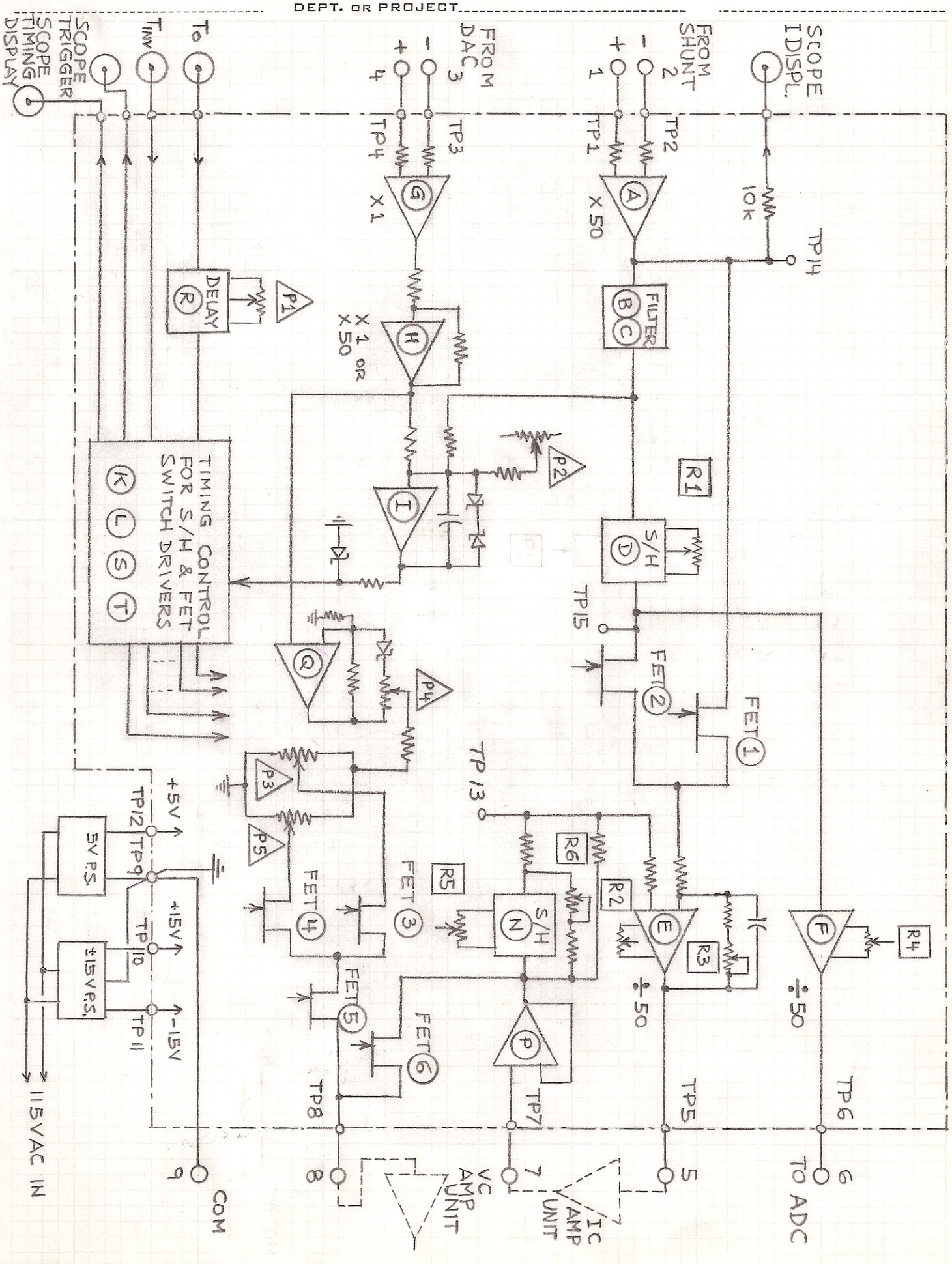
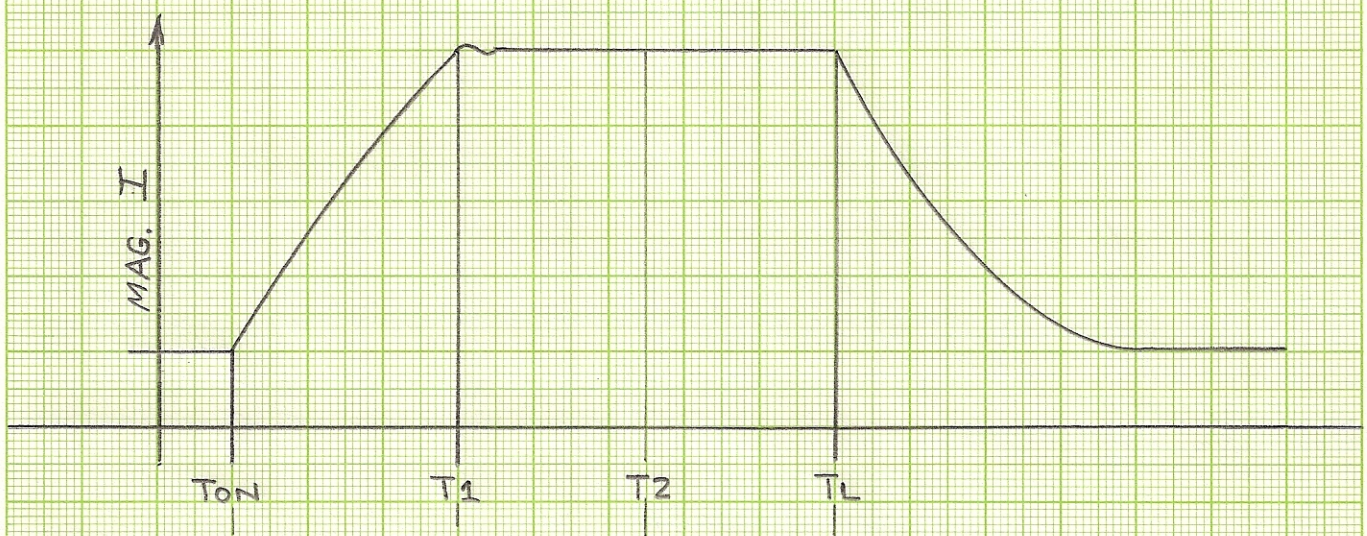
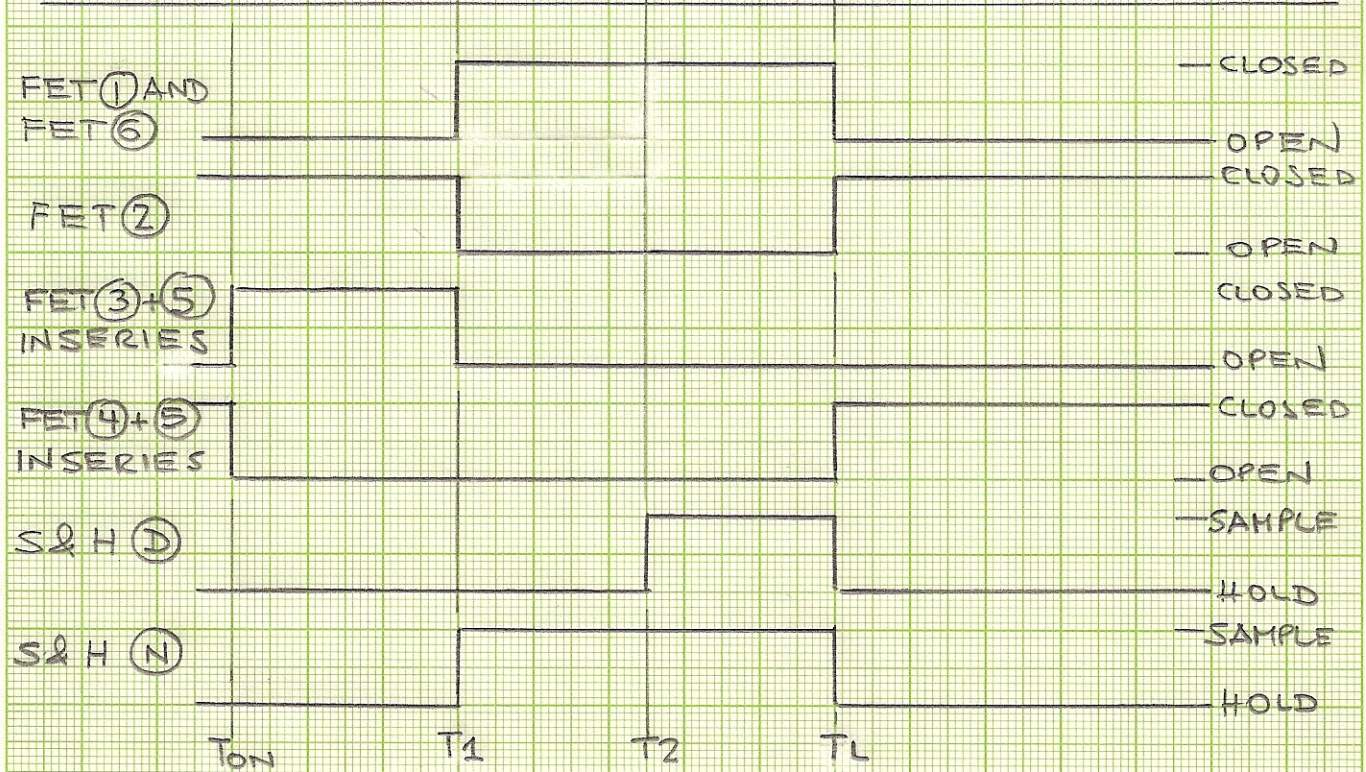


FIGURE 3

TIMING DIAGRAM OF
EXPERIMENTAL MAGNET POWER SUPPLY CURRENT



TIMING DIAGRAM OF FET SWITCHES AND SAMPLE-AND-HOLD AMPLIFIERS



6/25/81

BROOKHAVEN NATIONAL LABORATORY FIG. 4

BY HULLIGER DATE 12/1/81 SUBJECT CONNECTION DIAGRAM FOR SHEET No. ____ OF ____

CHKD. BY ____ DATE ____ PULSING CIRCUIT TO THE EMPS JOB No. ____

DEPT. OR PROJECT ____

SHUNT GROUND ON POSITIVE SIDE (FOR OTHER CONFIGURATIONS SEE DWG. BAO-DE 0463-4

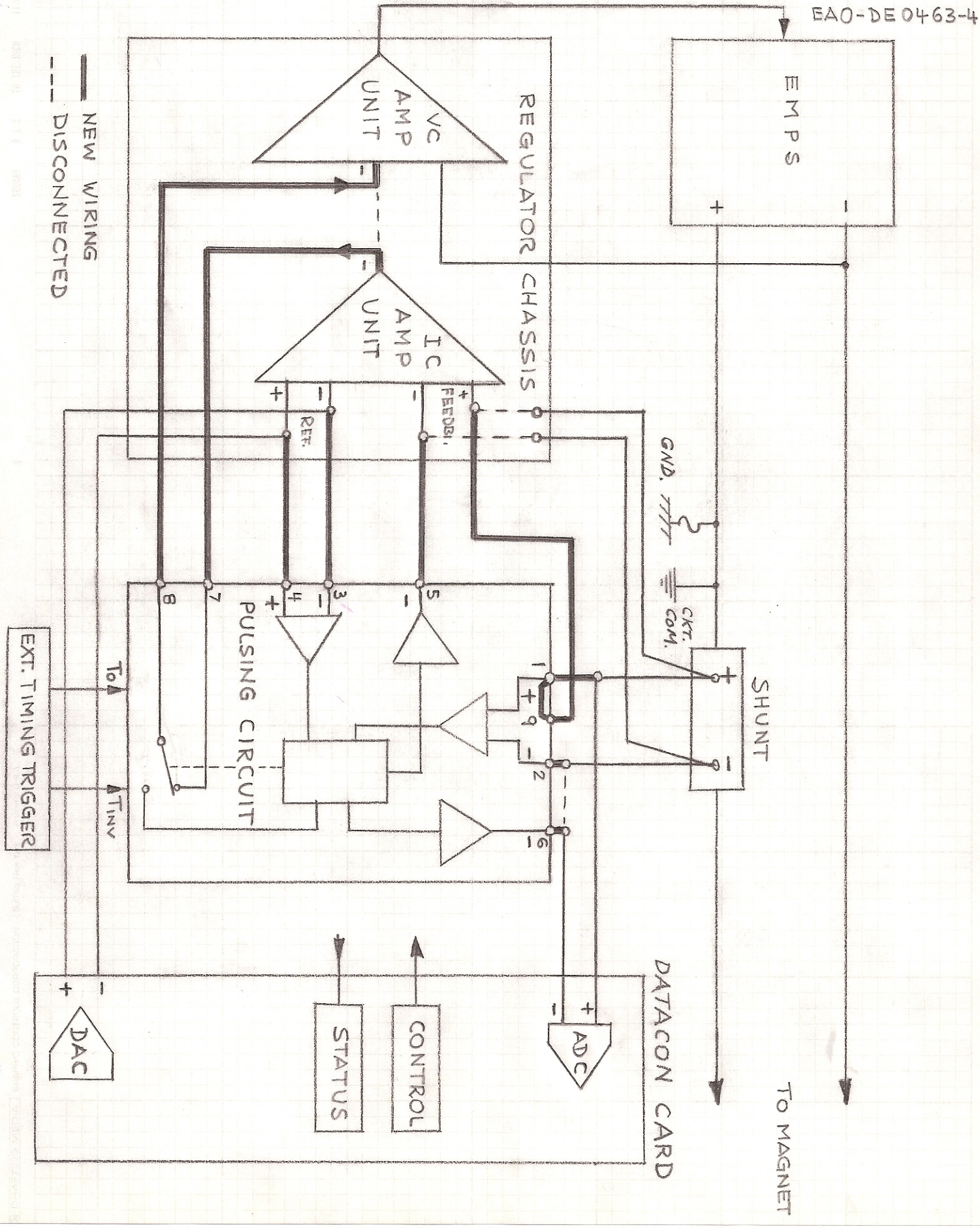


Figure 5

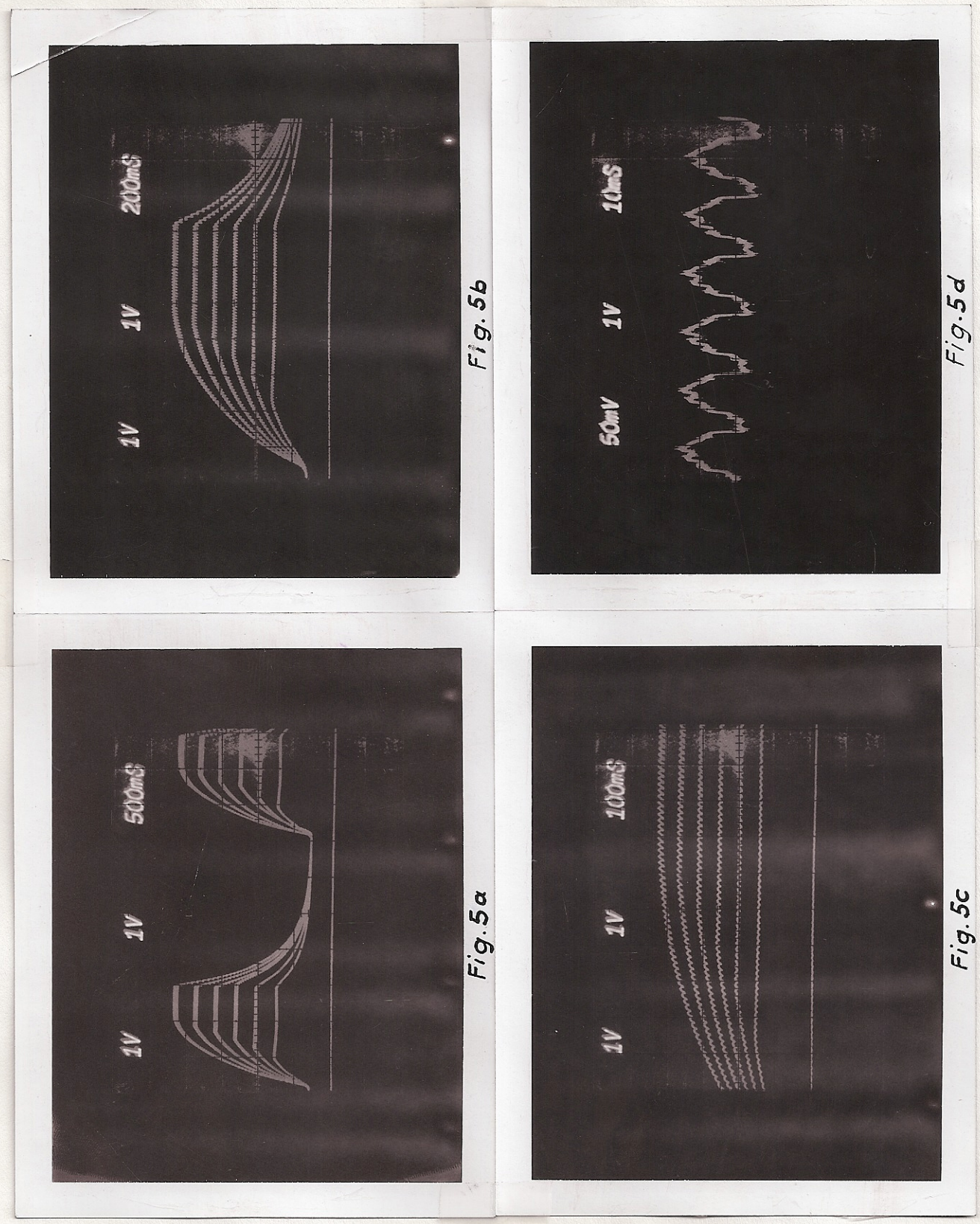


Fig.5a

Fig.5b

Fig.5c

Fig.5d

Figure 6

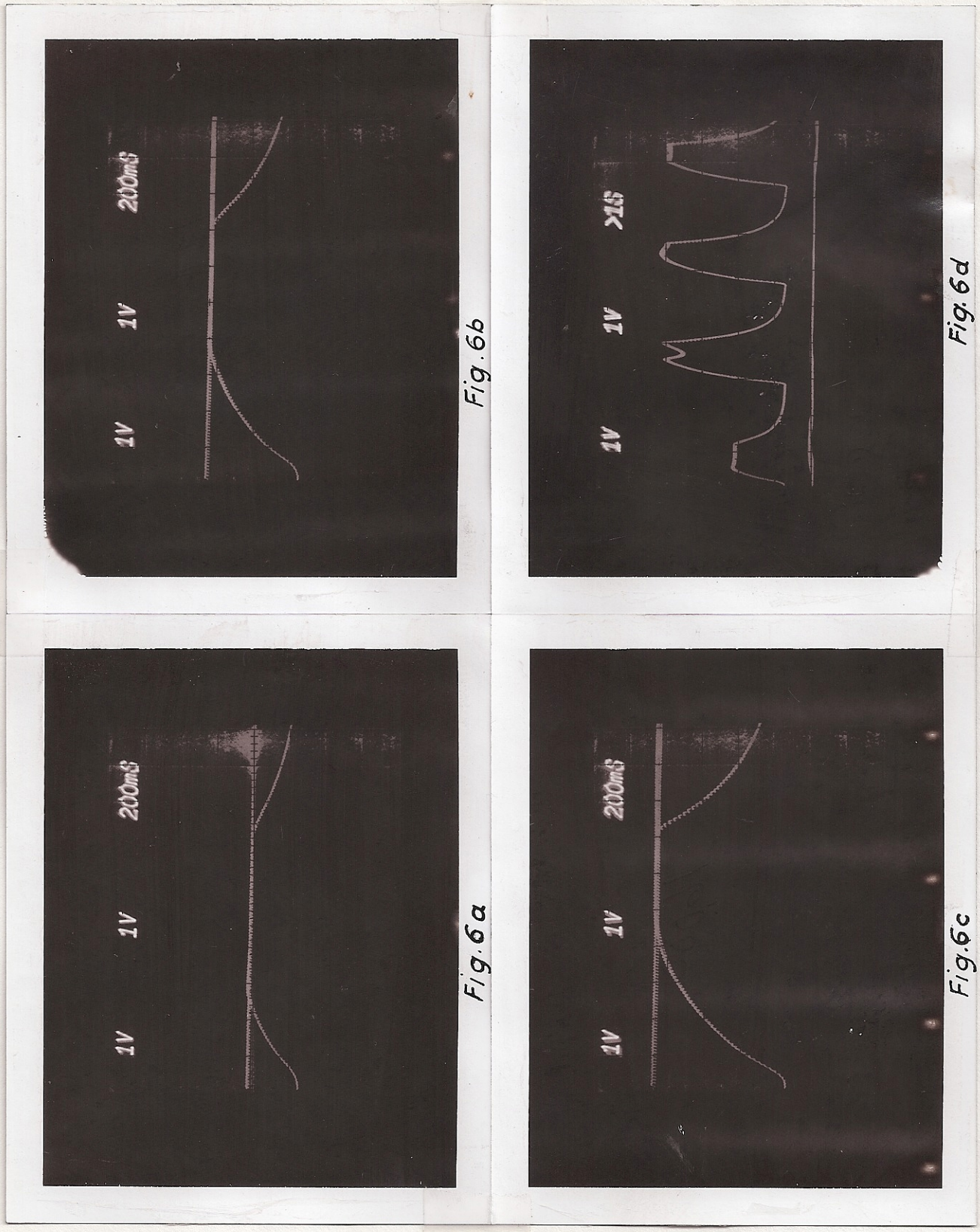


Fig.6a Fig.6b Fig.6c Fig.6d