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# PDP 11 - DATACOM interface

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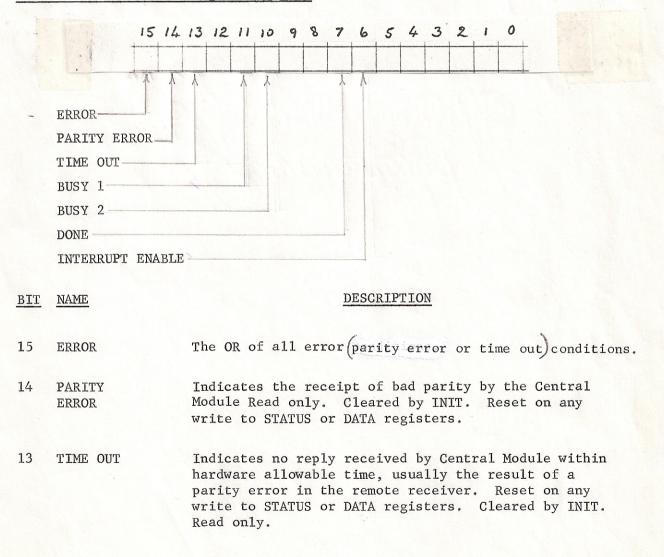
#### EP&S DIVISION TECHNICAL NOTE

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PDP 11 - DATACOM Interface

A central module of the DATACOM serial transmission system will interface to the PDP 11 Unibus via a status register and two data registers. The bit assignments in these registers are as follows:

Central Module Status Register (CMSR)



BIT	NAME	DESCRIPTION	
12	Unused		
11	BUSY 1	Indicates initiation of a load sequence. Set by any load (byte or word). Cleared when DONE becomes true. Cleared by INIT. Read only.	
10	BUSY 2	Indicates completion of a load sequence and that the DATACOM line is busy. Set by loading the high order byte of CMBR2 by a byte or word transfer. Cleared when DONE becomes true. Cleared by INIT. Read only.	
9-8	Unused		
7	DONE	Reception of line data by the Central Module is complete and data is available in the buffer or an error has occured. Cleared by referencing either data buffer (byte or word). Cleared by INIT. Causes interrupt if INT ENB is true. Read only.	
6	INTERRUPT ENABLE	Enable interrupt by DONE. Read/write. Cleared by INIT.	
5-0	Unused		
Central Module Buffer Register 1 (CMBR1)			
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Magnitude			
BIT	NAME		
		DESCRIPTION	
	Unuseg	DESCRIPTION	
15-4		DESCRIPTION 12 bit magnitude of set point or reading	
	Unuseg		
3-0	MAGNITUDE Unused All 16 bits are t		
3-0 N.B.	MAGNITUDE Unused All 16 bits are t use only 12 bits.	12 bit magnitude of set point or reading ransmitted and received. Currently, D/A converters	
3-0 N.B.	MAGNITUDE Unused All 16 bits are t use only 12 bits. ral Module Buffer	12 bit magnitude of set point or reading ransmitted and received. Currently, D/A converters Usage is device dependent. Register 2 (CMBR2)	
3-0 N.B. <u>Cent</u> :	MAGNITUDE Unused All 16 bits are t use only 12 bits. ral Module Buffer	12 bit magnitude of set point or reading ransmitted and received. Currently, D/A converters Usage is device dependent. Register 2 (CMBR2) 11 10 9 8 7 6 5 4 3 2 1 0	
3-0 N.B. <u>Cent:</u> <u>BIT</u>	MAGNITUDE Unused All 16 bits are t use only 12 bits. ral Module Buffer	12 bit magnitude of set point or reading ransmitted and received. Currently, D/A converters Usage is device dependent. Register 2 (CMBR2)	
3-0 N.B. <u>Cent:</u> <u>BIT</u> 15-8	MAGNITUDE Unused All 16 bits are t use only 12 bits. ral Module Buffer 15 14 13 12 A d dr NAME	12 bit magnitude of set point or reading ransmitted and received. Currently, D/A converters Usage is device dependent. Register 2 (CMBR2) <u>110 9 8 7 6 5 4 3 2 1 0</u> <u>DESCRIPTION</u> Address of receiver on DATACOM line. Loading this byte	

N.B.

Above assignment refer to data written by the processor. After a DATACOM cycle <u>all</u> bits read are device dependent.

#### Device Dependence

The bit definitions for CMBR1 and CMBR2 given above are, effectively, examples of usage. In particular, the assignments in CMBR1 are all device dependent and the COMMAND/STATUS bits 7 through 1 of CMRB2 are device dependent.

#### Bus Addresses

Four DATACOM central modules are installed on the PDP11 allowing 1024 remote devices to be addressed, 256 on each module. The following address assignments assume that the central modules are numbered n, where n varies from 0 through 3:

Register	Address
CMSR n	160000 + 8n
CMBR1 n	160002 + 8n
CMBR2 n	160004 + 8n
unused	160006 + 8n

#### Hardware Implementation

The central module implementation is actually a four-fold multiplexed logic design with eight output line devices paired and driven in parallel. Each pair can drive 256 addresses arbitrarily assigned between the two lines. In order to utilize this design with a single interface, two of the PDP-11 unibus address lines <sup>1</sup> (A03 and A04) are brought through the interface, by-passing the address recognition module M105. These two lines are then used to select the appropriate one of four line driver pairs. In order that the M105 module will respond to all 16 bus addresses the unused bus inputs are wired to agree with the address jumpers on A03 and A04. It is amusing to note that this implementation is transparent to the programmer, appearing as four independent devices with the above address assignments. He will not, however, be able to overlap Datacon operations on these devices!

#### References:

1) PDP-11 Peripherals and Interfacing Handbook, Digital Equipment Corporation, 1971.