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DATACOM Serial Transmission System for the PDP-11

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Introduction

A computer control system for experimenters' beam lines in the East Experimental Area is being constructed. The communication between the control computer (a PDP-11) and the controlled beam elements is by means of a serial transmission link called a DATACOM. The Datacom used in this application is a slightly modified version of that designed by R. Frankel for use in AGS control [1]. The purpose of this note is to describe the capability of the Datacom transmission link for those involved in the design of equipment which may be controlled via a Datacom.

Datacom Principle

The operation of the Datacom consists of a two part cycle. In the first, or TRANSMIT part of the cycle the CENTRAL MODULE, the Datacom element at the central control location at or near the computer, transmits a work of data serially via a single co-axial line to all the REMOTE RECEIVERS, which are receiving devices located near the controlled equipment. The word contains an address which identifies the remote receiver which is to respond. When a remote receiver recognizes that it is addressed, it returns information about the controlled device to the central module in a word of similar format to that transmitted. This operation constitutes the second or RECEIVE part of the Datacom cycle.

SET and READ Cycles

The two part Datacom cycle may be of one of two types. In a SET cycle the Central Module commands the acceptance by the Remote Receiver of data contained in the transmission. In a READ cycle, the TRANSMIT part of the

cycle merely indentifies that a READ is required at the addressed location. In the RECEIVE part of the cycle the Remote Receiver returns data to the Central Module in the same manner as for a SET cycle.

Datacom Usage

The Datacom transmission system described above provides a means of controlling and monitoring devices from a central location with minimum hardware and cabling (Figure 1). A detailed description of the bit and word formats is given below but, for the present, it suffices to note that the transmitted word consists of an 8-bit address and 24 data bits and that the received word contains 32 data bits. For a typical device with modest digital control requirements and one analog set point and one analog monitored variable the data field is subdivided by convention into an 8 bit COMMAND/STATUS field and a 16 bit MAGNITUDE field. It should be emphasized that these assignments are a matter of convention and may be varied where appropriate to the controlled device. The address field and the SET/READ bit are, however, defined by the system and must be so used in the transmission phase. A brief example of typical usage is illustrated in Figure 2. For a more detailed explanation of this application refer to Reference 2.

Format Details

In the computer control application the registers of the Datacom's Central Module are loaded in parallel from the computer. (See for example reference 3 for the computer interface). When the Datacom cycle is initiated the serial transmission occurs with the Central Module adding FRAME, KEY and PARITY bits to the data words. The sequence of bits transmitted is shown in Figure 3. The order is somewhat different from the logical fields for historical reasons of no interest in this application. The data pulses are bipolar excursions of $\frac{1}{2}$ μ s in each polarity followed by a $\frac{1}{2}$ μs rest period. The pulses are phase encoded, an initial positive excursion corresponding to a logical "1" and an initial negative excursion to a logical "0". The FRAME pulse is a special pulse formatted as a logical "0" of double duration in time. (Figure 4).

The function of the FRAME pulse is to clear all Remote Receivers to receive a transmission and as such is suitable for initializing the system.

The KEY bit is a logical "1" which indicates the completion of a transmission when it reaches the end of an initially cleared shift register. The parity bit is such as to make the total number of 1's in a transmission odd. The total number of zeros is then also odd. Both conditions are verified by the hardware. (The frame pulse is not included in the parity count.) A receiver detecting incorrect parity will not respond to the transmit cycle.

The format of the word returned to the Central module from a Remote Receiver is similar to the transmitted word but, to avoid triggering other Remote Receivers on the line, the polarity of all pulses is inverted. An inverter at the input of the Central Module restores the transmission for normal operation of its shift register etc. Parity is verified by the Central Module and a flag set to indicate an error. If no reply is received within a fixed time another error flag is set. No reply may be due to a non-existent address or to a parity error in the Remote Receiver.

A normal full cycle occurs in 107 μ s.

Extension to More Complex Devices

The system described above provides remote data acquisition and control facilities to devices of complexity comparable to a large, regulated D.C. Power supply. Extension of the system to acquire more data or provide more extensive control is made by assigning more remote receiver addresses to a given location. Each additional address provides 24 bits of control capacity and 32 bits of data returned to the central module. The central module is, of course, unmodified by the extension. In many cases, multiple but similar devices will be controlled by a given receiver. In this case the devices operate independently, merely sharing the remote receiver hardware. In other cases, a complex controlled device will operate on different parameters corresponding to the different addresses. The details of address assignment and bit definitions are the responsibility of the designer of the interface to the particular controlled devices.

REFERENCES

1. Datacom System Informal Report-AGS Technical Note H88
R. Frankel Dec. 6, 1971.

2. Datacom Interface to Magnet Power Supplies-E P & S Technical Note 52 B.B. Culwick June 26, 1972.

3. PDP-11 Datacom Interface- E P & S Technical Note 53
B.B. Culwick June 3, 1972.

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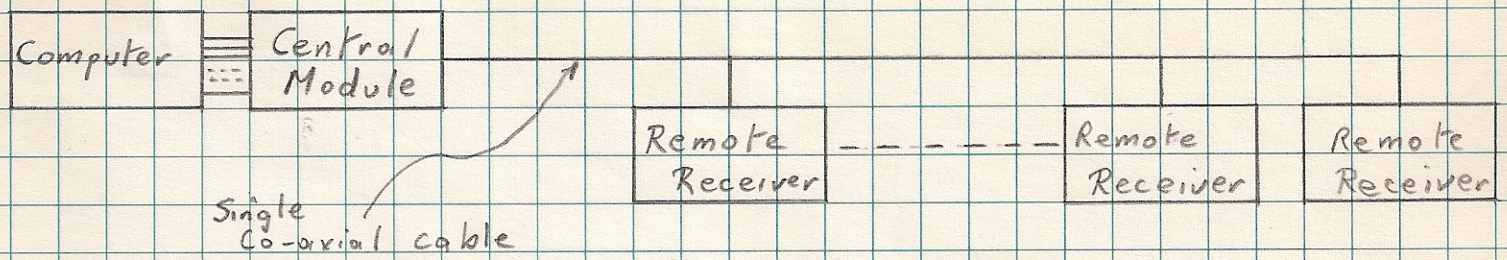
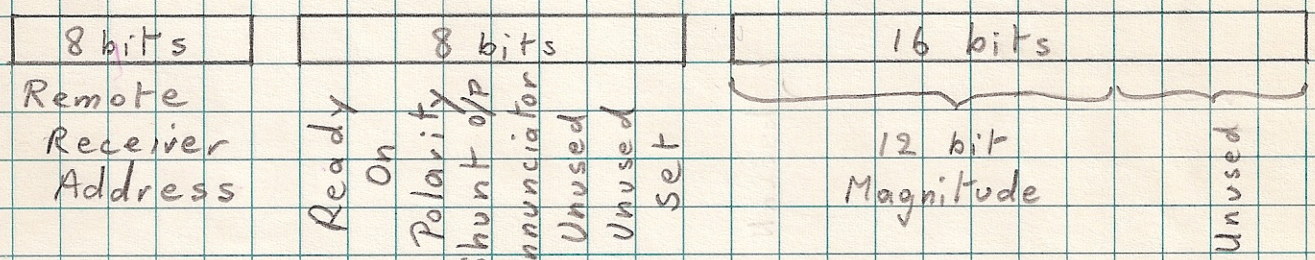


Figure 1 Datacom Block Diagram



Field: Address Command/Status Magnitude

Figure 2 Typical Bit Assignments

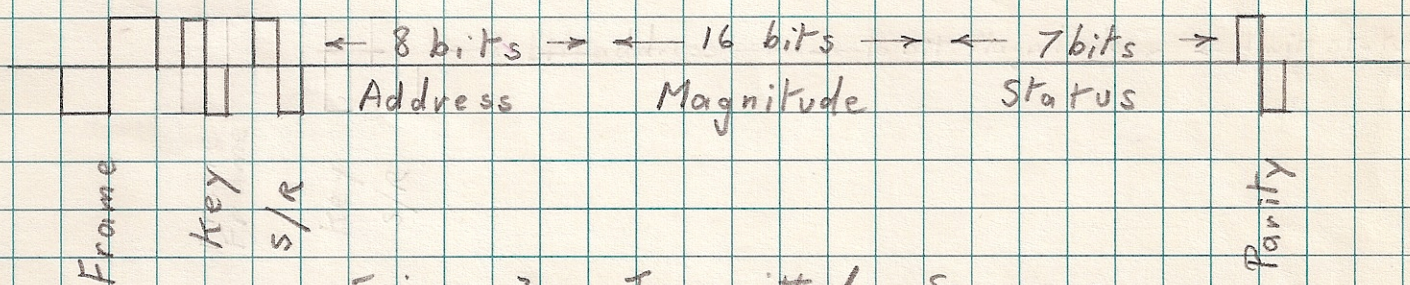


Figure 3 Transmitted Sequence

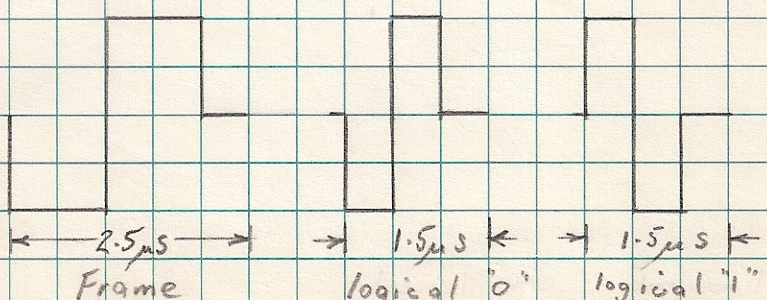


Figure 4 Bit Formats