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Single wire datacom link

V. J. Kovarik

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Collider Accelerator Department

Brookhaven National Laboratory

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EP&S DIVISION TECHNICAL NOTE

No. 49

V.J. Kovarik
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SINGLE WIRE DATACOM LINK

Introduction

This note briefly describes the data format and signal specifications of the serial transmission link between the central module and the device receivers (Fig. 1). The system as described will be used for control and data acquisition at station B.

Specifications

1. Bi-polar signals ($\pm$ 25V or $\pm$ 15V, optional) will be used to transmit data. This choice eliminates the need for dc restoration, allows closer packing of the information bits, permits a high noise rejection level and permits long runs of control cable (~5000 ft) before attenuation problems are encountered. Threshold levels (in the receivers) are adjustable.

2. In addition to the three housekeeping bits generated within the central module or device receiver, thirty-two bits of usable information are sent and received. A complete send and receive consists of seventy bits.

3. Approximately 110 microseconds will be required for a complete send and receive.

These specifications are the result of discussions with B. Culwick, D. Easler, R. Frankel and L. Leipuner.

Data Format

Figure 2 shows the transmission and reception (in block form) of data as it appears on the coaxial line. The frame pulse (F) unlocks all receivers, clears all registers and locks the receive portion of the central module. The key bit (K) enables the address lines, provided that parity bit (P) indicates that the information received is correct. If all the conditions

have been satisfied, the device receiver replies by sending out its frame pulse ($\overline{F}$). This pulse is the complement of the frame pulse sent out by the central module. Its function is to lock out all other receivers on the line and unlock the central module. A more detailed description of the internal timing sequence is beyond the purpose of this note. Notice that the reply frame pulse and the information bits are in complement form (Fig. 2). If the F pulse fails to lock out a receiver, then the key ($\overline{K}$) bit will not allow a receiver to reply to a receiver.

Figure 3 is a pictorial representation of the central module signals on the coaxial line. The frame pulse is two μsec long. Each information bit is one μsec long. In between each information bit there is .5 μsec of dead time. Clocking occurs approximately .75 sec after the start of an information bit.

Distribution: EP&S Div.
A. Maschke
R. Frankel
L. Leipuner
G. Smith

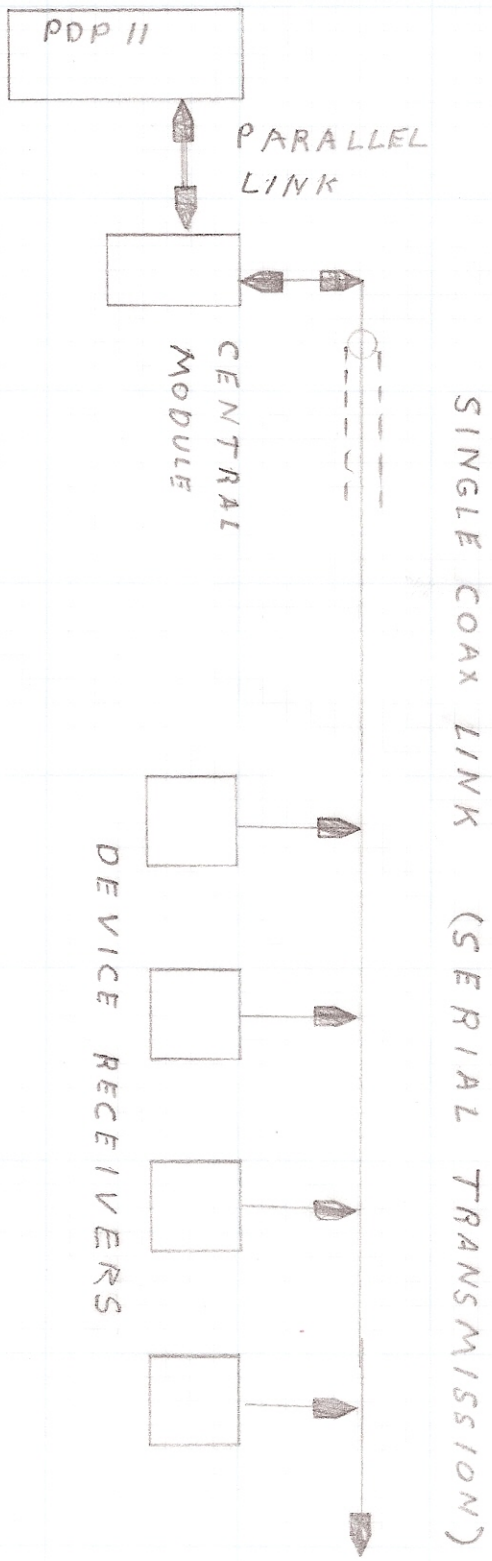

PDP 11
PARALLEL LINK
CENTRAL MODULE
SINGLE COAX LINK (SERIAL TRANSMISSION)
DEVICE RECEIVERS

FIG. 1

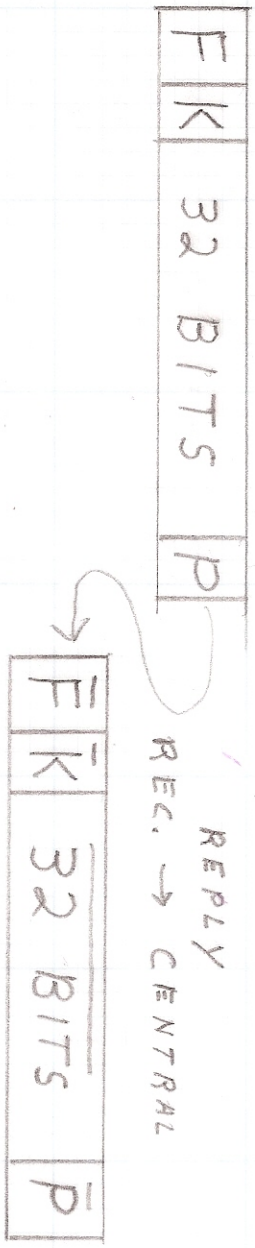
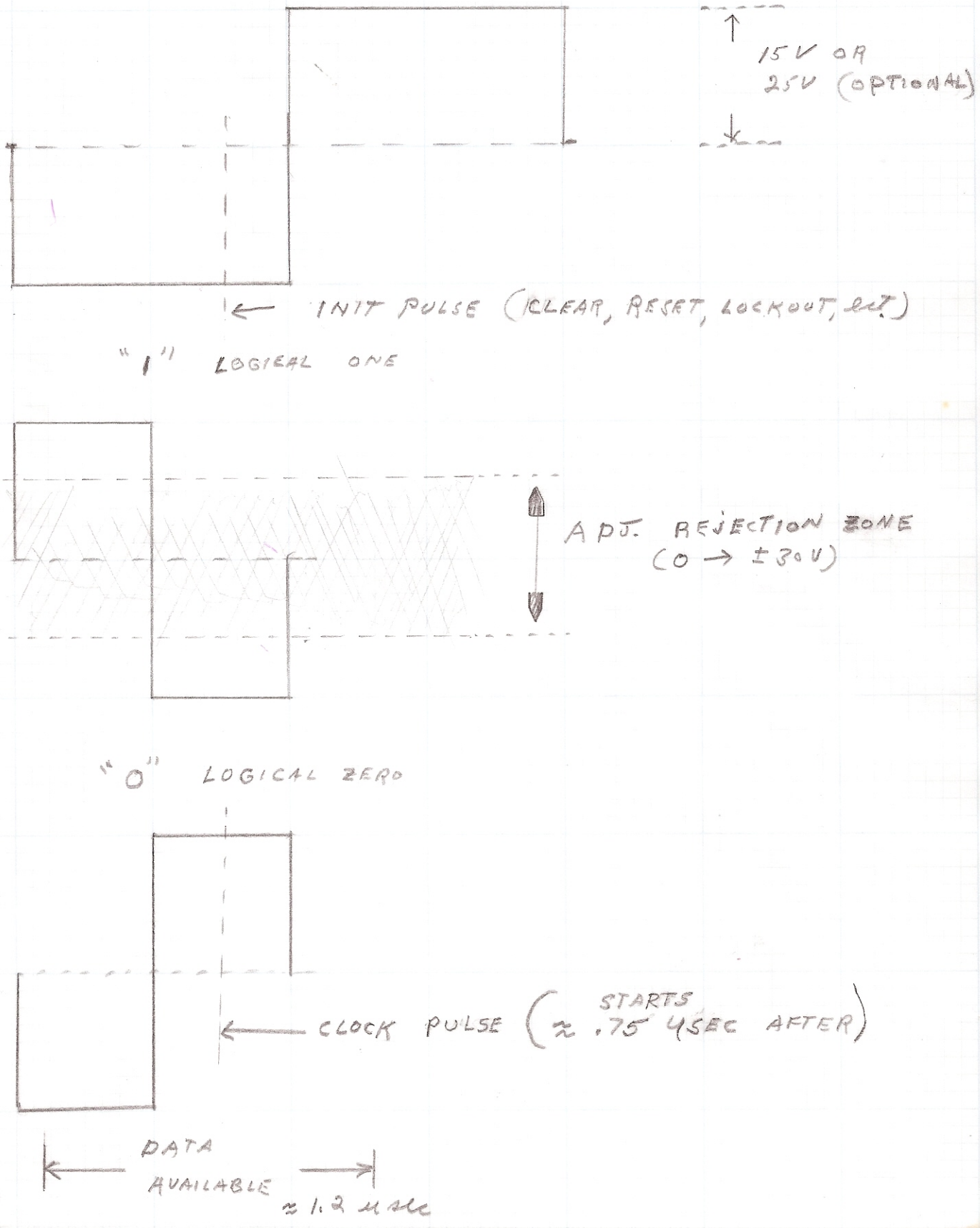

F
K
32 BITS
P
SEND
CENTRAL MOD. → REC.
REPLY
REC. → CENTRAL

FIG. 2

FIG. 3



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