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Intergrator modifications for booster loss monitor system

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Experimental Planning and Support Division Technical Note

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INTEGRATOR MODIFICATIONS FOR BOOSTER LOSS MONITOR SYSTEM

E. Beadle and B. Clay
July 27, 1992

Introduction.

The 8-Channel Integrator boards have been modified for use in the Booster Loss Monitor System (BRLM). The modifications were necessary due to limitations in the original circuit (D36-E130). This note briefly discusses the modifications made to the circuitry, and some of the performance bounds to keep in mind when applying the basic circuit.

Basic Circuit Assumptions.

The basic integrator is shown in Fig. 1. In this generic configuration many of the circuit subtleties are not apparent. For the usual analysis several assumptions are applied:

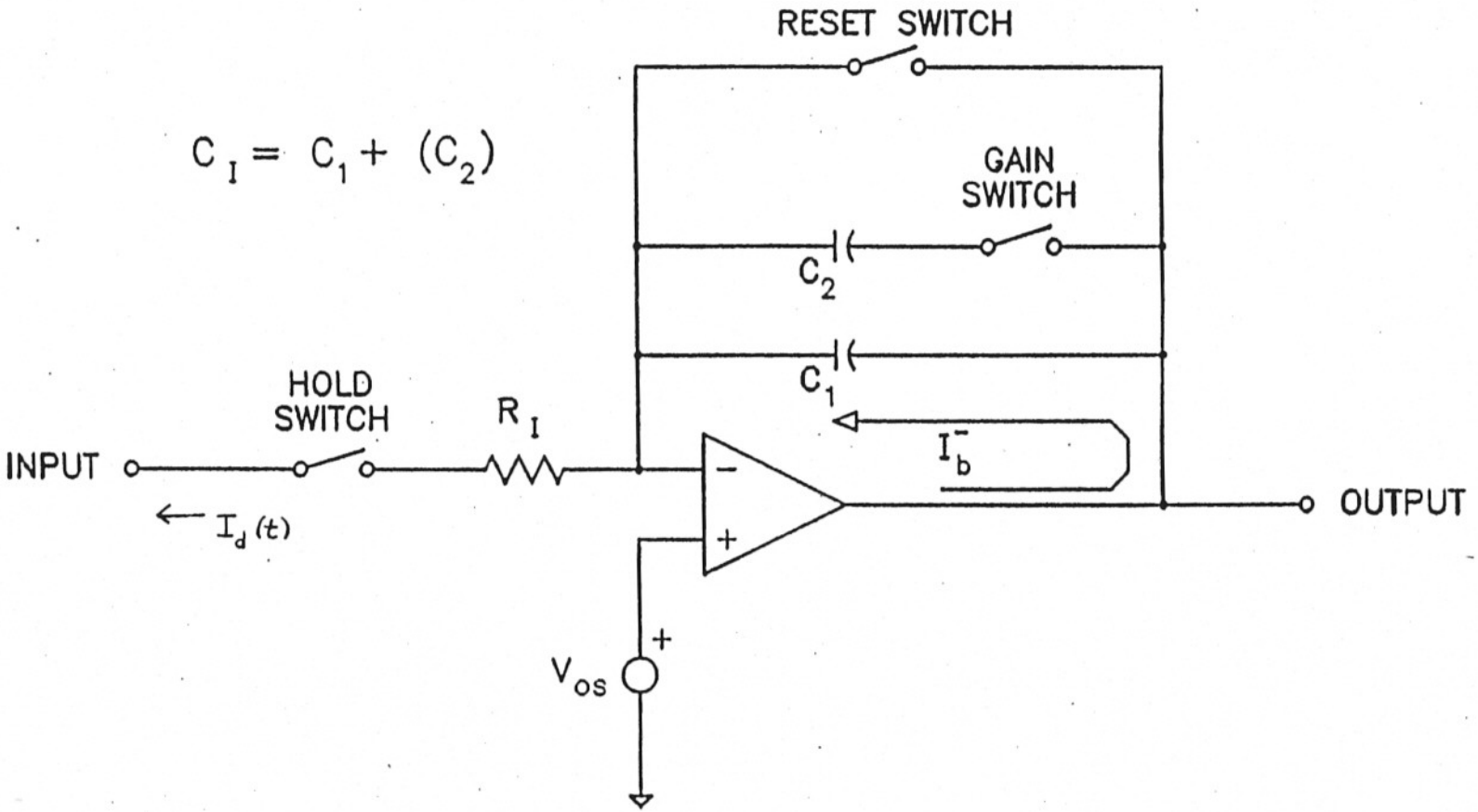
- Reset and Hold Switches "on" resistance is 50-150 ohms.
- Turn-on and Turn-off times of switches are negligible.
- Total resistance shunting feedback capacitor limits its discharge rate.
- Op-amp slew rate does not limit circuit response.
- Charge injection is independent of output polarity.
- No crosstalk between channels.

However, these assumptions are not strictly true and can lead to erroneous conclusions about the circuit operation. This has been particularly troublesome when the reset time was to be minimized.

Amplifier Limitations.

The initial design of the integrator circuit used the Burr-Brown 3527 op-amp. The 3527 amplifier has a slew rate < 1 V/μs and a settling time of 45 μs. Therefore, to reset from a

IDEALIZED INTEGRATOR CIRCUIT



$$V_o = + \frac{1}{C_I} \int I_d(t)dt$$

FIGURE 1

[2]

10 V output, at least 10 μs should be budgeted. However, when settling and switch transient times are included, the total time to reset exceeds the budgeted amount (10 μs) for application in the BRLM system. Therefore the Burr-Brown OPA602 was selected and tested. The slew rate of the OPA602 is 35 V/μs, and therefore slews the 10 V output range in less than 1 μs. The settling time of the 602 is rated at 1 μs.

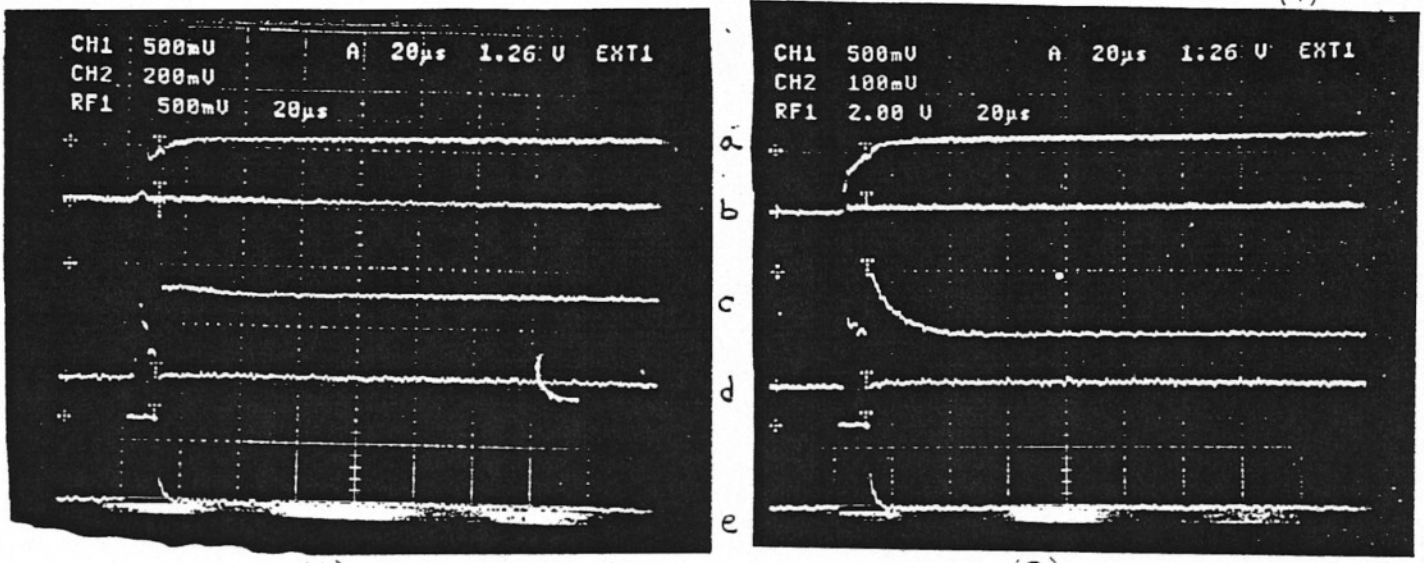
However, other limitations in the reset circuit, cause the reset time to be increased above the 1-2 μs range, as explained in this and the following sections. Figures 2 and 3 show the difference in the time responses for a reset operation. Important features to notice are that OPA602 inverting terminal remains nearly at virtual ground throughout the reset, as opposed to the 3527. It is the lack of virtual ground which illustrates the 3527 is overloaded and will require many microseconds to settle at 0 V. However, the BRLM system's reset time is much shorter than the 3527 settling time, and thus when the reset switch, a FET, opens after 10 μs, the opamp continues to settle and charge will accumulate on the feedback capacitor causing a residual offset as shown in the figures. The residual offset of the 3527 circuit was found to be a non-linear function of the output level prior to the reset operation. The offset shown for the OPA602 was from misadjusted charge compensation.

It is believed that the residual offset of the 3527 is caused by the termination of the reset, which creates other circuit imbalances, while 3527 is settling, and when the entire circuit has settled the output is at the residual offset. On the other hand the OPA602, has a 1 μs settling time (.01% for a 10 V step), and therefore completely settles during the reset time. Further, it is important to realize that when an amplifier has gone through a period of non-linear (constant-current) slewing, there is a period of time where the amplifier goes through overload recovery. The recovery time persists for a period commensurate with the slewing. Thus for a fixed slew rate, larger outputs cause longer slew times, and thus longer recovery times. In overload recovery, the circuit dynamics can be non-linear and difficult to predict. In the case of the 3527, and accounting for the switch turn-on delay (see below), resetting from outputs above 4 V can cause the overload recovery to persist beyond the duration of the reset. Following the overload recovery, linear settling occurs and the response in this period of time can be predicted using linear circuit theory. Fortunately, for the circuit designer the settling time specification should include the overload recovery time.

During the rest of the testing with the OPA602 in the circuit, it was determined that the slew rate of 35V/μs does not limit the circuit response in the circuit configurations used. For comparison the 3527 and 602 data sheets are included in Appendix B.

Reset Switch Limitation.

Through experimentation it has been found that there is a delay between the signal applied at the reset input and the reset FET switching "on." The delay is not constant and depends on



(A) $C_I = 1{,}000$ pF

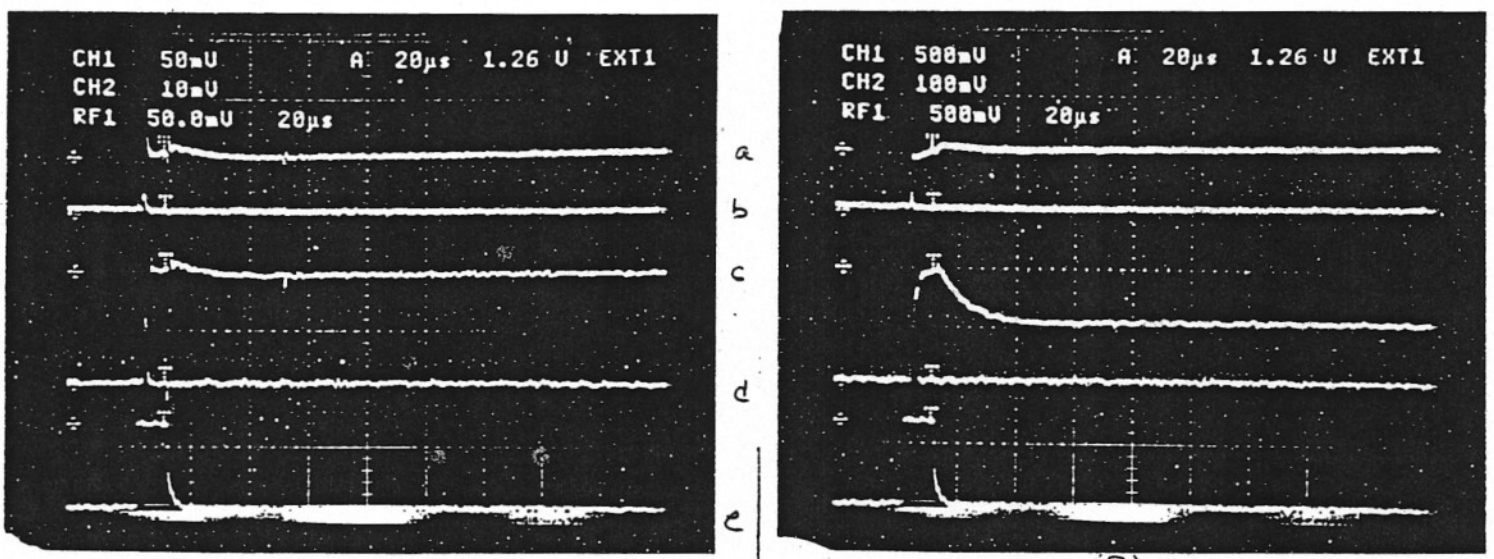
(B) $C_I = 180$ pF

FIGURE 2

TRACE

a. OPA 602 OUTPUT @ .5 V/DIV
b. OPA602 INVERTING INPUT @ 1 V/DIV
c. 3527 OUTPUT @ 2V/DIV
d. 3527 INVERTING INPUT @ 2V/DIV
e. GATE OF RESET FET (2N4416) @ 10V/DIV

(FOR a-c IN 2A & 2B THE INPUT IS -10 nA FOR 2 SECONDS)



(A) $C_I = 1{,}000$ pF

(B) $C_I = 180$ pF

FIGURE 3

TRACE		3A	3B
a	OPA602 OUTPUT	.05 V/DIV	.5 V/DIV
b	OPA602 INVERTING INPUT	.1 V/DIV	1 V/DIV
c	3527 OUTPUT	.05 V/DIV	.5 V/DIV
d	3527 INVERTING INPUT	.1 V/DIV	1 V/DIV
e	GATE OF RESET FET (2N4416)	10 V/DIV	

(FOR a-c IN 3A & 3B THE INPUT IS -10nA FOR 100 ms)

both the polarity and level of the output. Figures 4 and 5 display the reset for positive and negative outputs of various levels. Figure 4 shows the reset from a positive voltage. In this mode, there is a fixed 1.5 μs delay from the reset input to the output decaying towards zero. It is also important to notice the shape of the decay. Because the decay curve is not a straight line, the discharge rate is not limited by the FET I_{dss} of the FET as is the case below (see capacitor selection) or the opamp slew rate.

As convention dictates, the source terminal is the terminal from which the majority carriers flow. When the output is positive, the source of the FET is connected to the inverting terminal of the opamp. The opamp maintains the source at virtual ground, thus when the gate voltage barely exceeds the value of the $V_{gs(off)}$ the drain current will just begin to flow. Further increases in the gate voltage will allow more drain current to be conducted. Because the source voltage is fixed, the gate voltage at which the FET will begin to conduct is also fixed, hence the delay is fixed. Note that in this case the maximum V_{gs} is 0 V, so the gate current I_g is zero and the maximum current that can flow is limited by I_{dss} (see Appendix A). Operation of the FET in this manner is referred to as first quadrant operation.

For the case of negative output it should be noted that the role of the drain and source terminals is reversed. The source of majority carriers is now connected to the opamp output. Therefore when a reset is triggered, the gate voltage will increase from its most negative value (-14 V) to a point where the gate voltage begins to turn the FET "on." This is $V_{gs(off)}$ and is between -3 V and -6 V. Therefore, if $V_{gs(off)}$ is -6 V output levels less than -8 V will cause the FET not to turn completely off. As the output starts at more negative values, lower values of the gate voltage will turn-on the FET. Thus the FET turns-on with less delay as shown in Fig. 5. In this case the gate current I_g is not zero, as the gate-source junction is forward biased to some degree. The forward bias will also cause the maximum discharge current flowing between the drain and source terminals to exceed I_{dss}. Operation of the FET in this manner also corresponds to first quadrant operation, but is not a normal FET operation mode.

The present design (Fig. 6) uses Siliconix 2N4416 switching FETs. These FETs are limited to a zero gate bias drain current of 10 mA. This current is referred to as I_{dss}. For the case of positive output, the source is held at virtual ground by the opamp. Therefore, the drain-source voltage is positive and when the gate has fully switched to zero volts the FET follows the curve shown in Appendix A. On this curve the maximum current drawn through the FET is 10 mA. This current limits the discharge rate of the feedback capacitor. The capacitor discharge is linear while the FET is in the saturation region. When the output has dropped below the pinch-off voltage the capacitor decay becomes exponential. The reset to ground from a positive output is shown in Figs. 7a-7c under different conditions.

The difference between Fig. 7a and 7b is that the integrating capacitor has been increased from 1 nF to 10 nF. The maximum discharge rate then for the condition in 7b is 1 V/μs (10 mA/10 nF). The photo shows the top trace is linear in time with slope of 1 V/μs indicating the FET's I_{dss} limitation on the reset. The reset width was set at 10 μs, yielding an output of 5 V after reset. As a result, an FET with greater current handling capability was selected. Photo

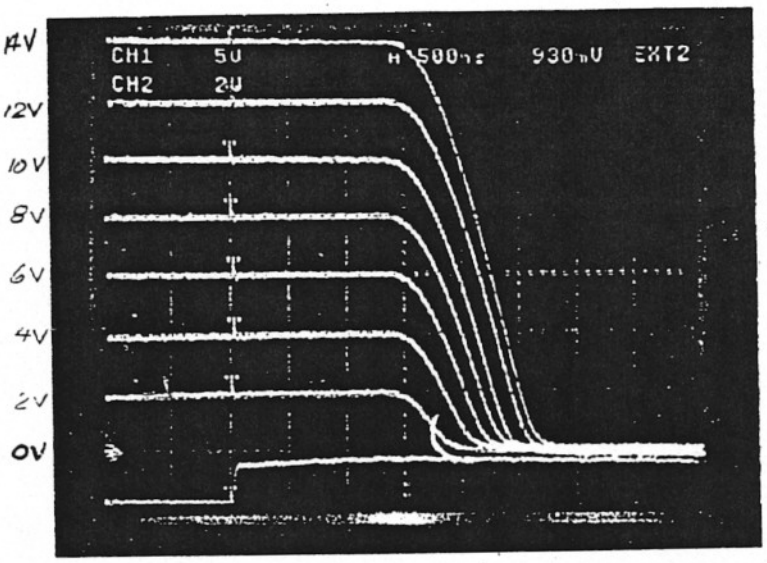
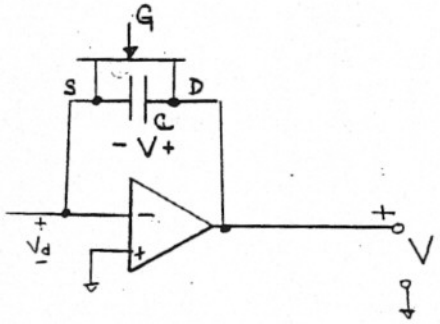


FIGURE 4

$C_I = 180$ pF

BOTTOM TRACE: RESET INPUT @ 5V/DIV

TOP TRACE(S): OPA602 OUTPUT @ 2V/DIV (POSITIVE OUTPUT)



$V_d \approx 0$

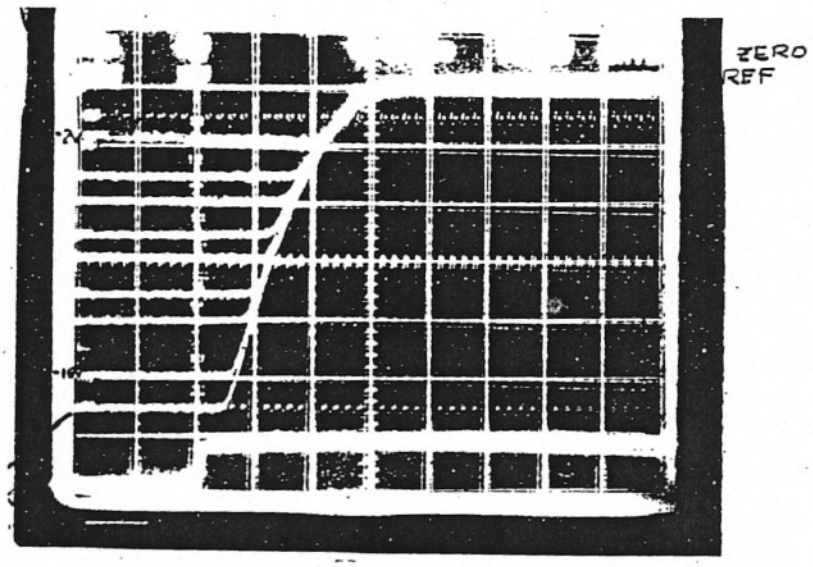


FIGURE 5

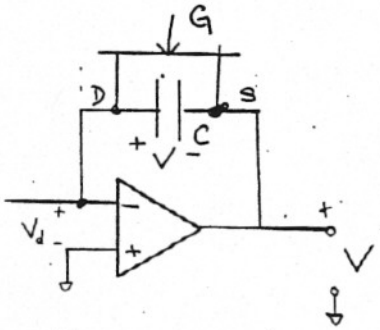
$C_I = 180$ pF

$t = 500$ ns/DIV

$V = 2$ V/DIV (TOP TRACE)

BOTTOM TRACE: RESET INPUT @ 5V/DIV

TOP TRACE(S): OPA602 OUTPUT (NEGATIVE OUTPUT).



$V_d \approx 0$

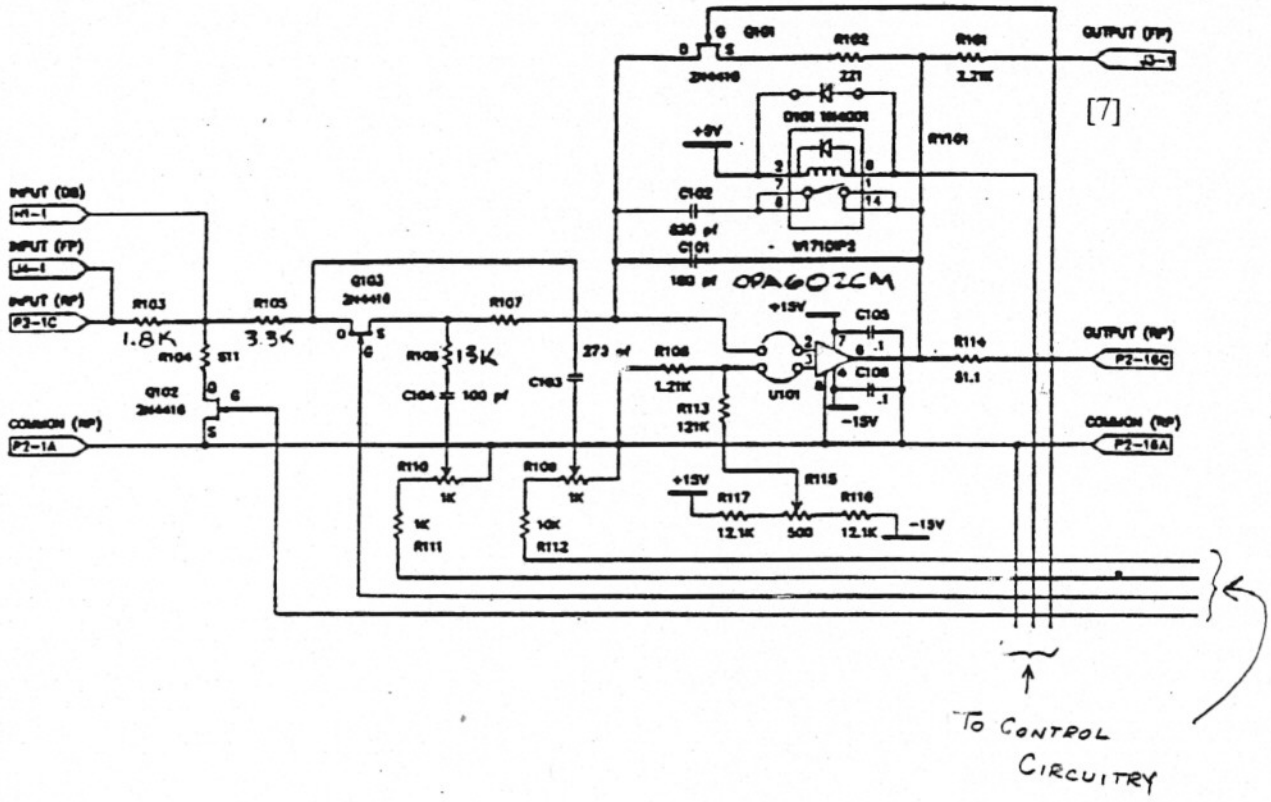
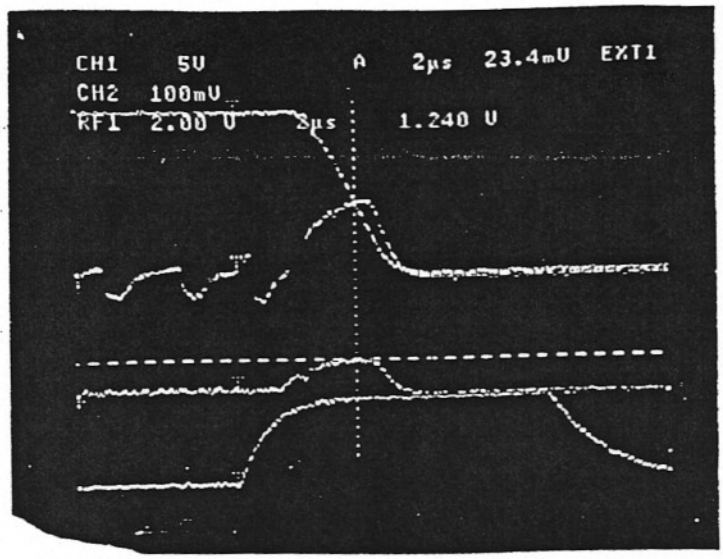


FIGURE 6: 1/8TH OF 8 CHANNEL INTEGRATOR (D36-E905)



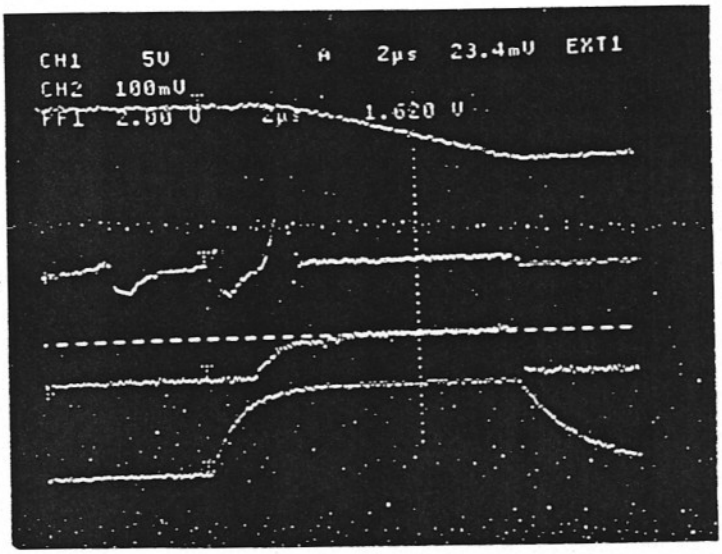
A

FOR A-C

TOP = OPA602 OUTPUT @ 5V/I
OPA602 INVERTING INPUT @ 100 mV/I
* ΔV ACROSS RX02 @ 2V/DIV
BOTTOM = GATE OF QX01 @ 10V/DIV

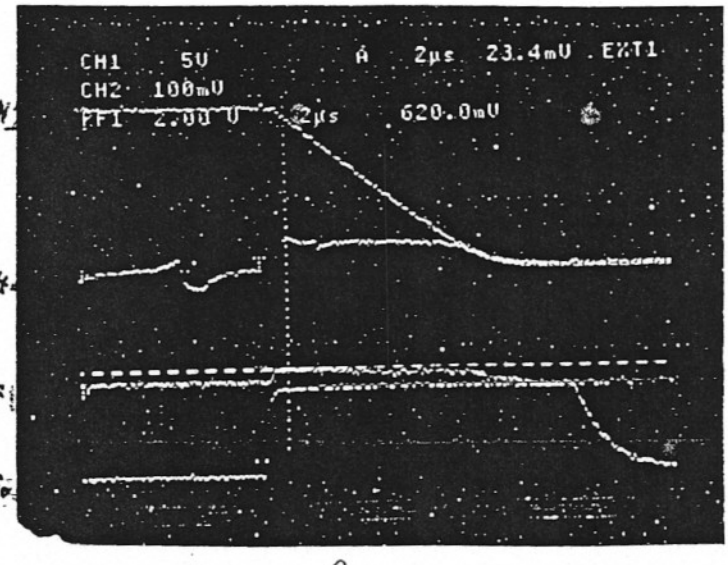
(* $I_{DS} = \Delta V / RX02$)

A: C_I = 1NF, FET = 2N4416
RX02 = 221 Ω



B

B: C_I = 10NF, FET = 2N4416
RX02 = 221 Ω



C

C: C_I = 10 NF, FET = 2N4861
RX02 = 22 Ω

FIGURE 7

7c shows the circuit response with a 2N4861 replacing the 2N4416. The 2N4861 has an I_{dss} range of 8-80 mA. Also comparing the last trace in Fig. 7b and 7c, it can be seen that the 2N4861 turns on faster. It is believed that the inverting terminal trace is showing "oscillation" prior to the reset, because the opamp is saturated, and the pulse away from virtual ground during reset is due to current flow discharging the capacitor.

For negative outputs the source is the terminal attached to the circuit output (see Fig. 5). As the gate goes towards zero volts and exceeds the source terminal voltage, the gate-source junction becomes forward biased and conducts current. Because $I_g \neq 0$ and $I_{ds} > I_{dss}$ a full reset can be achieved in the 10 µs allotted. Photos 8a-8c demonstrate this effect. In this case the I_{dss} limit does not occur as in the previous case and by viewing the second trace it can be seen that in each case the output resets to zero. The slower reset in photo 8b is due to the increased capacitance of 10 nF. The decrease in the reset time from 8b to 8c is due to the replacement FET drawing larger currents than the 2N4416 for the values of V_{gs} encountered in the reset operation.

Also, compare Figs. 8a-c with 7a-c, and notice that the gate voltage goes to zero more quickly in the positive output case, and for the negative output case the gate voltage follows the source discharge. This confirms the claim that for negative outputs the gate-source junction becomes forward biased.

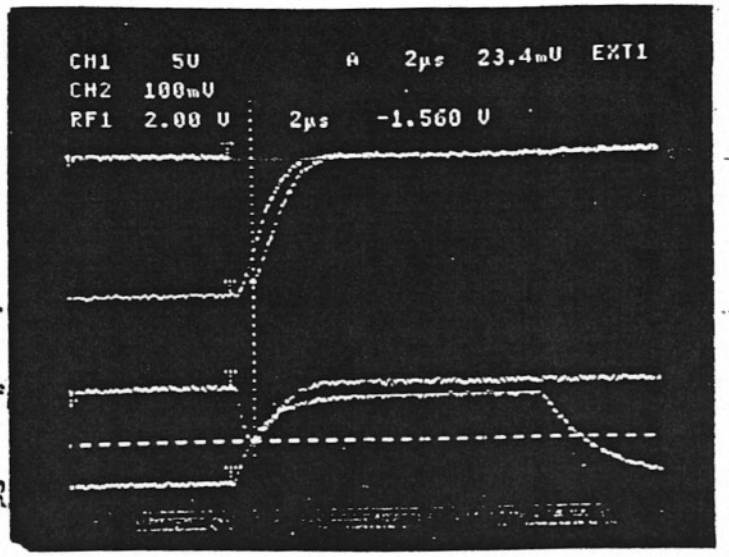
An additional change in Figs. 7c and 8c is the current limiting resistor in series with the FET has been reduced from 221 ohms to 22 ohms to try and decrease the reset time constant when the FET operates in triode region.

Finally, it was found that the reset FET did not "snap-off" when the reset signal is turned off (photos 7 and 8). This is because the original intention of the integrator circuit was to have a delay after the end of reset and before re-entering the integrate mode. However, in the loss monitor system is its not desirable to have this delay. Therefore, the FET switch control circuitry was modified to speed-up the turn-off. The control circuitry modification was to replace the FETs and BJTs and reduce some resistor values. This has had only a minor improvement.

Capacitor Limits.

Selection of an appropriate sized capacitor for the integrator can be difficult. The choice is based on balancing sensitivity, maximum signal, reset time constraints, slew rate limits and circuit errors. Generally, there is a minimum signal level of interest and for systems with A/D converters the output level should be matched to the A/D converters least significant bit. Thus, small currents require a small capacitor to provide the required output level. However, smaller capacitors impact on bias, drift and charge injection errors. These errors scale inversely to the capacitance size, and errors due to the bias current linearly increase with time. The drift in the baseline over time decreases the dynamic range and accuracy of the system. Charge injection from the switches can be nulled to some degree. However, over time and temperature the

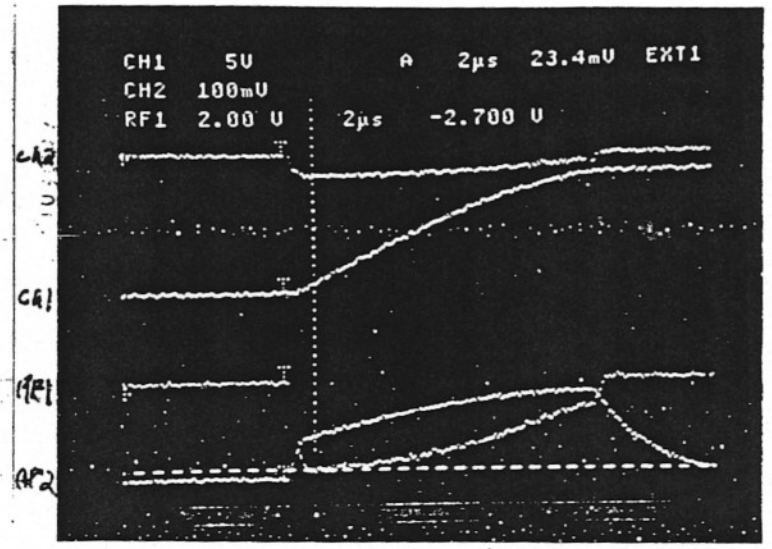
FOR A-C



A

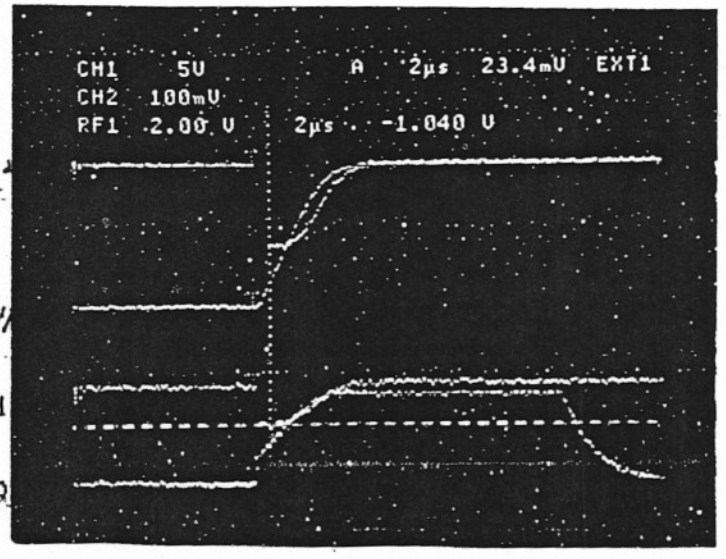
TOP = OPA602 OUTPUT @ 5V/DIV
OPA602 INVERTING INPUT @ 100mV/DIV
ΔV ACROSS RX02 @ 2V/DIV
BOTTOM: GATE OF QX01 @ 10V/DIV

A: C_I = 1NF, FET = 2N4416
RX02 = 221Ω



B

B: C_I = 10NF, FET = 2N4416
RX02 = 221Ω



C

C: C_I = 10NF, FET = 2N4861
RX02 = 22Ω

FIGURE 8

adjustment is not perfect and small capacitors amplify the residual charge imbalance. Additionally, charge injection effects with small capacitors is exacerbated because the charge injection will vary due to the forward biasing of the gate-source junction with negative outputs as opposed to positive outputs which do not forward bias the junction.

Another bound on the capacitor size can be found from the slew rate and output current limits of the amplifier selected. For the minimum value, the capacitor must satisfy the equation below so the amplifier is not overloaded while measuring the input.

$$Capacitor\ Value > \frac{Max\ Opamp\ Output\ Current}{Opamp\ Slew\ Rate} \tag{1}$$

Satisfying this criteria insures that even drawing the maximum current from the amplifier, the rate of change of the voltage across the capacitor will not exceed the amplifier slew rate. However, if less than the full output current will be drawn, then the capacitor can be downsized. For example, the loss monitor system maximum current draw is 1 mA, as imposed by the power supply, and with a slew rate of 35 V/μs, the minimum capacitor value is 29 pF based on this criteria.

Another lower bound can be generated by considering the "non-idealness" of the opamp such as finite open-loop gain. The open-loop gain will limit the integrator low frequency response and the accuracy of the integrator. A derivation of this limit is shown in Appendix C. Therefore, when considering application in a low frequency circuit, the lower 3 db point of the integrator should be checked over the range of open loop gains expected.

In estimating an upper bound for the capacitor the opamp slew rate limit will be neglected. However when applying the equations below, if the output slew rate meets or exceeds the opamp slew rate, the analysis must be redone considering effects of the opamp output current and settling time. Presently a reset time of T seconds from an initial value of V_i volts is considered. The circuit output and capacitor voltage is given by:

$$V_f = V_i - \frac{1}{C} \cdot \int_0^T i_{capacitor}(t) \cdot dt \tag{2A}$$

where:
V_i = initial circuit output voltage
V_f = final circuit output voltage
$i_{capacitor}(t)$ = capacitor discharge current
C = capacitor value
T = reset time

For positive outputs above the FET pinch-off voltage the capacitor discharge current is limited by the FET I_{dss}. Below this voltage, the FET operates in the triode region and acts like a resistor. In the saturation (pentode) region, the approximate time to reach the triode region is calculated below.

$$V_i - |V_{gs(off)}| = \frac{1}{C}\int_0^{T_{sat}} i_{ds}dt = \frac{1}{C}\int_0^{T_{sat}} i_{capacitor}(t)dt \qquad (2B)$$

Assuming that in the pentode region, for $V_{gs} = 0$, that i_{ds} is the constant, equal to I_{dss} and independent of V_{ds} we get:

$$V_i - |V_{gs(off)}| \approx \frac{1}{C} \cdot I_{dss} \cdot T_{sat} \qquad (2C)$$

which simplifies to:

$$T_{sat} = \frac{V_i - |V_{gs(off)}|}{I_{dss}} \cdot C \qquad (3)$$

As the output voltage drops below pinch-off, discharge current required by the cap will drop below the I_{dss} value, and then be limited by the FET resistance. Below pinch off, the voltage will decay exponentially, rather than as in the above case where the voltage decays linearly. In this regime, the discharge time can be estimated as:

$$-(R \cdot C) \cdot \ln\left(\frac{\epsilon}{V_p}\right) \approx T_{tri} \qquad (4)$$

where:

R	=	resistance shunting capacitor
C	=	capacitance value
ϵ	=	the final voltage ($\epsilon \leq V_p$)
V_p	=	pinch-off voltage
T	=	reset time

It should be noted that the R in the equation above is a combination of the FET resistance in series with any other current limiting resistance. Also the FET resistance is varying as V_{ds} (the output) changes, and in a somewhat non-linear fashion. However, for the first order calculations, the FET can be linearized to 100-150 ohms in the triode region. This value is found by reading the FET curves (Appendix D).

Therefore, to first order the total reset time is given as the sum of T_{tri}, T_{sat} and FET turn-on delay. For a given reset time T and initial output voltage V_i, and FET characteristics,

the maximum capacitance value can be selected according to the equation below (assuming $T_{sat} \geq 0$):

$$T_{tri} + T_{sat} + 1.5 \times 10^{-6} \leq T_{reset} \tag{5A}$$

$$-R \cdot C \cdot \ln\left(\frac{\epsilon}{V_p}\right) + \frac{V - V_p}{I_{dss}} \cdot C + 1.5\mu s \leq T_{reset}$$

$$C \leq \frac{[T_{reset} - 1.5\mu s]}{-R \cdot \ln\left(\frac{\epsilon}{V_p}\right) + \frac{(V - V_p)}{I_{dss}}\ ]} \tag{5B}$$

Thus, given the appropriate circuit parameters the maximum capacitance that can be reset in T seconds to a voltage ϵ can be estimated. This is important when a circuit channel is to be desensitized as has happened in the BRLM system during the present running period. The equation for the reset from a negative output has not been derived because the loss monitor system operates with positive outputs only.

An additional upper bound on the capacitance can be generated by considering the maximum charge to be stored on the capacitance corresponding to a full scale output. Typically, the full scale output is 10 V, and charge is the time integral of current so:

$$\frac{\int_0^T i_{inp}(t)dt}{Full\ Scale\ Voltage} = Capacitor\ Value \tag{6}$$

where $i_{inp}(t)$ = Input current from source.

Finally, an upper bound on the capacitance (C) based on the required output rate-of-change can also be calculated. This bound neglects the effects of the capacitor on overload recovery and linear settling times. Therefore, useable values will be somewhat lower than predicted here. Assuming that the input current (I_{inp}) and required slew rate (SR_{req}) do not exceed the amplifier' specifications, we have:

$$\frac{I_{inp}}{C} \geq SR_{req}$$

So, solving for the capacitance we find:

$$\frac{I_{inp}}{SR_{req}} \geq C \qquad (7)$$

Charge Injection Compensation

Due to the different modes of operation in the reset circuit, the charge injection effects can be different and therefore a simple adjustment for nulling may not be possible. For example, if the circuit is used in both the positive and negative polarities the amount of charge injected in the channel under these conditions is different, and adequate cancellation is difficult, if not impossible. Therefore, rigorous testing to assess how the circuit will function under the expected operating conditions is necessary.

Channel Crosstalk

There exists some interchannel crosstalk on the boards. This is most obvious when a channel with high source resistance has saturated. Under this condition, the interchannel capacitance charges up, injecting charge into adjacent channels. Also, the channels can communicate through the circuitry common to the gates of the FET switches. This effect has not been rigorously characterized.

Input Impedance

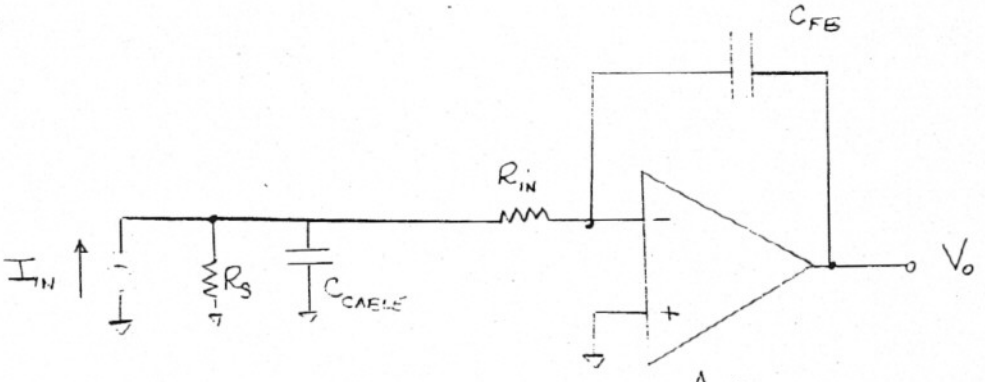
The input impedance of the standard integrator channel has been reduced in order to decrease the input time constant caused by cable capacitance. A model of the circuit and its response are shown in Fig. 9. As shown in the figure, the cable capacitance causes a delay in the response of the circuit. The circuit still maintains its accuracy, because the charge on the capacitance will enter the integrator when the pulse is removed. This is because the signal comes from a current source. However, there is still the delay caused by the input time constant in collecting all the charge. This is also shown in Fig. 9.

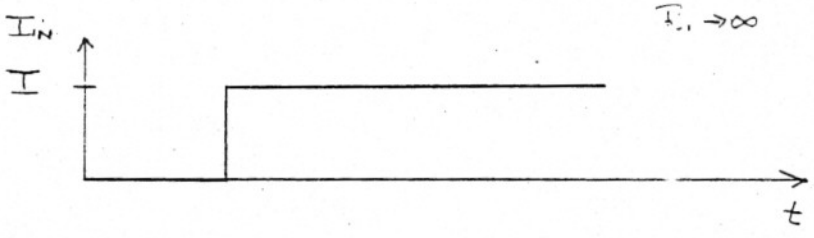
Documentation

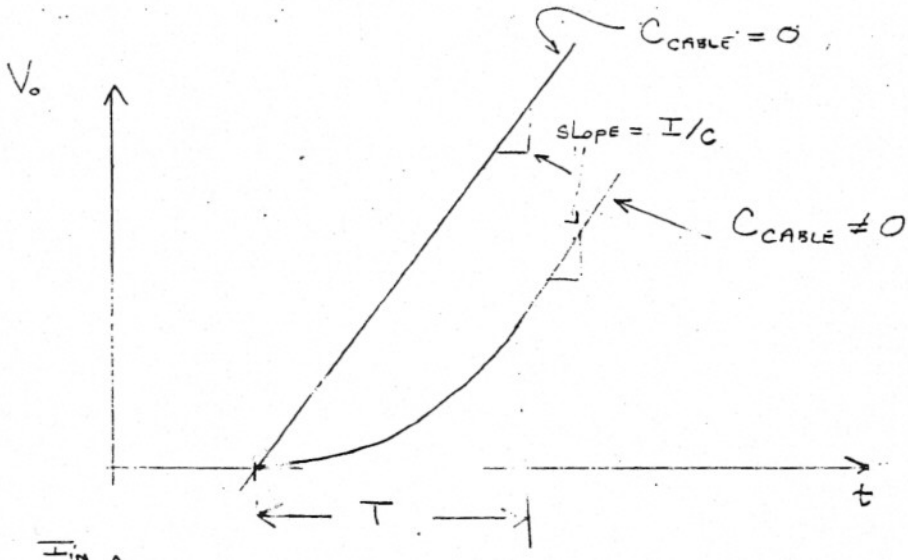
The versions of the BRLM integrators are available in the design room on drawing numbers:

- D36-E908 (36 KiloOhm Input Impedance Version)
- D36-E905 (5.1 KiloOhm Input Impedance Version)
- D36-E817 (510 Ohm Input Impedance Version)

EFFECTS OF INPUT TIME CONSTANT







$T \approx 5 \cdot R_{IN} \cdot C_{CABLE}$

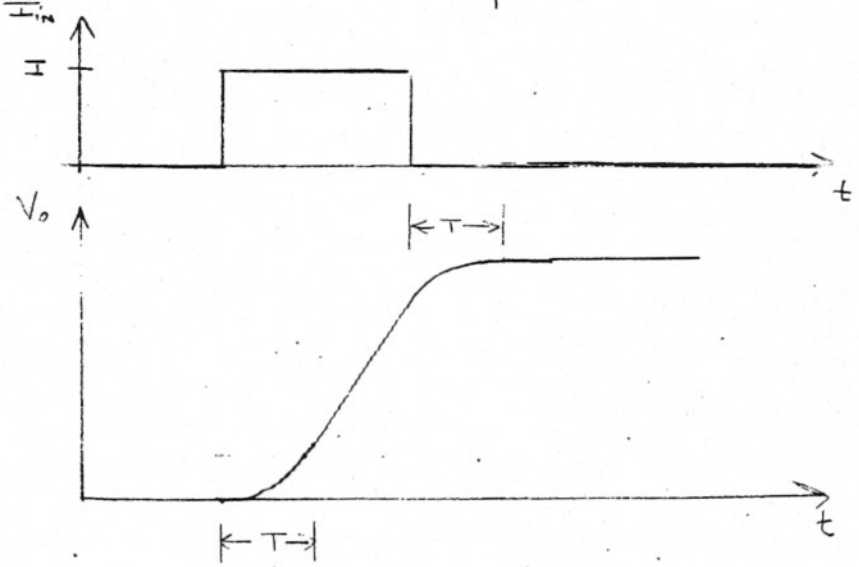
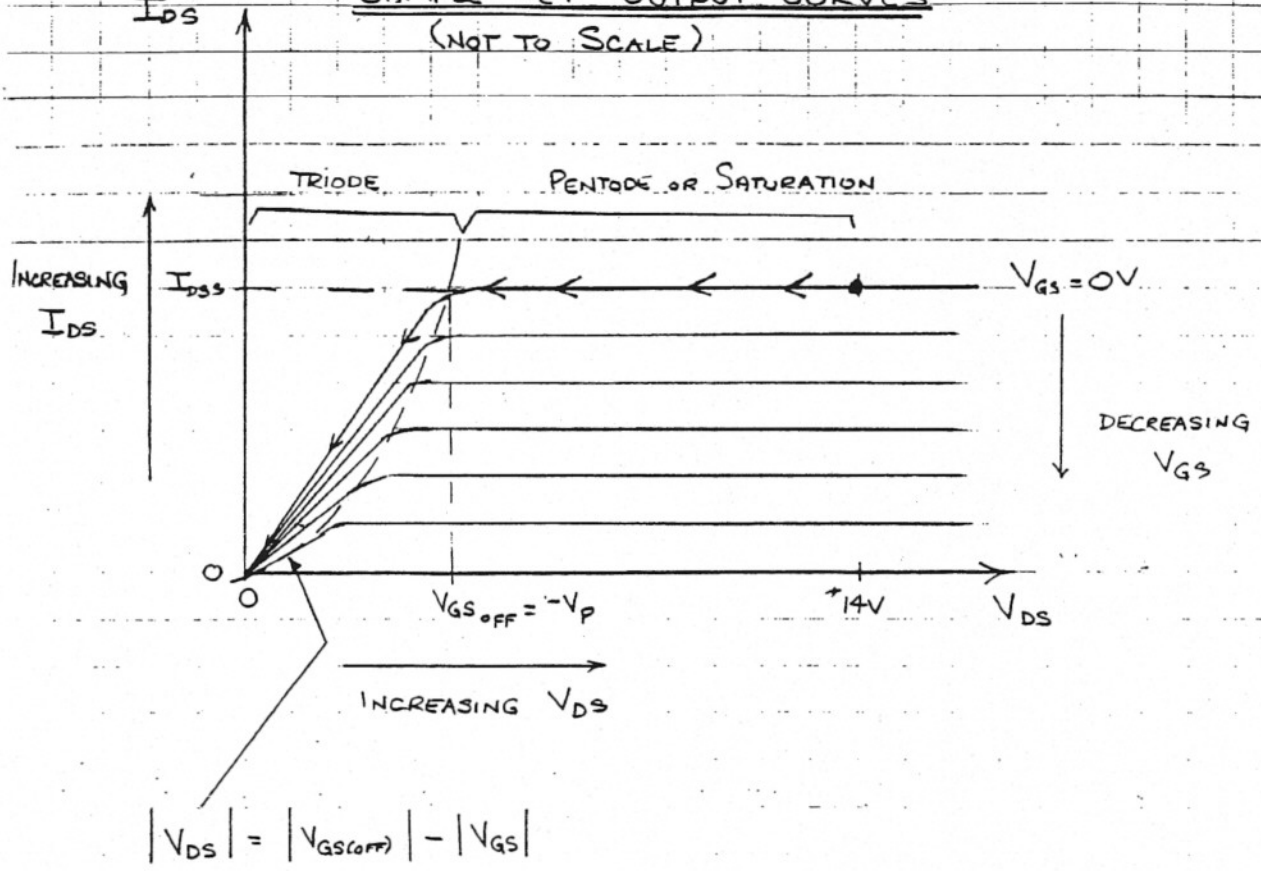


FIGURE 7
a) STEP INPUT
b) PULSE INPUT

APPENDIX A

SAMPLE FET OUTPUT CURVES

(NOT TO SCALE)



NOTES:

1) IN SATURATION REGION, $I_{DS} = I_{DSS}\left(1 + \frac{V_{GS}}{V_{GS_{OFF}}}\right)^2$

2) IN TRIODE REGION, TO FIRST ORDER, THE FET ACTS AS A FIXED, LINEAR RESISTANCE, AND $R_{DS} = V_{DS}/I_{DS}$

3) THE DIVIDING LINE BETWEEN THE REGIONS IS THE CURVE DEFINED BY:

$$|V_{DS}| = |V_{GS_{off}}| - |V_{GS}|$$

4) IF $V_{GS} > 0$, THEN I_{DS} CAN EXCEED I_{DSS}.

APPENDIX B

BURR-BROWN®

3527

NOT RECOMMENDED FOR NEW DESIGNS

Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOWER PRICED
- ULTRA-LOW DRIFT, 2μV/°C, max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 2pA, max
- LOW NOISE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM INTEGRATION
- LOW DROOP SAMPLE/HOLD CIRCUITS
- PRECISION VOLTAGE AMPLIFICATION
- HIGH INPUT RESISTANCE BUFFER

DESCRIPTION

The Burr-Brown 3527 is a precision operational amplifier. It offers excellent performance at moderate cost through the use of hybrid construction, monolithic ICs, matched FETs, thin-film resistors, and active laser trimming.

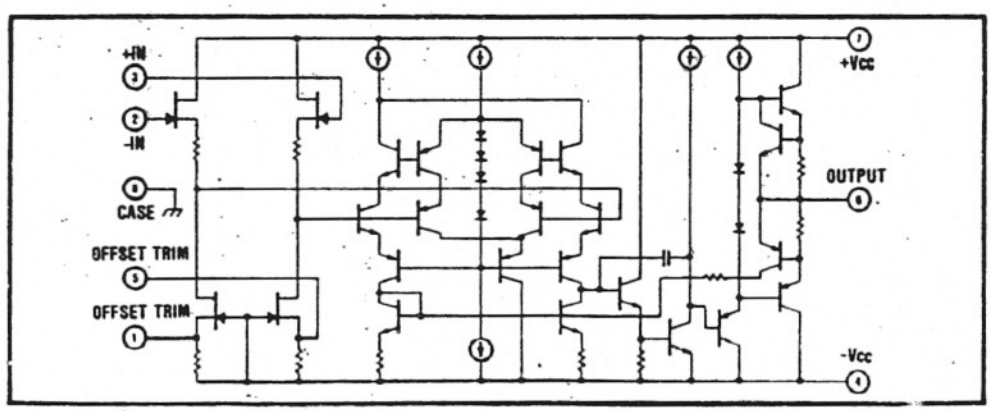
The 3527 low, initial offset voltage (250μV max) allows higher design accuracy at lower installed cost. Costly pots and external nulling of the offset voltage are not required for most applications. Also, higher system reliability is achieved by using fewer parts.

The offset voltage temperature drift of the 3527 is exceptionally low (2μV/°C max) and is compatible with the best bipolar amplifiers (BB3500E). It is achieved by laser adjusting the offset during manufacture and means that high system accuracy is maintained over the temperature range.

The low bias current (guaranteed 2pA max) allows the use of larger feedback resistor values, and smaller bias current errors are realizable.

Of course, all the other desirable features of high quality op amps are engineered into the 3527. It has low input noise, is free from latch up, is short circuit protected for continuous output shorts to common, is internally compensated for unity gain stability, and is pin compatible with 741 amplifiers. Guarding is achieved by the pin 8 case connection.

For increased reliability screening, consult Burr-Brown.



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SPECIFICATIONS

ELECTRICAL

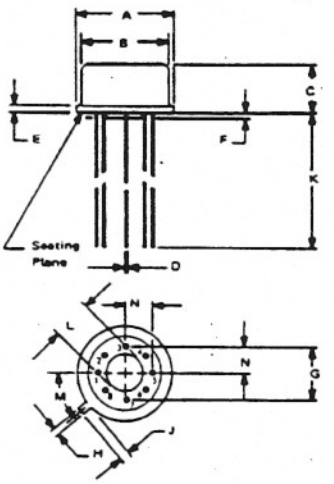
Specifications typical at T_A = 25°C and ±15VDC supplies, unless otherwise noted.

MODELS	3527AM			3527BM			3527CM			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC										
No Load		112			•			•		dB
R_L = 2kΩ	100	108		•	•		•	•		dB
RATED OUTPUT										
Voltage	±10	±12		•	•		•	•		V
Current	±10	±20		•	•		•	•		mA
Output Impedance		600			•			•		Ω
Load Capacitance		1000			•			•		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop		1			•			•		MHz
Full Power Response	10	14		•	•		•	•		kHz
Slew Rate	0.6	0.9		•	•		•	•		V/μsec
Settling Time (0.01%)		45			•			•		μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C		±200	±500		±100	±250		±100	±250	μV
vs. Temp. (-25°C to +85°C)		±5	±10		±2	±5		±1	±2	μV/°C
vs. Supply Voltage		±75			•			•		μV/V
vs. Time		±20			•			•		μV/mo
INPUT BIAS CURRENT										
Initial Bias, 25°C		-2	-5		-0.7	-2		-2	-5	pA
vs. Temp		**			**			**		
vs. Supply Voltage		±5			•			•		pA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C		±0.3			•			•		pA
INPUT IMPEDANCE										
Differential		10^{12}			•			•		Ω
Common-mode		10^{15}			•			•		Ω
INPUT NOISE										
Voltage, f_o = 10Hz		75			•			•		nV/√Hz
f_o = 100Hz		35			•			•		nV/√Hz
f_o = 1kHz		30			•			•		nV/√Hz
f_o = 10kHz		25			•			•		nV/√Hz
0.3Hz to 10Hz, p-p		2.6			•			•		μV
10Hz to 10kHz, rms		3			•			•		μV
Current, 0.3Hz to 10Hz, p-p		15			•			•		fA
10Hz to 10kHz, rms		60			•			•		fA
INPUT VOLTAGE RANGE										
Common-mode Voltage Range		±(|Vs|-3)			•			•		V
Common-mode Rejection at ±10V		76			•			•		dB
Max. Safe Input Voltage		±Vs			•			•		VDC
POWER SUPPLY										
Rated Voltage		±15			•			•		VDC
Voltage Range, derated performance	±5		±20	•		•	•		•	VDC
Current, quiescent		2.6	4		•			•		mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	•		•	•		•	°C
Operating	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C
θ junction-ambient		235			•			•		°C/W

*Specifications same as for 3527AM.
**Doubles every +10°C.

MECHANICAL TO-99 PACKAGE

Order Number: 3527AM, 3527BM, 3527CM Weight: 1 gram



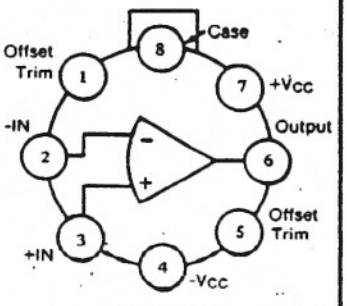
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM



(TOP VIEW)

BURR-BROWN®

OPA602

MILITARY & DIE VERSIONS AVAILABLE

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±250μV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING: 1μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

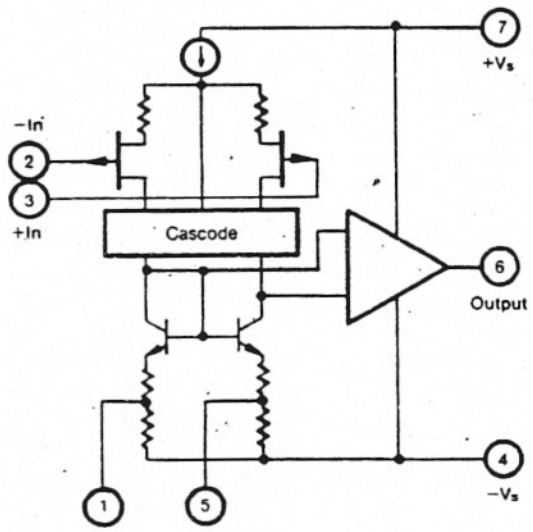
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-753B

SPECIFICATIONS

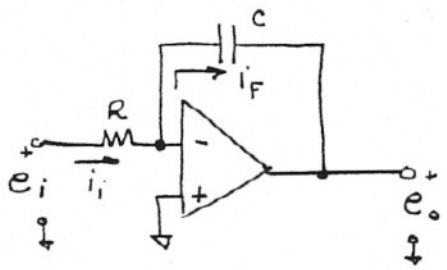
ELECTRICAL

At V_S = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM/AP/AU			OPA602BM/SM/BP			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage: f_O = 10Hz			•			23			•		nV/√Hz
f_O = 100Hz			•			19			•		nV/√Hz
f_O = 1kHz			•			13			•		nV/√Hz
f_O = 10kHz			•			12			•		nV/√Hz
f_B = 10Hz to 10kHz			•			1.4			•		µVrms
f_B = 0.1Hz to 10Hz			•			0.95			•		µVp-p
Current: f_B = 0.1Hz to 10Hz			•			12			•		fAp-p
f_O = 0.1Hz to 20kHz			•			0.6			•		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage:											
"M" Package	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	µV
"P" Package			1	2		0.5	1				mV
"U" Package			1	3							mV
Over Specified Temp:											
"M" Package			±550			±250	±1000		±200	±500	µV
"P", "U" Packages			±1.5			±0.75	±1.5				mV
Average Drift	T_A = T_{MIN} to T_{MAX}		•	±15		±3	±5		•	±2	µV/°C
Supply Rejection	$±V_S$ = 12V to 18V	70	•		80	100		86	•		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temp.			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC	1	10		0.5	2		0.5	1	pA	
Over Specified Temp.			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			•			10^{13}‖1			•		Ω‖pF
Common-Mode			•			10^{14}‖3			•		Ω‖pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		•	•		±10.2	+13, −11		•	•		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	•		88	100		92	•		dB
OPEN LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 1kΩ	75	•		88	100		92	•		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3.5	•		4	6.5		5	•		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		•			570			•		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	•		24	35		28	•		V/µs
Settling Time: 0.1%	Gain = −1, R_L = 1kΩ		•			0.6			•		µs
0.01%	C_L = 500pF, 10V step		•			1.0			•		µs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	•		±11.5	+12.9, −13.8			•	•	V
Current Output	V_O = ±10VDC	•	•		±15	±20		•	•		mA
Output Resistance	1MHz, open loop		•			80			•		Ω
Load Capacitance Stability	Gain = +1		•			1500			•		pF
Short Circuit Current		±25	•		±30	±50		•	•		mA
POWER SUPPLY											
Rated Voltage			•			±15			•		VDC
Voltage Range, Derated Performance		•		•	±5		±18	•		•	VDC
Current, Quiescent	I_O = 0mADC		•	•		3	4		•	•	mA
Over Specified Temp.			•	•		3.5	4.5		•	•	mA
TEMPERATURE RANGE											
Specification	Ambient temp.	•		•	−25		+85	•		•	°C
SM Grade					−55		+125				°C
Operating: "M" Package	Ambient temp.	•		•	−55		+125	•		•	°C
"P", "U" Packages		−25		+85	−25		+85				°C
Storage: "M" Package	Ambient temp.	•		•	−65		+150	•		•	°C
"P", "U" Packages		−40		+125	−40		+125				°C
θ Junction-Ambient			•			200			•		°C/W

*Specification same as OPA602BM

OP-AMP INTEGRATOR FREQ. RESPONSE:



1) $V_o(s) = A_o(s)\,(V^+(s) - V^-(s))$; s = LAPLACE VARIABLE; $A_o(s)$ = OPEN LOOP GAIN

2) $V^+(s) \triangleq 0$

3) $V_o(s) = -A_o(s)\,V^-(s)$

4) KCL @ V^- NODE: $i_i = i_F$

5) $\dfrac{V_{i(s)} - V^-(s)}{R} = [V^-(s) - V_o(s)]\,sC$

6) $V_i(s) - V^-(s) = [V^-(s) - V_o(s)]\,sCR$

6A) $V_i(s) + V_o(s)\cdot sCR = V^-(s)\,[1+sCR]$

USING (3) INTO (6A):

7) $V_i(s) + V_o(s)\,sCR = \dfrac{V_o(s)}{-A_o(s)}\,[1+sCR]$

$-A_o(s)\,[V_i(s) + V_o(s)\,sCR] = V_o(s)\,[1+sCR]$

$-A_o(s)\,[1 + A_{CL}(s)\,sCR] = A_{CL}(s)\,[1+sCR]$; $A_{CL}(s) = \dfrac{V_o(s)}{V_i(s)}$

$-A_o(s) = +A_o(s)\cdot A_{CL}(s)\cdot sCR + A_{CL}(s)\,[1+sCR]$

$-A_o(s) = A_{CL}(s)\,[A_o(s)\cdot sCR + 1 + sCR]$

8) $\dfrac{-A_o(s)}{A_o(s)\,sCR + sCR + 1} = A_{CL}(s)$

9) $A_o(s) \triangleq \frac{N_A(s)}{D_A(s)} = \frac{A_o(1 + s/s_{z_1})}{\prod_{i=1}^{j} (1 + s/s_{p_i})}$; A_o = DC OPEN LOOP GAIN
s_{z_1} = ZERO LOCATION
s_{p_j} = POLE LOCATIONS

COMBINE 8 & 9

$$A_{CL}(s) = \frac{-\frac{A_o(1 + s/s_{z_1})}{D_A(s)}}{\frac{A_o(1 + s/s_{z_1})}{D_A(s)} \cdot sCR + sCR + 1}$$

$$A_{CL}(s) = \frac{-A_o(1 + s/s_{z_1})}{A_o(1 + s/s_{z_1}) \cdot sCR + (sCR + 1) D_A(s)}$$

let $s = j\omega$

$$A_{CL}(\omega) = \frac{-A_o(1 + j\omega/\omega_{z_1})}{A_o(1 + j\omega/\omega_{z_1}) \cdot j\omega CR + (j\omega CR + 1) D_A(\omega)} = \frac{N_{A_{CL}}(\omega)}{D_{A_{CL}}(\omega)}$$

$$\therefore |A_{CL}(\omega)|_{dB} = +20 \text{Log} |A_o(1 + j\omega/\omega_{z_1})| - 20 \text{Log} |D_{A_{CL}}(\omega)| .$$

FROM EQUATION 10 IT CAN BE DETERMINED WHICH FREQUENCIES ARE INTEGRATED AND WHICH ARE "LOW PASS FILTERED". ALSO, THE DEPENDENCE OF THE CLOSED LOOP GAIN ON THE DC OPEN LOOP GAIN IS CLEAR. FINALLY, THE CLOSED LOOP GAIN CAN BE DETERMINED ALSO INCLUDING THE EFFECTS OF THE OP AMP OPEN LOOP POLES AND ZEROES.

APPENDIX D

2N4416 SERIES
N-Channel JFETs

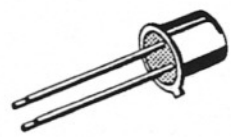
Siliconix incorporated

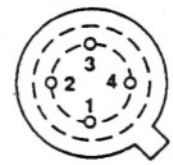
The 2N4416 and 2N4416A are n-channel JFETs designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise figure (4 dB max @ 400 MHz), high gain (10 dB min @ 400 MHz) and provide wide bandwidth. Its TO-72 hermetically sealed package is available with full military processing. (See Section 1.)

For additional design information please see performance curves NH.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4416	-6	-30	4.5	15
2N4416A	-6	-35	4.5	15

TO-72 (TO-206AF) BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 CASE

SIMILAR PRODUCTS

- TO-92, See J304 Series
- SOT-23, See SST4416
- Chips, See NH Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS 2N4416	LIMITS 2N4416A	UNITS
Gate-Drain Voltage	V_{GD}	-30	-35	V
Gate-Source Voltage	V_{GS}	-30	-35	
Gate Current	I_G	10		mA
Power Dissipation	P_D	300		mW
Power Derating		1.7		mW/°C
Operating Junction Temperature Range	T_J	-55 to 150		°C
Storage Temperature Range	T_{stg}	-65 to 200		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300		

SPECIFICATIONS[a]			LIMITS					
				2N4416		2N4416A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-36	-30		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-3		-6	-2.5	-6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	5	15	5	15	mA
Drain Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[d]	I_G	V_{DG} = 10 V, I_D = 1 mA	-20					pA
Drain Cutoff Current[d]	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2					
Drain-Source On-Resistance[d]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150					Ω
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance[c]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz	6	4.5	7.5	4.5	7.5	mS
Common-Source Output Conductance[c]	g_{os}		15		50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz	2.2		4		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		0.8		0.8	
Common-Source Output Capacitance	C_{oss}		1		2		2	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$
HIGH-FREQUENCY								
				100 MHZ		400 MHZ		
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V			100		1000	µS
Common-Source Input Susceptance	b_{iss}				2500		10,000	
Common-Source Output Capacitance	g_{oss}				75		100	
Common-Source Output Susceptance	b_{oss}				1000		4000	
Common-Source Forward Transconductance	g_{fs}					4000		
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 5 mA		18		10		dB
Noise Figure	NF	R_G = 1 kΩ			2		4	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
d. This parameter not registered with JEDEC.

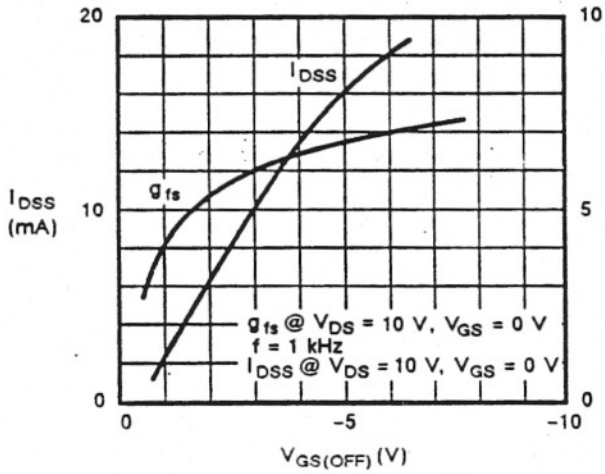
NH
N-Channel JFETs

Siliconix incorporated

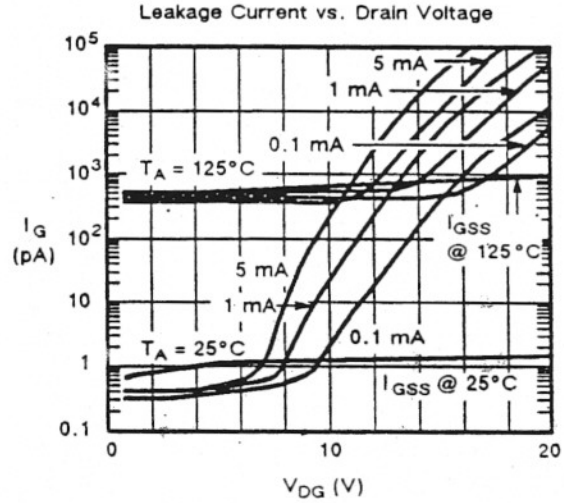
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• 2N5484, 2N5485, 2N5486 J304, J305
Single	SOT-23	• SST4416
Single	TO-72 (TO-206AF)	• 2N4416, 2N4416A
Single	Chip	• Available as NH1CHP, NH2CHP, NH3CHP

TYPICAL CHARACTERISTICS

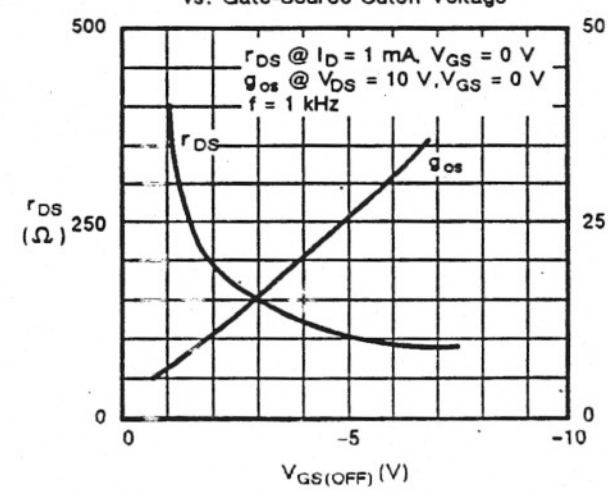
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



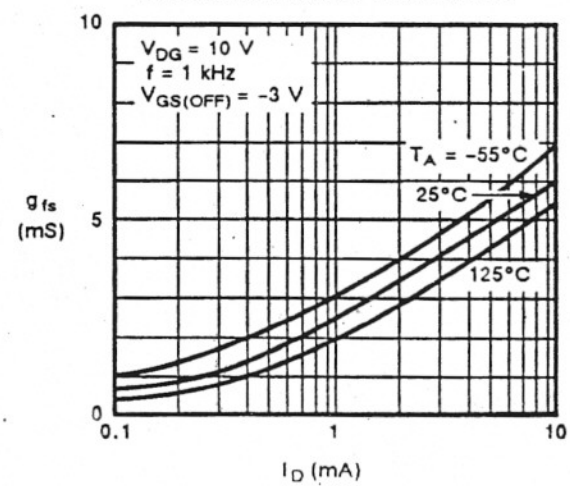
Leakage Current vs. Drain Voltage



On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



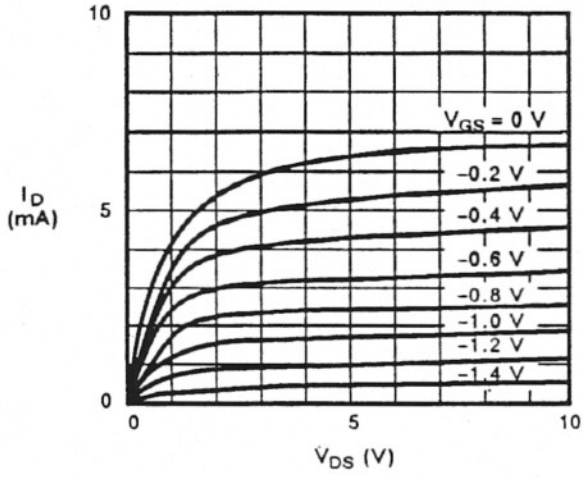
Common-Source Forward Transconductance vs. Drain Current



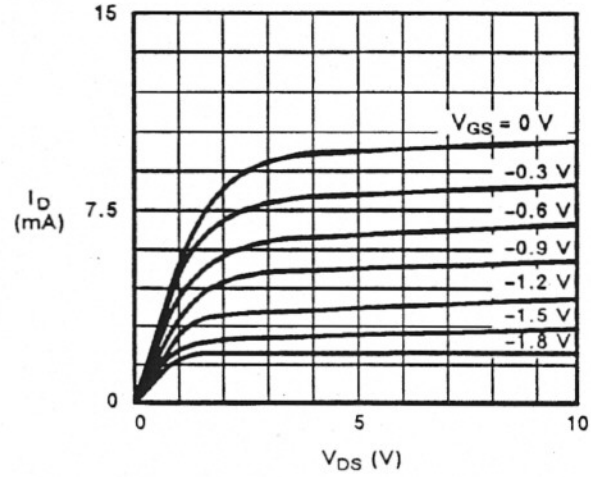
Revised (02/11/91)

TYPICAL CHARACTERISTICS (Cont'd)

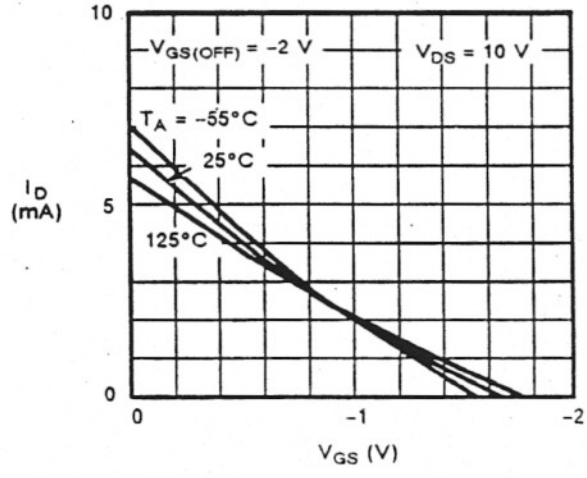
Output Characteristics ($V_{GS(OFF)} = -2$ V)



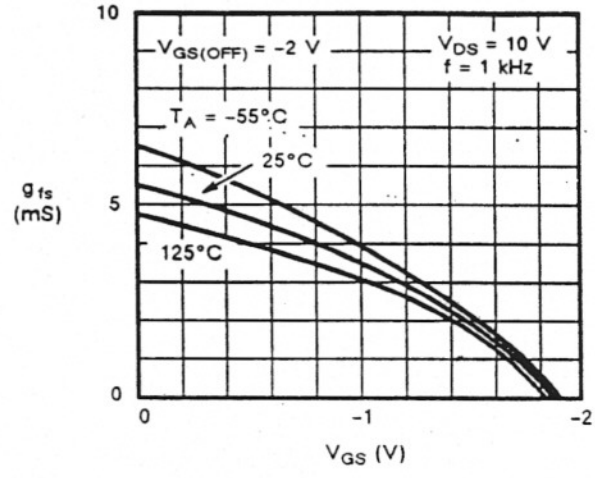
Output Characteristics ($V_{GS(OFF)} = -3$V)



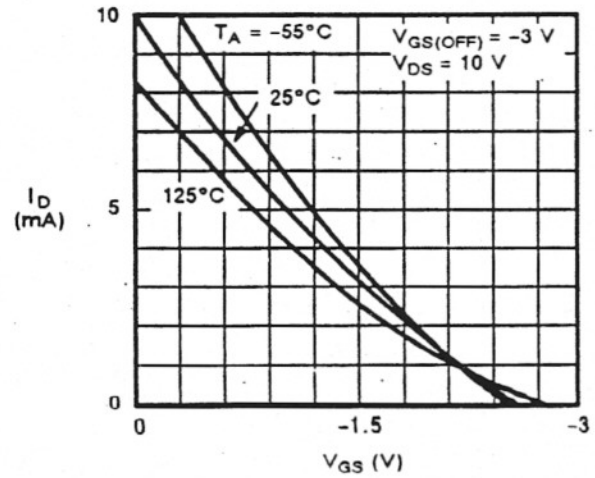
Transfer Characteristics



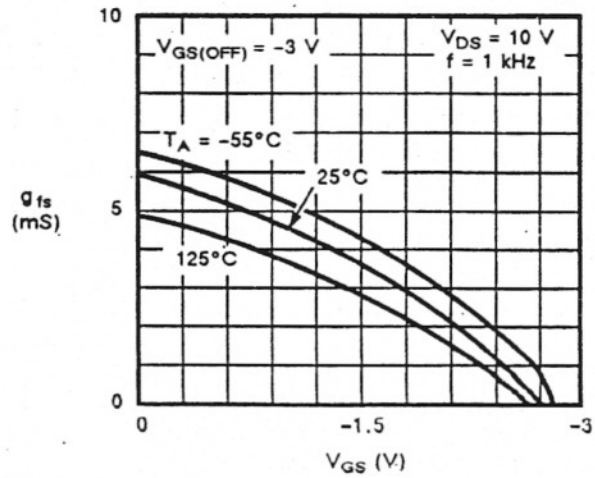
Transconductance vs. Gate-Source Voltage



Transfer Characteristics



Transconductance vs. Gate-Source Voltage



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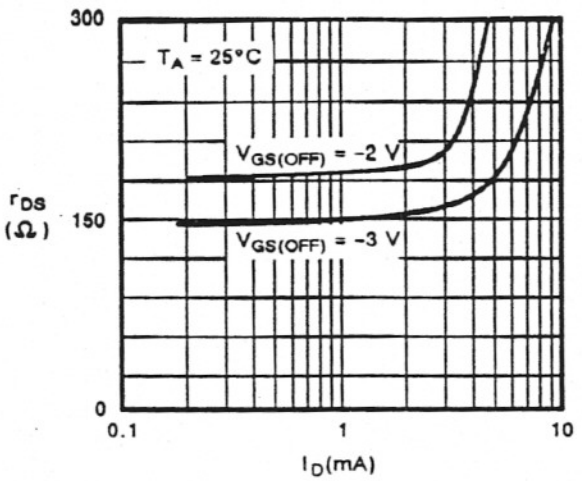
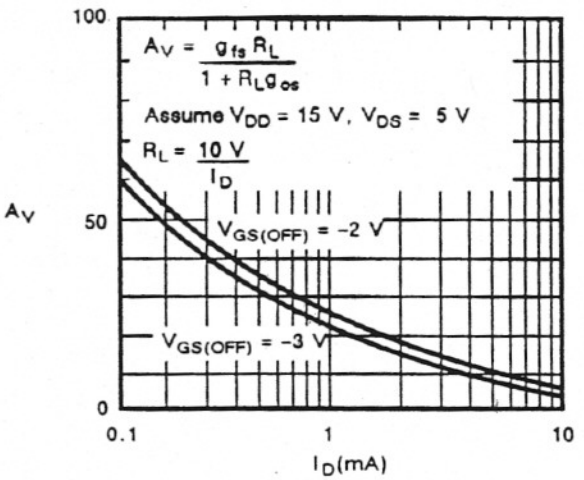
TYPICAL CHARACTERISTICS (Cont'd)

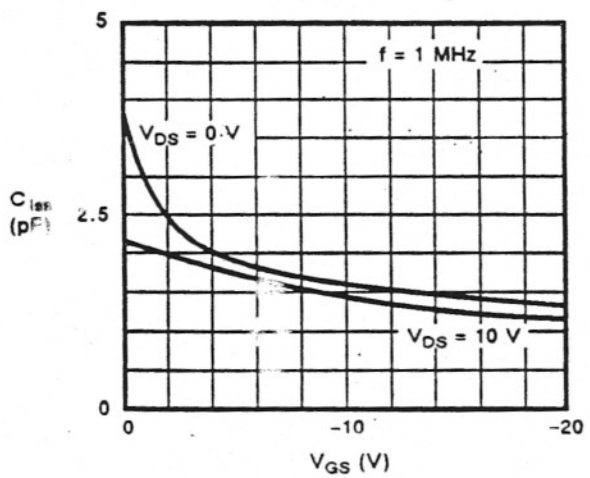
On-Resistance vs. Drain Current



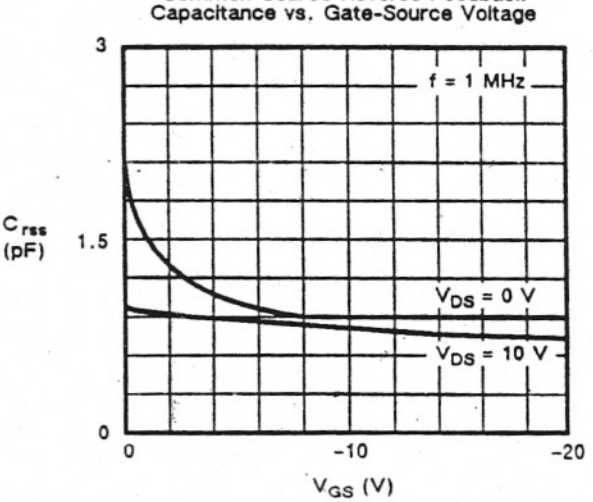
Circuit Voltage Gain vs. Drain Current



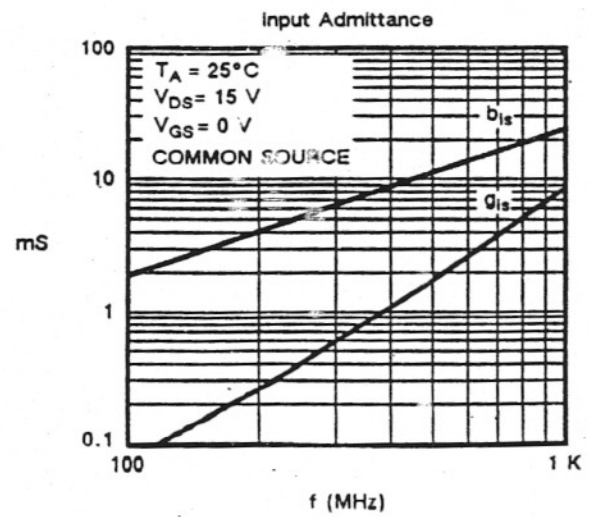
Common-Source Input Capacitance vs. Gate-Source Voltage



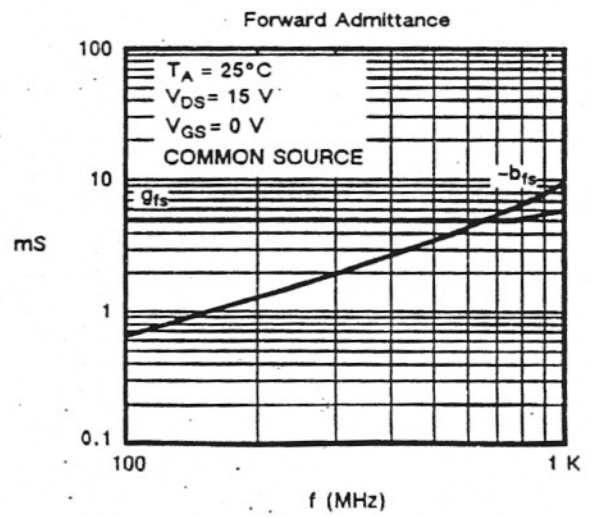
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Input Admittance

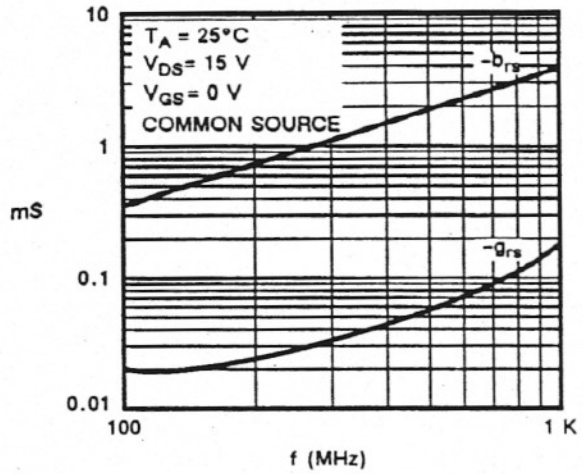


Forward Admittance

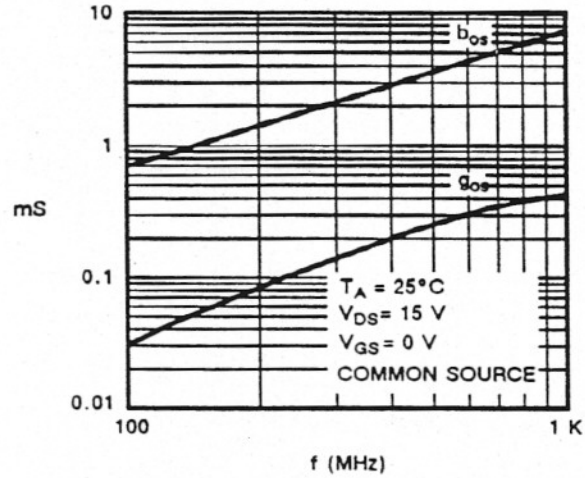


TYPICAL CHARACTERISTICS (Cont'd)

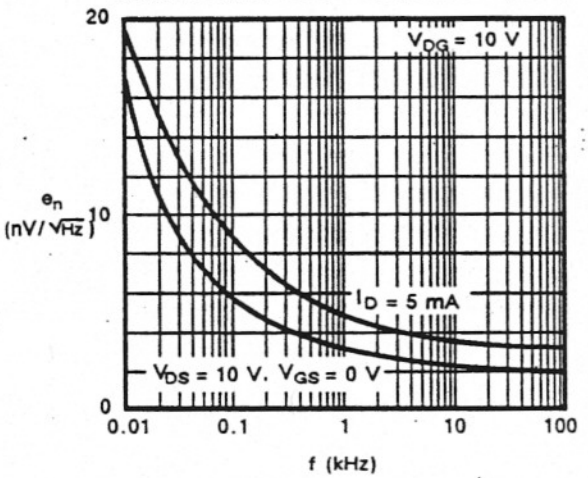
Reverse Admittance



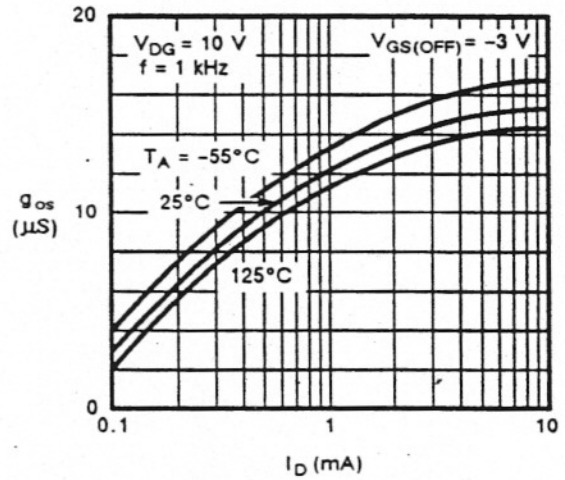
Output Admittance



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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