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Energy Recovery Linac: Low Level RF

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INTRODUCTION

A superconducting RF (SRF) Energy Recovery Linac (ERL) is currently under development at the Collider-Accelerator Department (C-AD) at Brookhaven National Laboratoyr (BNL). The major components from an RF perspective are a) a 5-cell SRF ERL cavity, b) an SRF photocathode electron gun, and c) a drive laser for the photocathode gun. Each of these RF subsystems has its own set of RF performance requirements, as well as common requirements for ensuring correct synchronism between them. A low level RF (LLRF) control system is currently under development, which seeks to leverage both technology and experience gained from the recently commissioned RHIC LLRF system upgrade. This note will review the LLRF system requirements and describe the system to be installed at the ERL.

LLRF SYSTEM REQUIREMENTS

The system parameters for the 5-cell cavity, gun and laser are summarized below.

Table 1: 5-Cell Cavity Parameters

PARAMETER	VALUE	UNITS
Single Pass Energy Gain	20	MeV
Peak Stored Energy	226	J
RF Frequency	703.74	MHz
Maximum Bunch Frequency	9.383	MHz
RHIC RF Revolution Harmonic	9000	
RHIC RF Bunch Harmonic	75	(for 120 bunches)
R/Q (Circuit Definition)	200	ohm
Q BCS @ 2K	4.5E10	
Qext	3.0E7	
Maximum Available PA Power	50	kW
Total System Delay	1	us
Lorentz Detuning Coef	1.2	Hz / (MV/m)^2
Lorentz Detuning	480	Hz
Lowest Mechanical Resonance	100	Hz
Mechanical Q	1000	
Longitudinal Loss Factor (k)	0.45	V / pC

Table 2: RF Gun Parameters

PARAMETER	VALUE	UNITS
Peak Stored Energy	8.37	J
Beam Kinetic Energy	2	MeV
RF Frequency	703.74	MHz
Maximum Bunch Frequency	9.383	MHz
Maximum Bunch Charge	50	nC
Maximum Current	469	mA
R/Q	54	ohm
Qext	39.5E3	
Maximum Available PA Power	1.5	MW
Longitudinal Loss Factor (k)	0.7	V / pC

Table 3: Laser RF Parameters

PARAMETER	VALUE	UNITS
Master RF Repetition Rate	703.74	MHz
Pulse Repetition Frequency	9.383	MHz
Frequency Tunability	+/- 1	MHz
Maximum Integrated Jitter	1	Ps (rms)
Average Output Power Stability	1	% (rms)
Pre-Pulse and Post_pulse Pedestals	< 0.5	% (within 100ps)

Some definitions follow for completeness:

$$\frac{R}{Q} = \sqrt{\frac{L}{C}} = \frac{V^2}{2\omega_0 U}$$

$$Q = \frac{\omega_0 U}{P} = \omega_0 RC = \frac{R}{\omega_0 L}$$

$$k = \frac{\omega_0}{2}\frac{R}{Q}$$

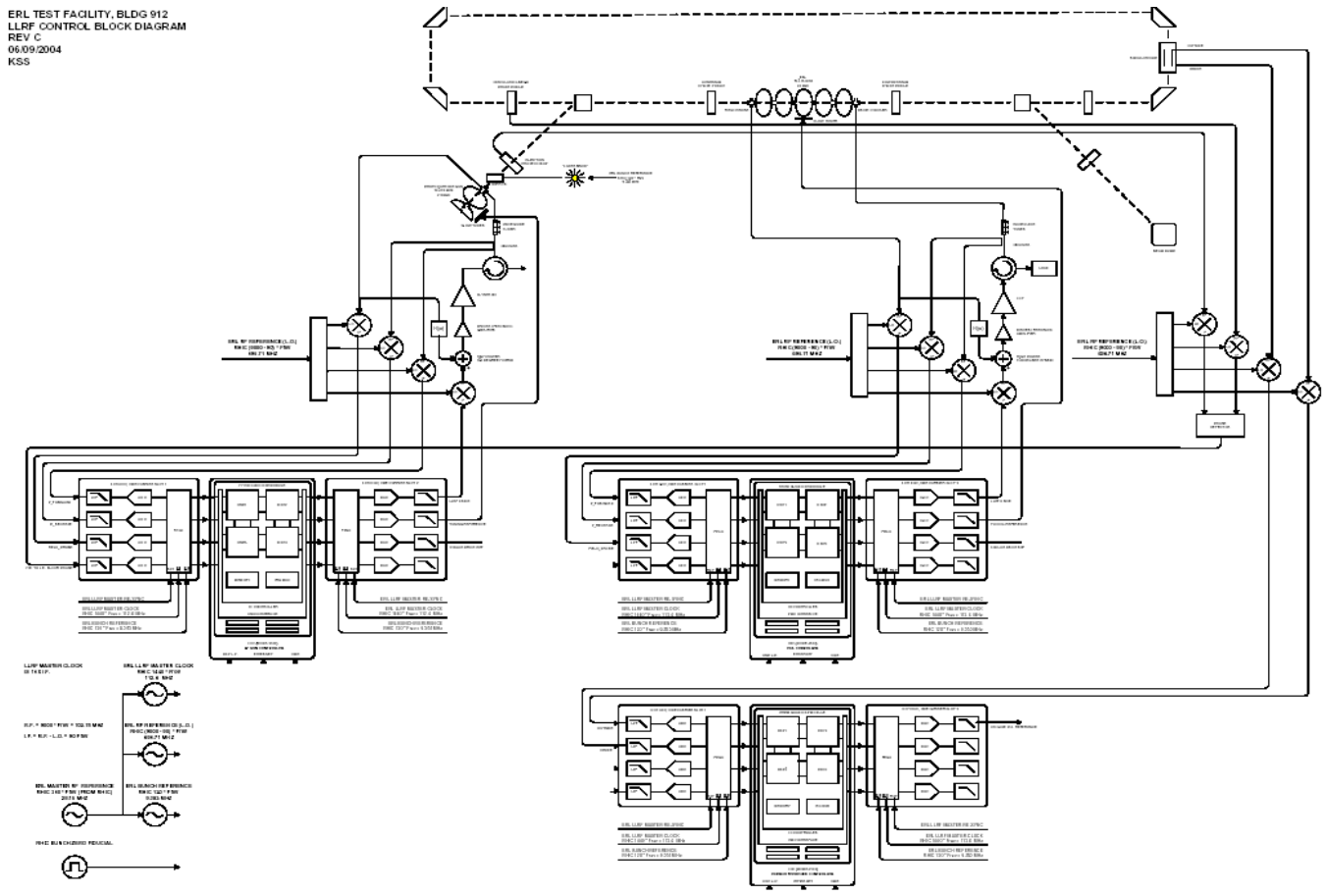
In order to satisfy all possible demands on the RF systems, the original simulations and resulting design parameters were based on the high current operation with 50nC per bunch at a 9.383 MHz bunch frequency, which leads to the 469 mA average current of Table 2. For the RF gun, this requires a power delivered to the beam of 938 kW, and Q = Qext for the RF gun of 39.5E3. The simulation is detailed elsewhere [1]. The simulation assumes that given the low beam loaded Q of the RF gun, adequate

control can be readily achieved for nominal operating conditions. The simulation focused on control of the 5-cell cavity, operating at a loaded Q of 3.0E7, with a dominant mechanical oscillation mode at 1kHz chosen to produce an rms frequency modulation of 5Hz, or about 0.5 loaded cavity bandwidths. Under those conditions, the maximum required PA power was 18 kW and the maximum energy deviation was 70eV or a fractional energy error of about 1.4E-6. The simulation assumed a PI loop with 2us delay, and 16 bit resolution of the digitized cavity voltage (field probe).

LLRF SYSTEM DESCRIPTION

The low level RF system for the R&D ERL (5-cell cavity, RF gun and laser) will be a variant of a newly designed digital LLRF controller platform, recently commissioned during the RHIC Run 10 start-up, and soon to be commissioned at the Electron Beam Ion Source (EBIS) – the next generation heavy ion injector for the RHIC complex. The concept and implementation of the generic system has been described elsewhere in some detail [2,3,4]. A block diagram of the R&D ERL LLRF system is shown in Figure 1.

Figure 1: R&D ERL Low Level RF Block Diagram



The central component of the LLRF hardware is a chassis referred to as a “controller” [Figure 2, 3]. . Essentially a controller is a powerful, flexible, software/firmware configurable digital signal processing platform, adaptable to many tasks. A controller consists of a “carrier” board together with up to six associated “daughter” mezzanine modules [Figure 4] which attach to the carrier via an IEEE standard XMC interface. The carrier serves as a stand-alone network attached control system interface, host platform for the daughter mezzanine modules, communication hub and diagnostic data acquisition engine. Daughter modules provide system specific functionality and signal processing horsepower – an example being a 4CH ADC board used to digitize RF signals from a cavity. All boards are custom designed at BNL, based on a common powerful Field Programmable Gate Array (FPGA) family, the Xilinx Virtex-5 FX devices

Figure 2: The LLRF Controller

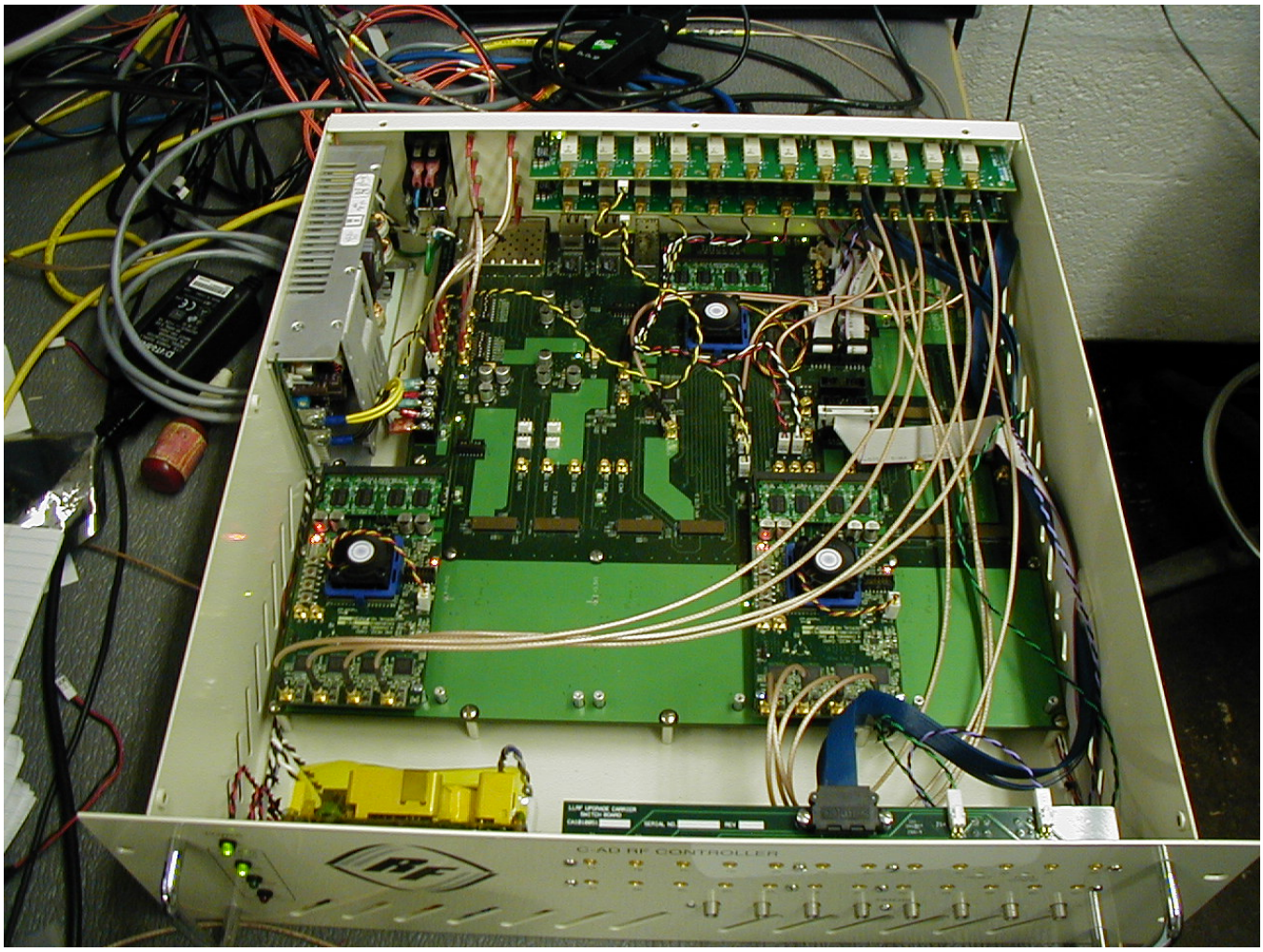


Figure 3: Controller Block Diagram

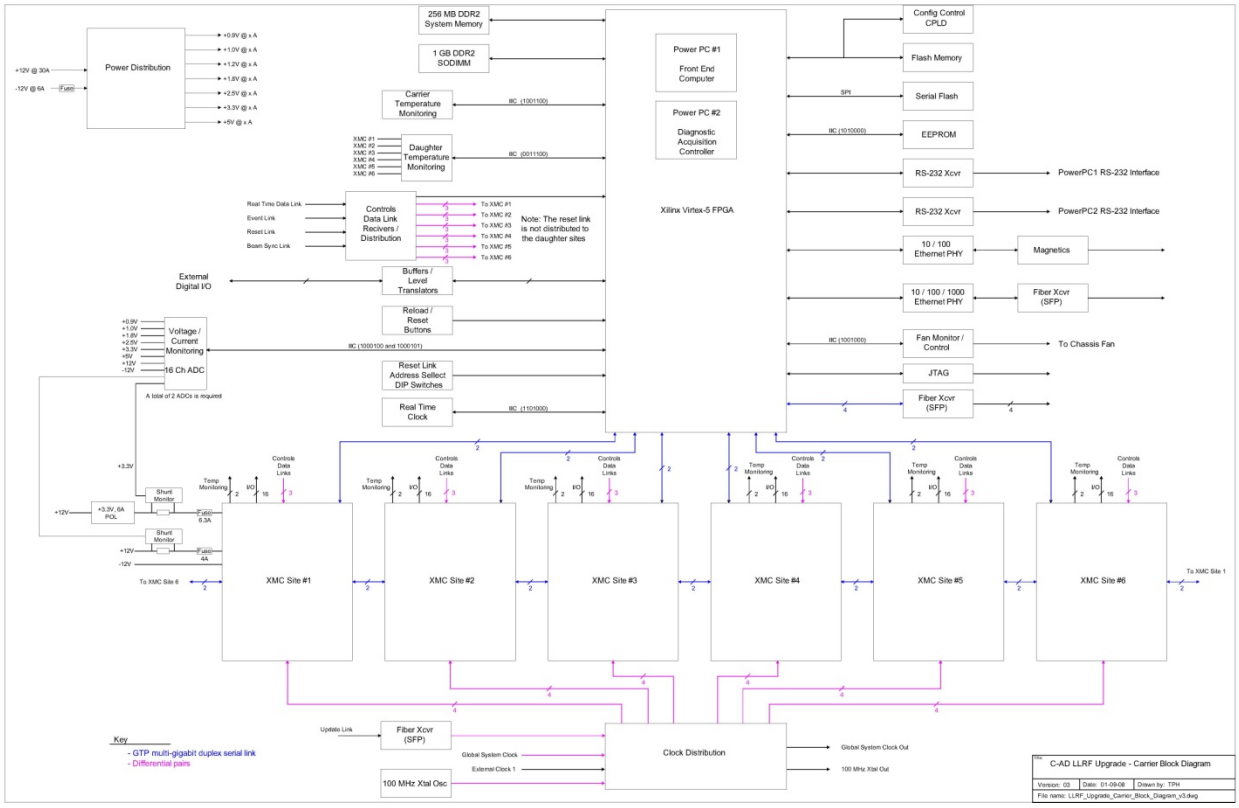
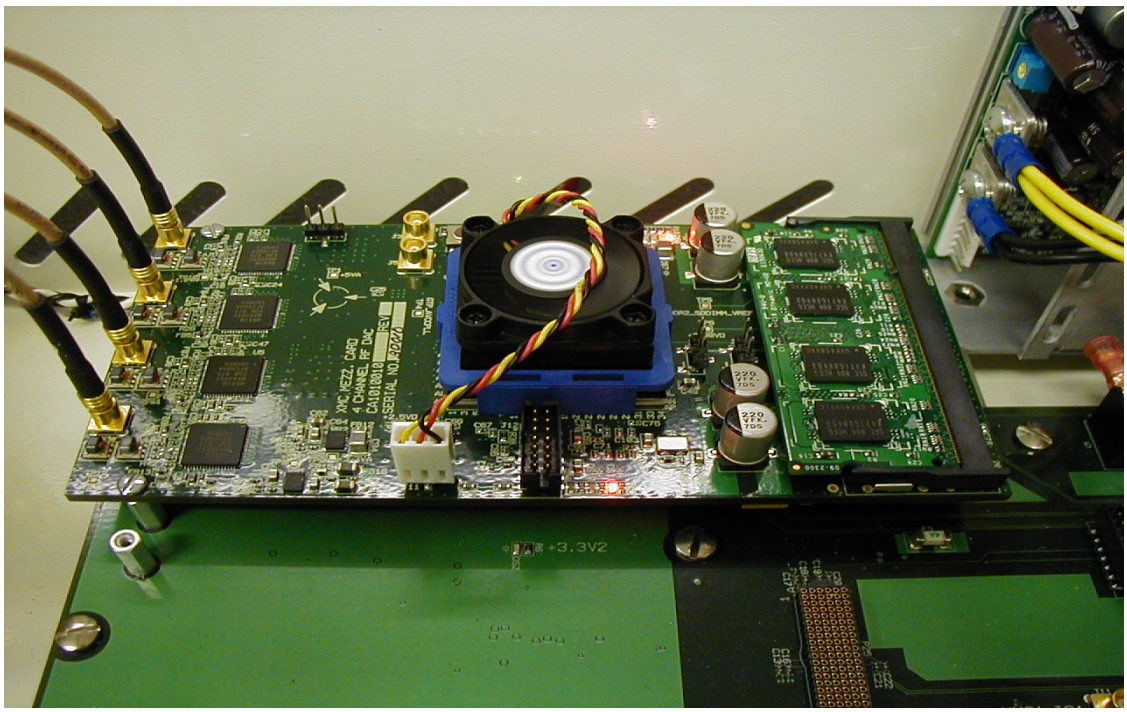


Figure 4: Daughter Mezzanine Module (4CH RF DAC)



The Virtex-5 FX FPGA family provides a number of very powerful resources. Depending on the specific version used, there are either one or two hard core PPC processors available. 16 multi-gigabit serial transceivers provide very high bandwidth communication, and even deterministic data links as needed. Hardware "DSP Slices" provide very high speed signal processing functionality. Large arrays of programmable logic and static RAM, high speed low jitter clock generation and distribution, very large IO pin count, support for numerous single ended and differential IO standards, and relatively low power dissipation complete a feature list which we exploit to the fullest.

For the R&D ERL, two of these controllers will be integrated into a LLRF control system. Only half of the available daughter sites in each chassis are planned to be populated to implement the system, leaving ample capacity for future expansion or reconfiguration of the system. To provide ultra low noise LLRF signal processing with absolute synchronism (phase lock) across multiple controllers and daughter modules, the system relies on two key components.

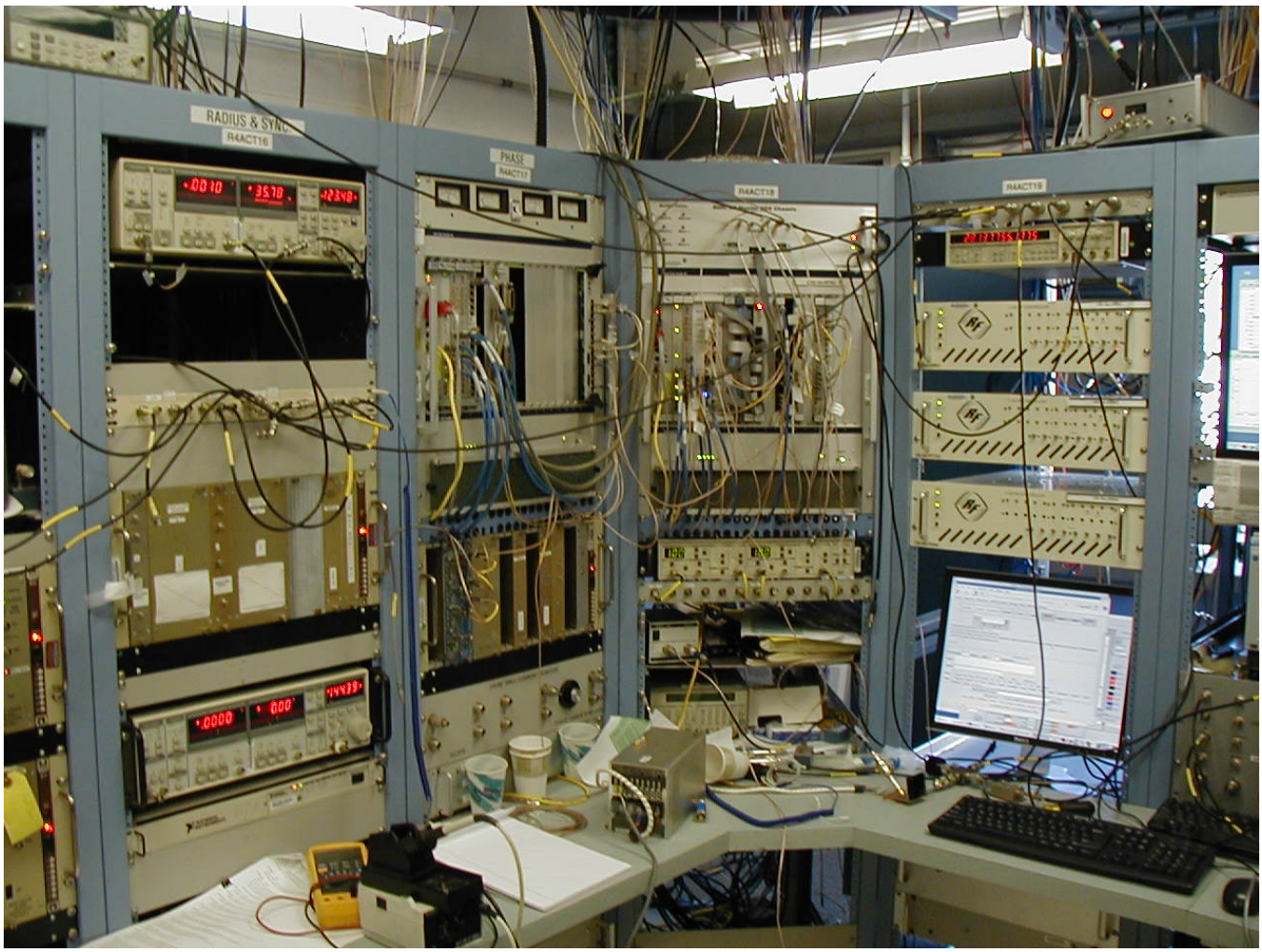
First, an ultra low noise 100MHz master clock is distributed to both chassis, and within, to the carriers and daughter modules. This clock has a typical integrated phase noise of <100 fs rms in a 1Hz to 100kHz bandwidth (BW 1-100k). This clock is distributed within the controllers via high speed differential PECL fanouts, and on each daughter is used as a reference clock for a 1600MHz PLL. This PLL provides a variety of divided output clocks for on board DACs, ADCs, FPGAs, etc., with a typical integrated phase noise of about 140fs rms (BW 1-100k). The RF DACs used to provide RF drive signals produce carrier signals with phase noise of 170fs to 200fs rms (BW 1-100k), when clocked at 400 MSPS.

Second, a multi-gigabit serial link referred to as the "Update Link" and employing the same 100 MHz master clock as a reference, provides a deterministic timing in the form of an encoded "Update Pulse" event occurring every 1000 clock cycles, or at a 100kHz "Update Rate". This Update Pulse is decoded locally at every carrier and daughter module providing deterministic timing across the system. The Update Link also broadcasts global event and data packets, which if desired can maintain a fixed timing relationship to the Update Pulse via pre-assigned "slotting" within an Update Period. An example of this would be a "Master Reset" event, used to deterministically reset all RF synthesizers to known reference phases.

The combination of these permits a complete LLRF system to be built up from the requisite number of chassis and daughter modules, while ensuring that all sub-components can maintain the desired RF phase relationships. Although the R&D ERL LLRF System has not yet been integrated and installed, the recently commissioned RHIC LLRF System [Figure 5], and our LLRF lab development systems, provide a functioning proof of principle platform. In the RHIC system, a total of five LLRF Controllers are integrated into a single system – two providing LLRF for the "Blue" ring, two for the "Yellow" ring, and 1 serving as the Update Link master chassis. This system provides RF synthesis for 16 RF cavities at 28MHz (h=360) and 197MHz (h=2520), 2 "beam synchronous" timing systems at h=360, machine to machine synchronization clocks at h=0.25, h=1, and h=19, and so on. All systems must maintain a fixed

phase relationship (across both rings), including over the RHIC acceleration ramp where the 28MHz sweeps over about 120kHz. In addition, because of the very long beam store times (up to 8 hours), the RF must exhibit ultra low noise in order to minimize longitudinal emittance growth. Performance to date has been excellent.

Figure 5: RHIC LLRF System (Controller Chassis are the three identical chassis, far right, above the LCD display terminal)



While much of the R&D ERL LLRF is conceptually similar to RHIC, the system specific parameters and requirements must be accommodated. Many issues remain to be fully investigated, but none are expected to be show stoppers at this time. The most obvious of these is the ERL fundamental RF frequency of 703.75 MHz. The plan for 703.75 MHz operation is to employ standard up and down conversion techniques to convert the ERL 703.75 MHz to/from some readily managed IF frequency, probably 40MHz or lower. Some testing of the RF synthesizers has been done, using the first image

tone for the 703.75 MHz signal. Phase noise results were very promising. With or without heterodyning, system phase and amplitude stability requirements (nominally 0.1% and 0.1 deg rms at 703.75 MHz) imply careful attention will need to be paid to stabilizing cabling and components against drift sources – primarily temperature. It is expected that much useful knowledge can be gained from the RHIC stochastic cooling efforts currently underway, where system bandwidths span 4GHz to 8GHz and beyond, with stringent phase and gain stability requirements.

The laser reference requirements appear to be well within the already proven capabilities of the platform. Remaining to be addressed are particular implementation details concerning how to handle the various desired gating and ramping requirements.

REFERENCES (TO BE COMPLETED)

[1] M. Blaskiewicz, RHIC Electron Cooling ZDR

[2] KSS, LLRF Workshoop 2005 Paper

[3] KSS, LLRF Workshop 2007 Paper

[4] FFS, ICALEPS Paper