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The SEB/HITL four-channel gated integrator

G. A. Smith

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BROOKHAVEN NATIONAL LABORATORY
Associated Universities, Inc.
Upton, New York 11973

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THE SEB/HITL FOUR-CHANNEL GATED INTEGRATOR

INTRODUCTION

For many years the 4-channel integrator module has been used around the AGS as a charge integrator for loss monitors, SWICS, SEC's, and other types of beam detectors. Many variations of the module are in use, all of which are similar in function (i.e., they perform charge integration) but differ in such details as gain, input/output connections, gating requirements, and even basic performance parameters like leakage current. These variations have been the result of modifications intended to improve the device performance and to adapt the unit to new requirements.

Recently, large numbers of new modules have been constructed for HITL and the SEB. This, along with just plain good economic and operational common sense, has prompted the development of a standard module which can be easily adapted to both areas. This paper describes the resulting design from its basic operation to its more aesthetic details, as well as such things as testing, adjustments and troubleshooting.

BASIC OPERATION

Figure 1 shows, in simplified form, a schematic of one channel of the gated integrator. The amplifier and the capacitor perform the integration; the FET's (S1 through S3) act simply as switches which control the integration interval and reset the circuit.

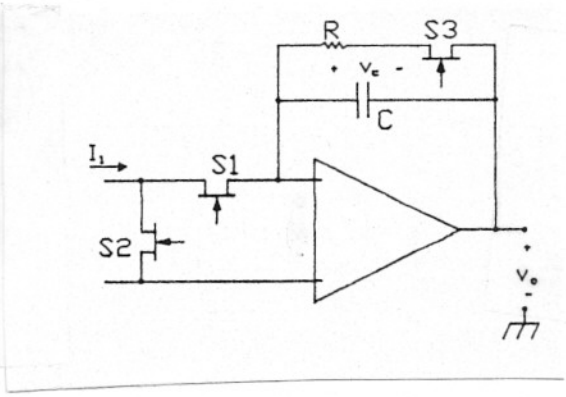

Fig. 1. Simplified Integrator Schematic

The circuit is initialized by momentarily closing S3; this discharges the capacitor, C. The resistor is needed to limit the current during that time, but its presence sets a lower limit to the discharge time. Immediately following this initialization period called reset, the integrator output voltage will be zero and will remain at zero until current flows into the amplifier input through S1. S1 and S2 compliment each other (i.e. S2 is closed only when S1 is open and vice versa) so that the current I1 is shunted to ground when it is not being integrated.

With S1 closed, the amplifier output is:

$$V_o = - 1/C \int i_1 dt = - Q/C$$

which is to say that the circuit literally adds up (or integrates) all of the charge that flows into its input and produces an output voltage equal to the voltage that would exist if that amount of charge were stored on capacitor C (except the polarity is reversed).

SOME CONSIDERATIONS

In real life, with real integrators, there are limits to the performance of the ideal circuit discussed above. One of the principal limits in design is caused by the tiny but inevitably present leakage currents that flow to the input terminal of the amplifier. These currents can come from a variety of sources including amplifier bias current and resistive paths to voltage sources physically near to the input terminal. These currents create a drift in the output voltage of the integrator which is not related to the signal and so constitutes an error. The magnitude of these currents, usually a few picoamperes, can vary significantly depending on whether S1 is open or closed. They set a lower limit to the detectable signal and since they are often temperature or even humidity dependent, they are difficult to predict or compensate for.

Another source of difficulty arises from the gating of the integrator. Due to the presence of parasitic coupling from the gate to both the source and drain of the FET's, small amounts of charge inevitably get

coupled into the amplifier input during the fast leading and trailing edges of the gating pulses. These parasitically coupled charges cause offsets in the output voltage and are another source of error. In the Four-Channel Integrator this problem is partially compensated for by intentionally coupling a small amount of charge to the input from the complement of the gate drive signal. Figure 2 shows how this is done. R1, C1 and R2 constitute the reset pulse compensation circuit; C2 and R3 form the integrate/hold compensation. For each channel, R2 and R3 must be adjusted to produce the correct results. This adjustment is discussed later.

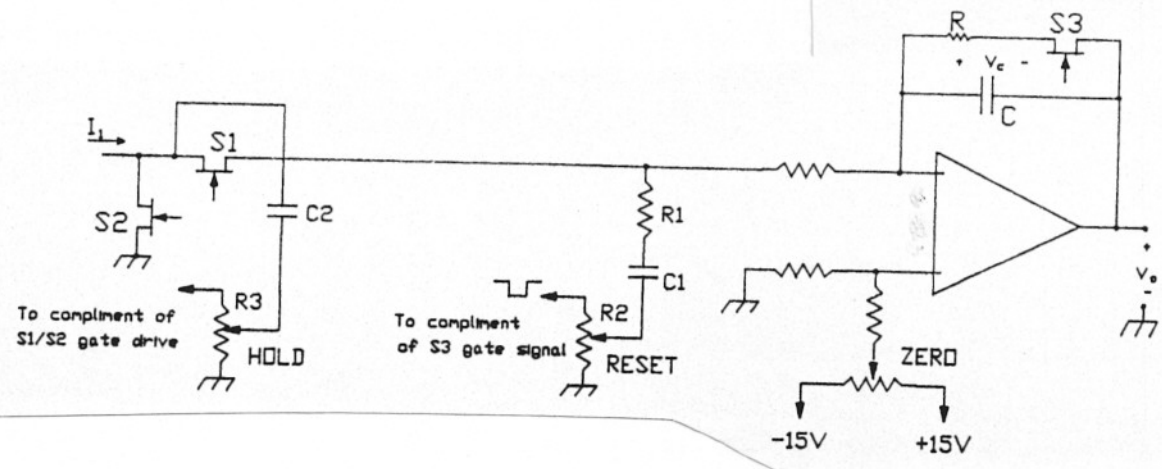

Fig. 2. Simplified schematic showing gating compensation and Zero adjustment

Still another practical reality that has caused problems comes from the presence of the small, but still considerable, offset voltage inherent in the op amp. When the device is driven from a low impedance source such as an amplifier, any offset voltage present at the input tends to cause current to flow into the source impedance. This creates yet another potential source of drift which occurs during the integrate time. To eliminate this, a so-called "zero" adjustment has been provided.

THE DEVICE (MECHANICALLY)

Appendix A of this report lists the pertinent drawings and documents for both of the current versions. The information is filed under AGS Job No. D32-1E3.

The circuit is laid out on a printed circuit card which is about 9 in. by 7.25 in. and mounted in a single width NIM module. The cards for both versions are identical. All connections to the card are made through the standard NIM connector on the back of the module to wire wrap pins on the card (see section on variations below). It must be noted that no attempt has been made to use the NIM standard with regard to pin functions. These modules must never be inserted into a bin which has not been specifically wired to accept them.

The two versions have similar, but not identical front panels. Input and Output jacks are provided on both panels as test points for each channel. These are not intended to be used as connections to any device. LED's indicate the status of the gating at any time and are intended as visual diagnostic aids. However, the "zero" adjustment is missing on the SEB unit. Actually the adjustment still exists; the potentiometer is just not accessible from the front panel in the SEB version. To make the adjustment correctly actually requires special knowledge of the unit and its application (see section on adjustments). To prevent casual use by uninformed personnel, it was decided to prevent access from the front in this unit.

THE DEVICE (ELECTRICALLY)

The schematic for the most recent version of the Four-Channel Integrator is D32-E11-5F. This drawing, while labeled HITL 4-CHANNEL INTEGRATOR does in fact double as the schematic of the SEB version as well.

The two versions differ in two ways, both associated with gating. In the HITL unit, TTL pulses drive the gates; in the SEB unit, additional components are added to allow the reset, integrate and hold inputs to be driven by predet pulses which can be + 15V or higher. The second difference is that the SEB unit is automatically placed in the integrate mode by the reset pulse. It can be switched back and forth from integrate to hold as often as required without resetting, but it is always put into integrate upon resetting. The HITL version on the other hand, simply remains in whatever mode it was in prior to reset.

The integrator uses a Burr-Brown 3527BM Low Bias current, FET input, and operational amplifier (U2, U4, U6, U8 on the drawing). This device has a 2 pa maximum bias current which makes it a suitable choice for most

applications. With a constant leakage current of this amount, an integrator with 1000 pF capacitor would "drift" linearly 2 mV over 1 sec. The layout for this amplifier on the printed card is very critical. Jumpers E5-E6, E7-E8 in channel 1 are wires which bridge out on both sides of the board to completely enclose the input terminals of the operational amplifier, shielding the input from any possible leakage cross the surface of the board from higher potential points.

It is worthwhile noting that leakage can be, and in fact is, different in integrate than in hold. The PAD 5's (the 5 stands for the maximum leakage current in pa) for example can contribute significantly more than the amplifier to drifting which occurs when in the integrate mode. This can be an important factor when the device is to be used in applications where long integration times are needed..

There are two integrating capacitors in each channel and a relay which allows the selection of one, or the parallel combination of the two. This provides a remote "gain" selection for each module by driving the gain input line (TTL level). As with gating, gain selection applies to the entire module, not individual channels.

Some care needs to be taken in the selection of integrating capacitors. They must be high quality, low leakage, stable parts with a basic tolerance equal to that required in the application. The integrator accuracy can be no better than that of the capacitor. In the SEB and HITL units, dipped Mica capacitors with ± 1% tolerance are used.

OPTIONS

Four-Channel Integrators are used with a variety of different sources and input currents can vary by orders of magnitude. To provide flexibility in handling these differing requirements, the choice of the capacitor is left as an option. However, in exercising this option, the user must be aware of several pitfalls. Too low a capacitor value can result in the leakage current completely dominating the results. This design has been used with values as low as 22 pF, but it is recommended that with capacitors less than 180 pF the user assure himself that the result will be what he expects.

On the high end, the circuit has not been used in an application requiring more than 10,000 pF, although it can function with up to .47

uf. For all cases there is the additional necessity of allowing sufficient discharge time for the capacitor during reset. Reset time is controlled by one half of the on-board SN74123, U11. Components R92 and C25 set the actual reset pulse width. Applications vary in the amount of time available for reset and so the value of C25 is in a sense also optional. A good rule of thumb, however, is that the minimum value of C25 must equal or exceed the value of the integrator capacitor. The minimum value of C25 in common usage is 4700 pF. This is equivalent to a 10 µsec reset time.

ADJUSTMENTS

Three adjustments are provided for each channel of the integrator. These are called RESET, HOLD, and ZERO. RESET and HOLD are the gating compensation adjustments and ZERO is the offset voltage compensation pot. In actually performing these adjustments, it is necessary to simulate the actual gating, and most important, the input conditions with which the module will be used. Two examples of this will be given below.

The RESET adjustment controls the amount of charge which gets coupled from both the leading and trailing edges of the reset gate (see Fig. 2). Because S3 is on during the reset time, the effect of the leading edge is nullified. Some charge is coupled to C during the trailing edge, however, since S3 is turning off at that time. R3 can be adjusted to give zero offset in the output just after reset.

The HOLD adjustment controls the amount of charge coupled onto C as the channel is switched into both integrate and hold modes. Because the states of S1 and S2 are different during the hold to integrate--integrate to hold transitions, differing amounts of charge get coupled to C during these times and so the adjustment allows the change in level from integrate to hold to be made zero.

What is supplied here are two controls to compensate for three transitions. In all cases this will not always be enough, but for the most common uses, i.e. a single reset/integrate/hold sequence each cycle, these will suffice.

The ZERO adjustment is another story. Its function is to provide an offset voltage equal to but of opposite polarity to the amplifier bias voltage in the special case where the channel is driven by a low

impedance device such as a beam transformer or an amplifier. In its present form it is useful only over integration periods of several hundred microseconds. Beyond that, instabilities not yet well understood ruin its effectiveness. Ordinarily it will be adjusted by grounding the input and adjusting the control for a Zero slope during the integration period.

The ZERO adjustment is ineffective when the source is a high impedance (greater than 10^{10} ohms) device such as a SWIC or Loss Monitor.

VARIATIONS

It seems appropriate at this point to mention that the two versions of the Four-Channel Integrator described above are the result of an overhaul of a nearly identical device formally titled the Slow Beam 4-Channel Gated Integrator (see AGS Dwg. D11-E510-5A). This older version is worth mentioning because it performs the same function as the new version although not quite as well, and because large numbers of them are still used on the AGS floor.

First is should be pointed out emphatically that these are not compatible devices. The pinouts on the rear NIM connector are not the same. In fact, only power and gating signals are brought through the connector on the older unit and then not all the same pins. Insulated BNL connectors are mounted on the front panel for signal input and optional K-LOC connectors electrically in parallel with these are mounted on the rear above the NIM connector. K-LOC's are also provided on the rear for the gating signals.

On the card there are differences in the way the gating compensation is derived, but the intention is the same and the RESET and HOLD adjustments are made to achieve the same results as above. In this unit, it will be noted that the reset pulse always puts the integrator into integrate mode and it is common to find that the hold input is not used.

In the drawing the gating pulses are shown optically isolated by MCT-2 isolators. This technique, while good for the larger pulses generated by most Predets, did not work reliably for the lower level TTL pulses and so a large number of units have been fitted with a transistor circuit similar to the one in the newer version.

APPENDIX A

HITL/SEB 4-CHANNEL GATED INTEGRATOR DRAWINGS

(See Job No. D32-1E3)

	SEB	HITL
Schematic Diagram	D32-E11-5F	Same
P.C. Board Artwork	D32-E12-4E	Same
P.C. Board Drilling	D32-E13-4E	Same
P.C. Board Assembly	D32-E14-4E	Same
F.P. Drilling/Silkscreen	D11-E801-3	D32-E15-3
NIM Bin Module Assembly	D11-E802-3	D32-M1184-4

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