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PRELIMINARY SYSTEM SPECIFICATION FOR THE AGS LOSS MONITOR UPGRADE

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Technical Note

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Introduction:

This document is to serve as a vehicle for communication concerning the feature set for the upgraded AGS Loss Monitor system (RLRM). As the target hardware is still under development this document will remain fluid, and open dialog between the design groups is recommended and appreciated.

The intent of the AIP RLRM is to directly replace the existing RLRM system with a new system with some enhanced capabilities. The system design has been developed considering operational experience with the Booster Loss Monitor System (BLM)[1].

System Concept Overview :

The intent of the loss monitor system is as a *monitoring* system. As such, no interlocking or primary safety functions for machine or personnel are assigned to this system. The data measured by the RLRM during the machine cycle are the losses over specified user specified time intervals, called "windows". The window widths are bounded below by the data acquisition system scan time (approximately 2 ms) and above by the slowest rep rate of the machine (about 5 seconds). The windows are specified by a pair of times referred to as window start and window stop times. Up to 16 windows for each machine cycle can be specified. Adjacent windows can be placed no closer than the integrator reset time (20 us). Windows are not allowed to overlap. During the time outside the windows in a machine cycle, the loss monitor system will not take data.

The data collected is the accumulated charge from each detector. The charge is accumulated using analog integrators. The system is designed so that all the integrators share common control signals, and as such independent channel control is impossible. The integrator outputs are digitized by a VME-based data acquisition system, to a resolution of better than 12 bits, at the end of each window. Along with the loss measurements, the circulating beam monitor (CBM) readings are recorded. To insure that only the losses during a window are measured, the integrators are reset to their baselines during non-window times. The integrators remain in the reset mode until the next window occurs.

Further, because integrator output is limited to about +10 V, beyond which no further loss can be accumulated, the control software will include a threshold detection or limit check feature. For this feature, the user will be supplied the capability to specify a separate software limit for each channel in each window for each of the two gain settings. When channels surpass their limit in a particular window they are recorded in a list. At the end of a machine cycle the list of the channels is presented to the user. The list displayed to the user includes the channel name/number, the window, the limit, and the readback. Using this data, the user can shorten

specific windows to get better data and avoid saturation of the electronics. This feature can also be used to detect channels that go above certain tolerable limits at certain times automatically, without visually scanning an entire display. This might be useful during machine tuning or studies. Further, this feature can be enhanced to alarm the user or logging task when a channel seems "dead" or constantly reading full-scale. As mentioned, in addition to the single user of the system, there is a background logging task available. The logging task can only be executed when no one else is using the system. The logging task has all the parameters for data collection preset, and becomes active when the user closes the RLRM application.

In addition to the windowing and threshold detection mentioned above, the control hardware and software will support :

- changing the integrator gain between HI and LO values
- scanning and reporting system status bits
- controlling the 256x8 mux
- providing integrator mode controls (timing signals)
- formatting high level displays

Any system configuration changes such as mux connections, integrator gains, window placement, etc. will only occur at each T0.

"High-Level" Software and Displays

The minimum displays available to the user include, a timeline with the windows clearly marked, a numerical summary of the individual channel readings for a selected window, and a graphical display of the losses for each channel around the ring for a given window. Further, numerical and graphical displays of the total loss for each channel for all the measurement times should be available. It would be advantageous to allow the user to group channels together to summarize losses without viewing individual channels. For example, grouping the superperiods together would be useful. Included on graphical plots or numerical summaries are the values of CBMs, a time stamp/pulse number, and system gain. Other useful summary information desired will be supplied by operations personnel. Also a display of the system status bits is required.

A requirement of the high-level code is to make control of the system simple and intuitive to operate. One requirement is to be able to normalize the loss data to the CBM readings. This should be an option to toggle on and off. Further the ability to average several cycles together would be of use. This way the same time windows are applied for N cycles, and an average loss and variance are computed and displayed numerically or graphically. Another requirement is the ability to tag channels as malfunctioning should a channel be determined as non-functioning. Also an offset and drift acquisition routine will be required for both engineering test and operations. Acquiring the offset and drift will allow baseline correction to be enabled in software. The actual algorithms will be specified in an engineering software tech note. However, this requirement is no different from what is planned for the ATR transfer line loss monitor system. Other requirements will be set by the operations personnel.

System Hardware Overview

Currently, 160 analog electronics channels are planned for, however, the system is designed to provide up to 256 analog channels should the need arise. The channel allocation has channels 1-120 assigned to the detectors mounted on the dipoles with the remaining 40 channels as uncommitted and are termed "expansion channels". The expansion channels can be used to deploy ancillary monitors on an "as-needed" basis, to improve spatial resolution on loss measurements or as temporary back-ups for malfunctioning electronics channels in the base 120.

The hardware block diagram is shown in figure 1. Each channel has a detector (argon filled Andrews Heliax) biased at nominally +200 VDC using in-line floating DC power supplies. The output current from each detector is accumulated by gated analog integrators. The integrator output voltage is directly proportional to the charge measured over the gate time. The integrator data is acquired using a VME-based data acquisition system configured with simultaneous sample and hold (S/H) amplifiers, one or more multiplexed analog-to-digital converters (MADCs), and optically isolated digital I/O. The optical isolation interface options are shown in figure 2. Since the present requirement is for only 160 channels, only that number of S/H channels will be supplied at commissioning, however the system must be expandable to up to 256 channels. The 256 total includes the CBMs unless they are accessible from another high-level application. The design of the data acquisition system is expected to closely mimic the RHIC designs. The integrator outputs can be viewed in the MCR using the 256x8 mux.

Channel Nomenclature

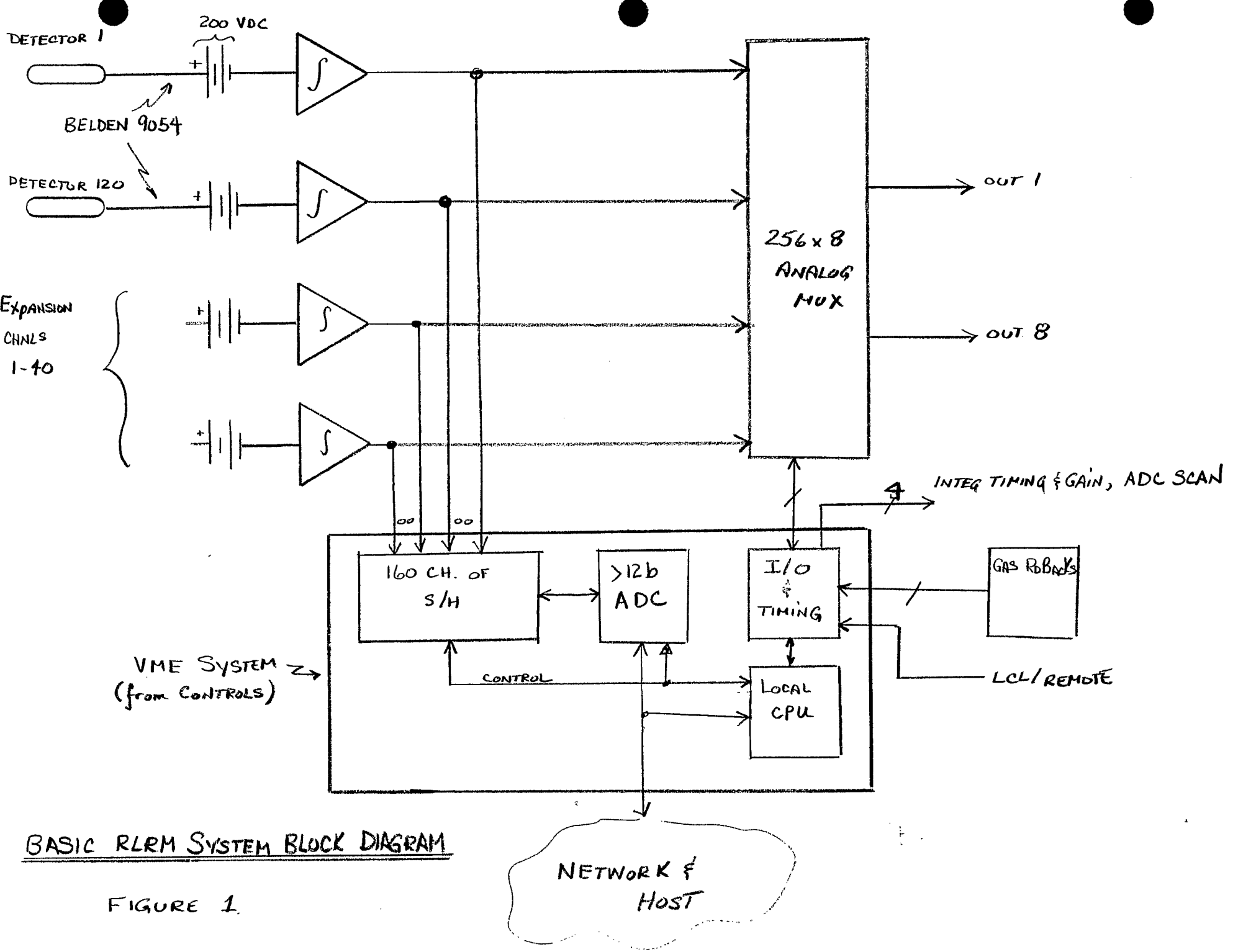
Given past operational experience the 160 channels should be referred to by their logical function and not by the physical location of the detector. This is because as a system matures the initial channel functionality and physical location pairings are often altered. Therefore the signals are to be called simply "channels" 1-120, which are intend to be connected to the existing 120 long loss monitors, and channels 121-160 will be termed as "expansion channels" 1-40.

Gas System

The gas system will be similar in construction to the BLM. That is the ring will be divided in several sections, each with its own gas supply from a pressurized bottle. The bottles will be regulated down to 10 psig and the pressure will be sensed and monitored so the user can be sure of proper system pressure at all times. A benefit of segmenting the gas system is the reduction in time required for purging the system when a detector is replaced.

Detector Design and Mounting

The detector is a coaxial ion chamber made from lengths of RG 318/U Heliax cable , pressurized to approximately 10 psig with an Argon-CO2 mixture. The detectors are nominally two dipoles in length and mounted on the girder below the median plane. Movement up to the median plane would increase the system sensitivity, but may hinder convenient access to the beam



BASIC RLRM SYSTEM BLOCK DIAGRAM

FIGURE 1.

Interfacing For Control & Timing I/O & ADC

Control Line Outputs

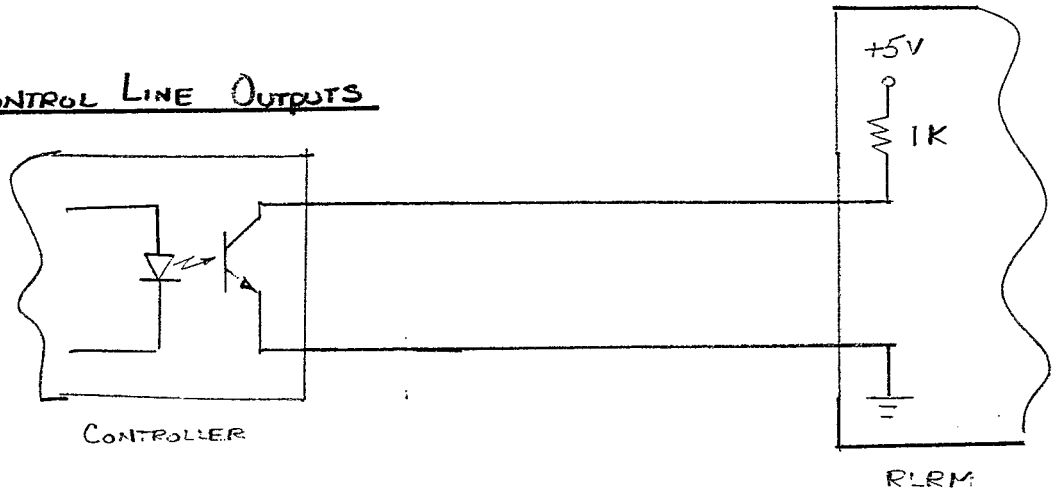
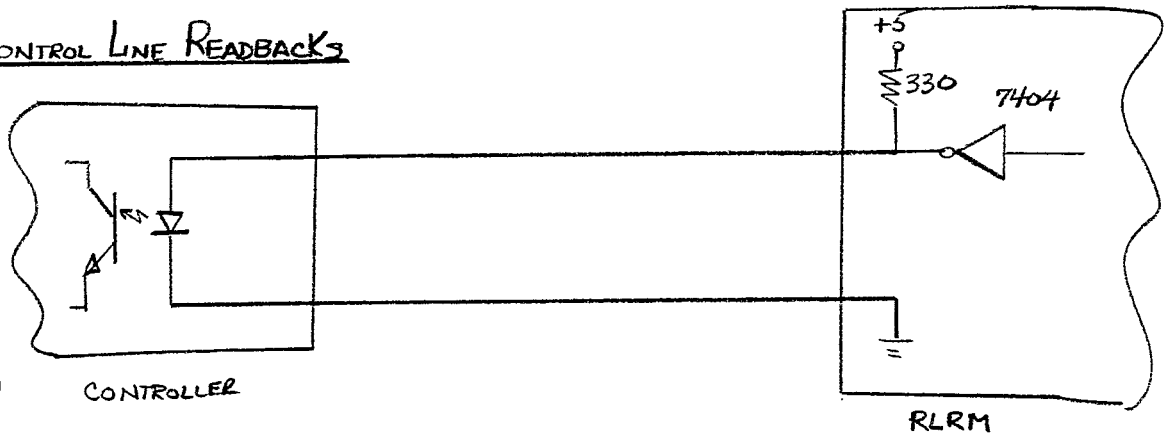
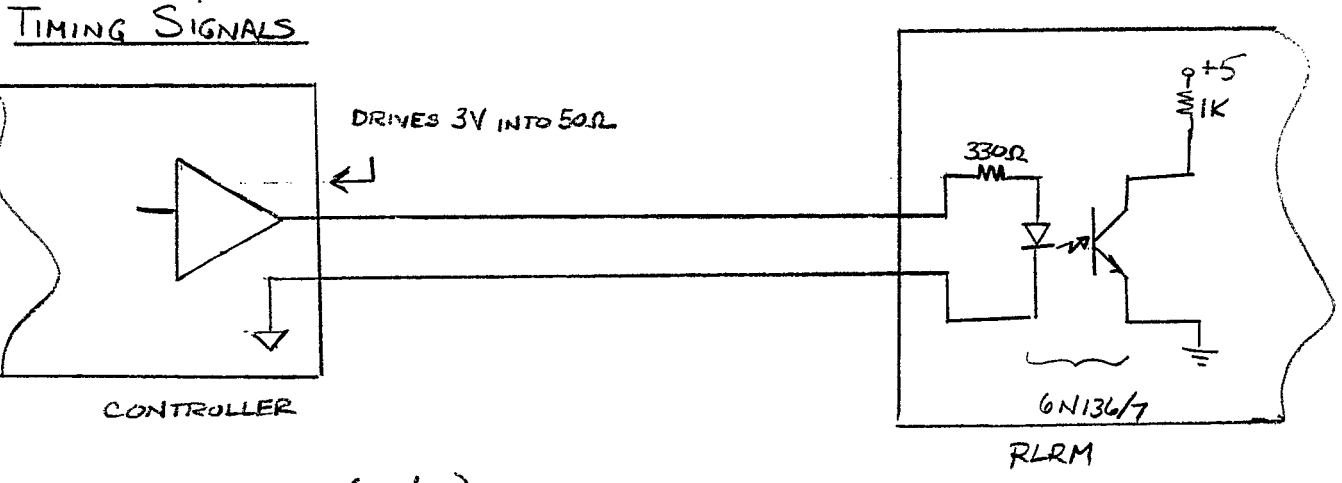


FIGURE 2.

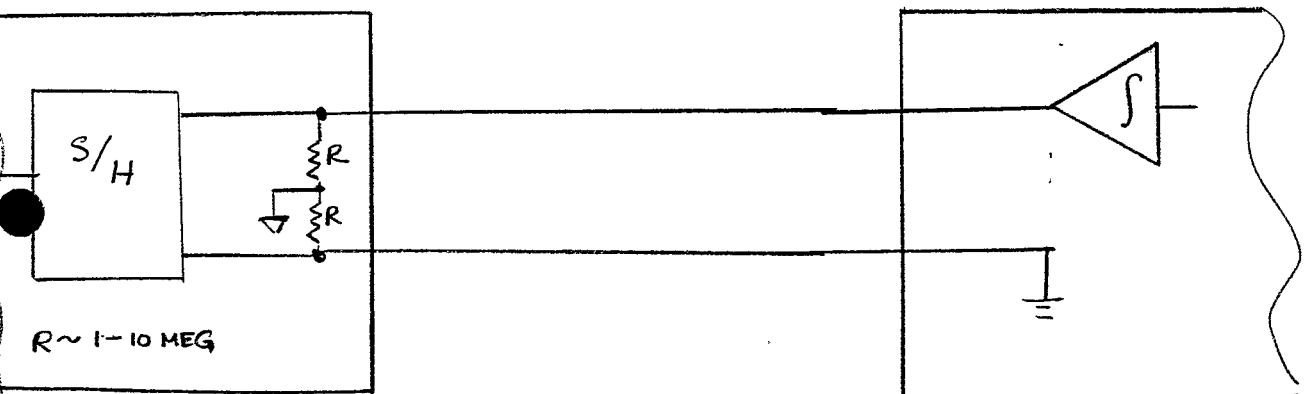
Control Line Readbacks



Timing Signals



ADC Inputs (S/H)



pipe. Discussion is required on this topic. The detector signal and voltage connections are made through a rexolite insulated UHF connector. Rexolite has been a proven material for radiation resistance. Both ends of the detector have gas fittings to allow gas flow.

Detector Biasing

The detectors are biased at nominally 200VDC and the output is processed by integrator circuits which are DC-coupled to the detectors (figure 3). The 200V is generated using a DC-DC converter that switches in the 100 kHz - 1 Mhz range. The circuit uses a regulated +15 V supply rail chopped by an enhancement mode N-channel FET (shown schematically as a switch). The transformer is a step-up with a nominal turns ratio of 15:1. The secondary output voltage is adjustable over a range of 180-250 VDC under light loading. The adjustment is achieved by varying the primary circuit resistance. The circuit is rated for 1.5 mA @ 140 V output.

In the past each transformer has used a single primary with four secondaries. However, crosstalk problems have been noticed in the BLM, and the new generation of bias supplies will use separate transformers for each channel. Thus, for each board 8 chopper circuits will be constructed. This will necessitate larger DC power supplies for the +15 V rails than used in the BLM.

The boards will provide leakages below 10-20 pA and provide high isolation between the channels. To reduce the effects of leakage due to variation in ambient temperature and humidity the boards will be baked and conformally coated with Humiseal. In addition the bias voltages and low level signal outputs to the integrator will be on separate DIN connectors to further decrease leakage.

The output cables to the detectors will be Belden model 9054. It is a triple-shielded RG 59/U type cable with 75 ohm impedance and polyethylene dielectric. The cable is constructed with dual 95 % braids and a 100% foil on the outter layer. This cable was selected for its shielding effectiveness of 110 db , radiation resistant dielectric and low triboelectric properties. The cables will be direct runs from the racks in the RF building to the detectors to avoid leakage problems.

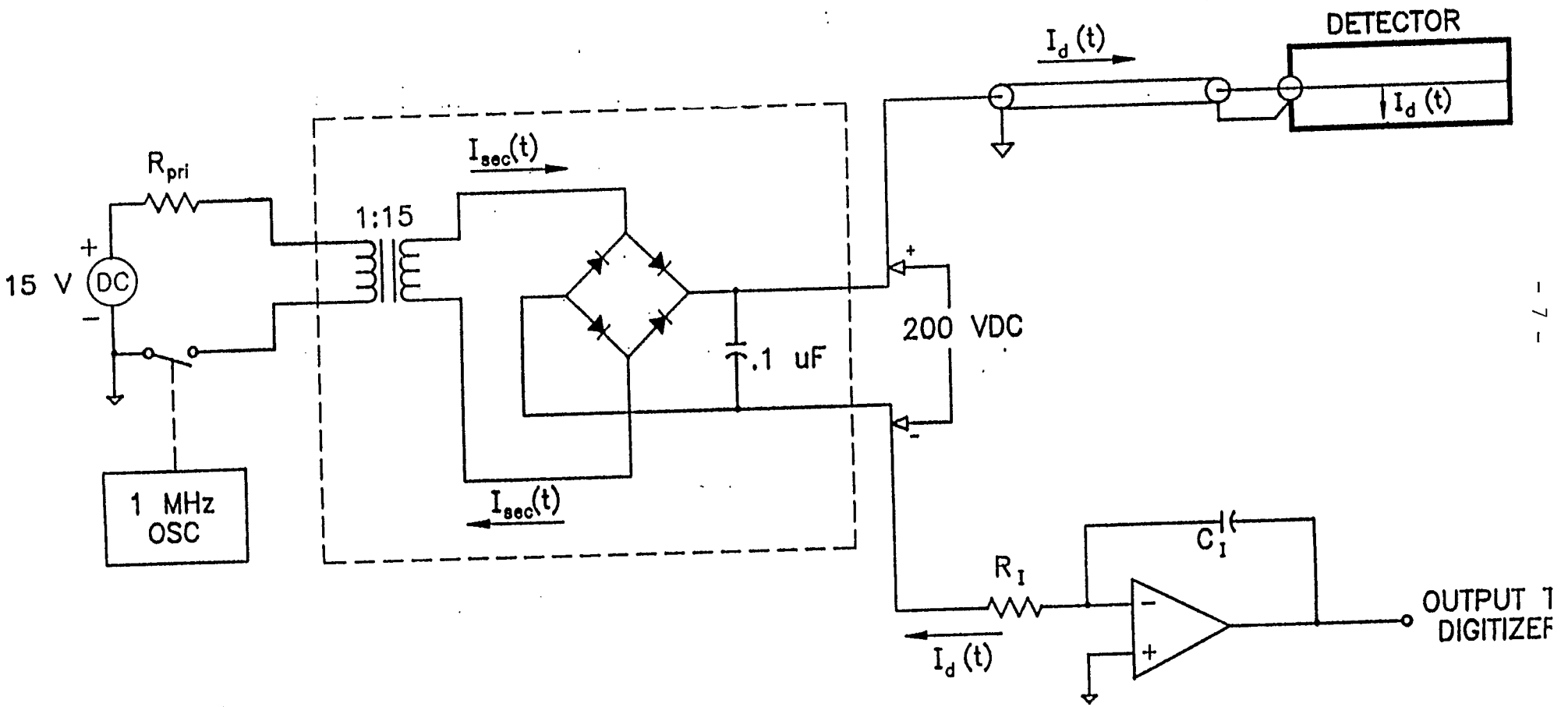
Integrators

A simplified schematic of the integrator circuit is shown in figure 4. The integrators have the capability to gate the integration time interval, hold or reset the output, and select gain. The integrate, hold and reset modes are controlled by the hold and reset switches. The integration scale factor is selected using the gain switch, which makes a binary selection of feedback capacitance. Either low sensitivity (C1+C2) is selected or high sensitivity (C1) is selected. The values selected for the capacitances are C1=1nF and C2=100 nF. The capacitors used are low leakage and low dielectric absorption to insure accurate measurement. The gain switch is implemented with a relay to avoid the leakage and finite on resistance associated analog switches. As such, the gain is intended for switching only at each T0. The reset and hold switches are FETs because of switching speed requirements. All of the switches are controllable via TTL levels and are driven from optically isolated drivers in the controller. The reset time of the integrators has been set to 20 us. This allows a 10 V signal to be reset to within a few millivolts of 0 V.

Selecting the integrator input resistance requires balancing several constraints. The input resistor limits the integrator response time to an impulsive loss by limiting the charge flow from

Basic One-Channel Loss Monitor System

FIG. 3

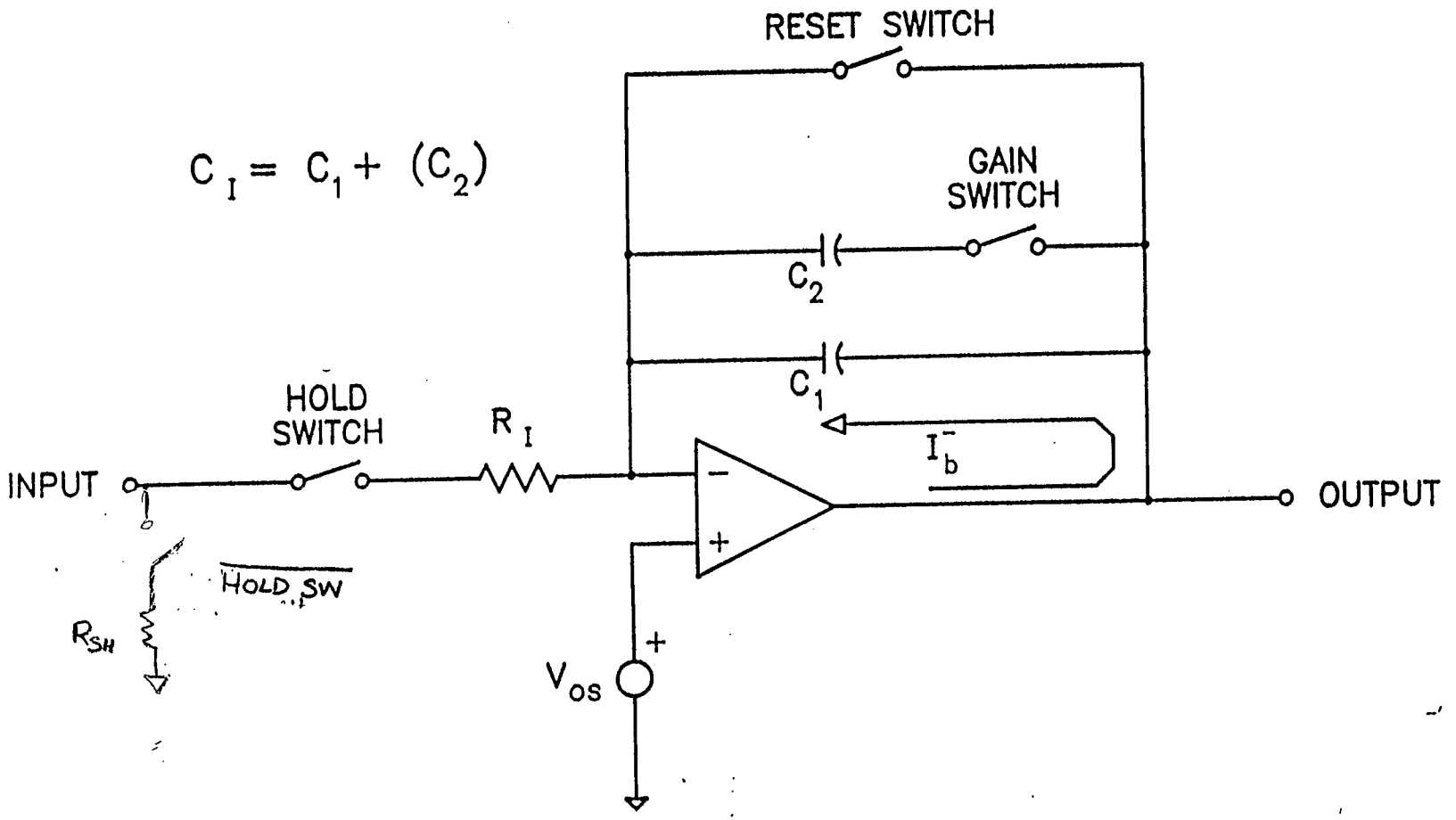


$$V_o = + \frac{1}{C_I} \int I_d(t)dt$$

$$V_o = \frac{I_d \cdot \Delta t}{C}$$

IDEALIZED INTEGRATOR CIRCUIT SHOWING DC ERRORS

FIG. 4



$$V_o = +\frac{1}{C_I}\int I_d(t)dt + \underbrace{\frac{1}{R_I C_I}\int V_{os}\,dt + \frac{1}{C_I}\int I_b^-\,dt + V_{os}}_{\text{ERROR TERMS}}$$

the cable capacitance into the integrator. The time constant formed by the input resistance and cable capacitance sets the speed of the time resolution of the system. However, if the input resistor is too low, noise pick-up on the cables and chopper noise from the DC supplies cause excessive noise at the integrated output. Thus, high values of input resistance are desirable. As a compromise, a 5.1 K input impedance is chosen. This impedance has been successfully used in the Booster and does not cause excessive noise currents to be generated and is consistent with a 99% collection time of 1 ms, considering the worst case cable capacitance. That is it takes 1 ms after an impulsive loss to collect 99% of the signal.

Data Acquisition System

The data acquisition system under primary consideration is the MADC being constructed for RHIC[2]. To support the RHIC MADC which has a single S/H and multiplexes the input, commercial VME-based S/H boards will be used to eliminate sampling skew. Since a single MADC is shared amongst all the channels, the expected time to scan all the channels is approximately 2 ms yielding a maximum scan rate for the system is 500 Hz. If faster scan rates are desired the number of ADCs must be increased. It is intended to use a standard binary format for the digital data. The channel scan and gain list feature available on the MADC board will not be fully used, as the programmable gain will be fixed at unity and the scan order will also be fixed.

If integration of commercial S/Hs and the RHIC MADC is a problem, a commercial alternative for the VME-based data acquisition is from PENTEK, where the ADC and S/Hs are designed to work together in an application such as this. In addition, the I/O between the controller and RLRM hardware is expected to be optically isolated. The standard optical configuration are shown in figure 2 , and are the same as in the RHIC systems, thus the RHIC boards can be used again. However, here too commercial boards can be substituted if necessary.

Mux Control :

The mux shown is used to allow the MCR personnel to monitor any 8 of the 160 RLRM channels. This mux replaces the existing RLRM mux and should be more cost effective than the muxes used in the BLM system. Further since the mux acts as a sub-mux, the control system muxes bringing signals to the MCR need not dedicate up to 256 channels of space to the RLRMs.

The design of the single board mux is a true crosspoint switching matrix whereby any channel can appear on any or all outputs without restriction. To implement the mux, two 128 x 8 single board muxes will be installed in the instrumentation. Control for these muxes consists of 16 bit command word and up to a 24 bit readback word. The communication is expected to be either serial (UART) or parallel, with parallel mode preferred for simplicity. The mux configuration will be changed at most 1 time per cycle, with the changes triggered at T0. The mux control algorithm has already been developed and flow charted in detail for immediate coding.

I/O Summary :

All of the I/O bits between the Loss Monitor System and the controller will be TTL levels from the 74xx series drive capability. The anticipated I/O functions are expressed below :

Controller Inputs :

GAS FAIL READBACKS	4 Bits	Level
POWER FAIL INDICATORS	8 Bits	Level
INTEGRATOR GAIN RDBACK	1 Bit	Level
SYSTEM LCL/REMOTE	1 Bit	Level
SPARE BITS	8 bits	Level

Controller Outputs :

INTEGRATOR RESET	1 Bit	Pulse
INTEGRATOR START	1 Bit	Pulse
INTEGRATOR STOP	1 Bit	Pulse
START ADC SCAN	1 Bit	Pulse
SPARE	8 Bits	Level
SPARE-PULSED	4 Bits	Pulses for Timing

The integrator reset pulse and start/stop pulses are the same as for the Booster system. Typically they are TTL compatible signals and are approximately 1 us wide. The actual width is inconsequential as internal timing in the instrumentation will take care of the pulse shaping.

1. Beadle, E. and Bennett, G., "The AGS Booster Radiation Loss Monitor System", AIP Proceedings No. 229, pp. 35-47, 1991.

2. Michnoff, R., "General Purpose Multiplexed Analog to Digital Conversion System System Specification", October 1994.