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THE LEBT TEST PULSE GENERATOR

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Accelerator Division
Technical Note

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1. The test pulse generator (TPG) is a stand-alone unit which can provide all of the timing signals and calibrated currents needed to test various instrumentation modules.

2. Introduction

The TPG can provide the timing signals listed below. They can be triggered from either trigger input (EXT) or the internal clock (INT). This allows the unit to be synchronous or fully independent.

A. Internal Trigger
   1. Rep. rate from 1 pulse per 2.5 sec to 10 pps.
   2. Positive TTL output.
   3. 5 usec wide

B. Scope Sync
   1. Echo of INT/EXT trigger
   2. Positive TTL output
   3. 5 usec wide

c. Beam Widtn
   1. Delayable from INT/EXT trig.,10-500usec.
   2. Positive TTL output
   3. 500 usec wide.
   4. A LED can light for 10 msec driven by this pulse

D. Reset(for 4 Chan Integrator) derived from INT/EXT trig.
   1. Switchable polarity TTL
   2. 5us wide.

E. INTEGRATE
   1. Delayable from Reset 10-1000 us
   2. Switchable polarity TTL
   3. 5us wide.

F. HOLD (for 4 ch. Integrator)
   1. Delayable from INTEGRATE 10-500us
   2. Switchable polarity TTL
   3. 5us wide

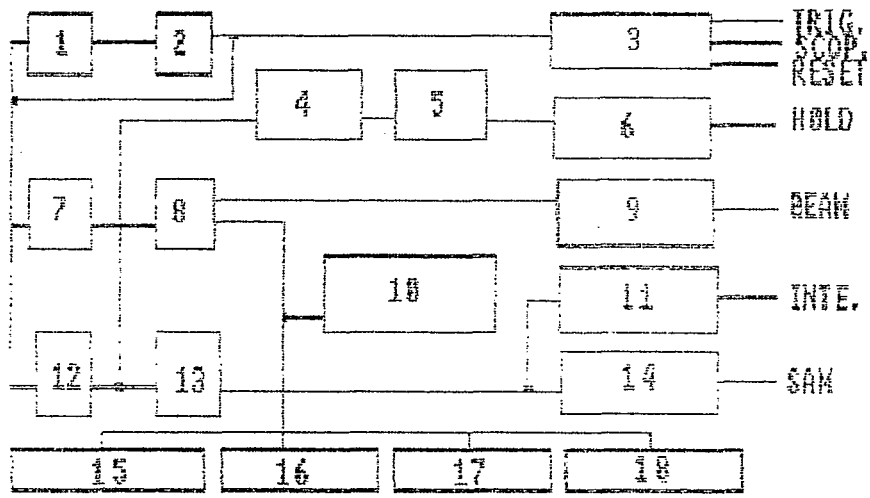
G. Sample (for 16 ch. sample and HOLD)
   1. Delayable from Reset 10-1000 us
   2. Switchable polarity TTL
   3. 5us wide.

H. Analog Calibration signals

The unit can provide calibration signals, coincident with the Beam Width. The calibration sources are current sources with impedance greater than 1v/calibration current. The tolerance for the 100nA source is 1%, and the rise time is 15us. The tolerance for the 10uA, 100uA, and 50mA signals is 0.1%, and the rise time for them is 5us.

3. Design

A. The block diagram of the TPG is as follows:



Blocks 1 and 2 constitute the Internal clock for Trigger.
Block 3 buffers the trigger, scope and reset signals.
Block 4 introduces a (10-500)us delay between the INTEGRATE signal and HOLD signal.
Block 5 adjusts the width of HOLD signal.
Block 6 is the buffer of the HOLD signal.
Block 7 introduces a (10-500)us delay into the INT/EXT trigger pulse.
Block 8 determines the pulse width of the current source.
Block 9 adjusts the width of BEAM WIDTH signal.
Block 10 is the driver curcuit for the BEAM WIDTH indication LED.
Block 11 is the buffer for the INTEGRATE signal.
Block 12 introduces a (10-1000)us delay between the SAMPLE signal and the Internal trigger pulse.
Block 13 adjusts the width of the SAMPLE signal.
Block 14 is the buffer of the SAMPLE signal.
Blocks 15 ,16,17,18 are the current sources.

B. TTL signals:

All TTL signals are generated by a 74123 dual monostable multivibrator. Each 74123 has two monostable stages. First of all, choosing Rx and Cx according to the function Tw=0.28RxCx(1.0+0.7/Rx), makes the pulse width equal 0.28RxCx(1.0+0.7/Rx).

To get the exact width, A large value potentiometer gives rough adjustment and a small one gives fine adjustment.

Each component is chosen as below:

pulse name	width	Pot. and Rx	Cx	Tdelay	Pot.;Rx	Cx
Int, Trigger Reset Scope Sync	5uS	R2=2kΩ P3=500Ω P4=2kΩ	C2= 4700 PF	2.5S ~ 0.1S	P1=1kΩ P2=200kΩ R1=6.2kΩ	C1= 47uF
Beam width	500uS	R4=33kΩ P7=500Ω P8=10kΩ	C4= .047 uF	10- 500uS	R3=51Ω P5=5MkΩ P6=50Ω	C3= .047 uF
Integrate Sample	5uS	R7=2kΩ P13=500Ω P14=2kΩ	C7= 4700 pF	10- 1000uS	R6=50Ω P11=1kΩ P12=75kΩ	C6= .047 uF
Hold	5uS	R5=2kΩ P9=500Ω P10=2kΩ	C5= 4700 pF	10- 500uS	R3=51Ω P5=50kΩ P6=50Ω	C3= .047 uF

C. Internal trigger signal:

Two monostable stages with positive feedback make the internal trigger pulse, buffering this pulse gives the internal trigger signal.

D. Analog calibration signals

When the current>=10uA, two transistors can make the current souce. The 10uA, 100uA and 50mA current source can be made from this circuit but the 100nA current source can not use this circuit. Its distributed capacitance is too big to make a source with such a low current value. Using the LF356 and 1N759A circuit works well.

Atiached are SPICE computer analyses of the four current source circuits.

The load resistance of the four current source circuits must be limited to maintain proper operation.

100nA	R_L < 100kΩ
10uA	R_L < 0.2kΩ
100uA	R_L < 5.1kΩ
50mA	R_L < 2Ω

4. Tolerance of current sources

The tolerance of current sources was measured by DC Voltage input. If the current is big, then Its tolerance will also be high.

The tolerance for the 100nA was found be 0.06%, which was lower than the 1% requirement.

10uA, 100uA and 50mA current sources: The tolerance will change as the temperature changes. SPICE program can be used for showing the relationship between temperature and tolerance.

Following is the measurement data for the 50mA current source, the data shows that if the tolerance is lower than +/-0.2%, then the change of temperature is lower than +/-2.5 degree Celsius. So, if the change of temperature is lower than +/- 1 degree Celsius, then a good tolerance can be obtained for any circuit.

T °C	17	18	19	20	21	22	23	24	25	26	27
current (mA)	49.5	49.5	49.6	49.6	49.7	49.8	49.8	49.9	49.9	50	50
tolerance (%)	-1	-1	-0.8	-0.8	-0.6	-0.4	-0.4	-0.2	-0.2	0	0
T °C	28	29	30	31	32	33	34	35	36	37	
current (mA)	50.1	50.1	50.2	50.2	50.3	50.3	50.4	50.4	50.5	50.5	
tolerance (%)	0.2	0.2	0.4	0.4	0.6	0.6	0.8	0.8	1	1	

5. TPG packaging and pin assignments for J_2/P_2, J_3/P_3 connectors:

The test pulse generator (TPG) is packaged in a 7HP wide (6u x 220mm) Eurocard cassette. The cassette has 3 connectors: clock, P_3 and J_2. The clock input is a KLOC (LEMO) connector, located on the front panel and the clock signal is used for external triggering of the TPG. The P_3, a 25 pin D type connector, is located on the front panel and provides outputs for all the TPG signals. The J_2 connector

is the standard Eurocard mate for the P_2 backplane. The TPG uses J_2 as its power connector.

Refer to Figure 1 for front panel layout.

Table 1 and Table 2 provide signal names for the J_3/P_3 and J_2/P_2 connectors.

Table 1:

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	14	Sample
2	Trigger	15	Integrate
3	Scope	16	Hold
4	Beam	17	Reset
5	NC	18	NC
6 Coaxial Cable	GND Current Source	19	NC
7 Coaxial Cable	50mA Current Source	20	NC

Table 2:

Signal	Pin Number
GND	A-13, 15, 17, 19
+5V	A32, C32
-15V	A31
+15V	C31

6. Thanks

I would like to thank R.L.Witkover and the AGS Instrumentation Group for valuable help in this work.

I would like to thank A.Stillman for valuable help in the use of SPICE program.

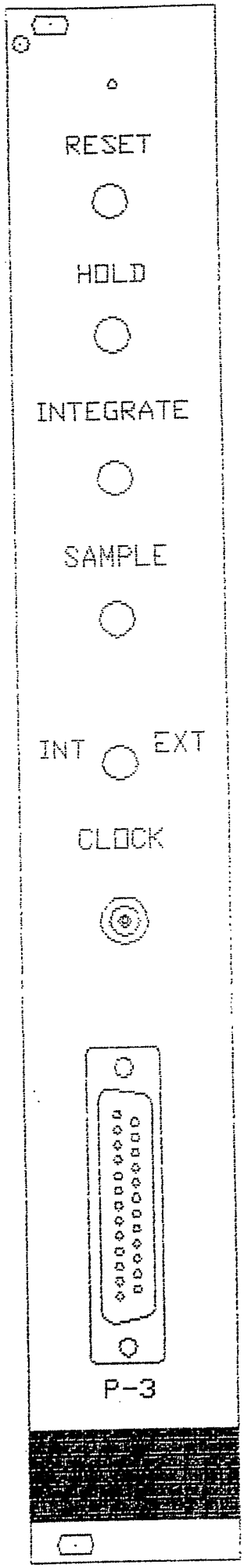
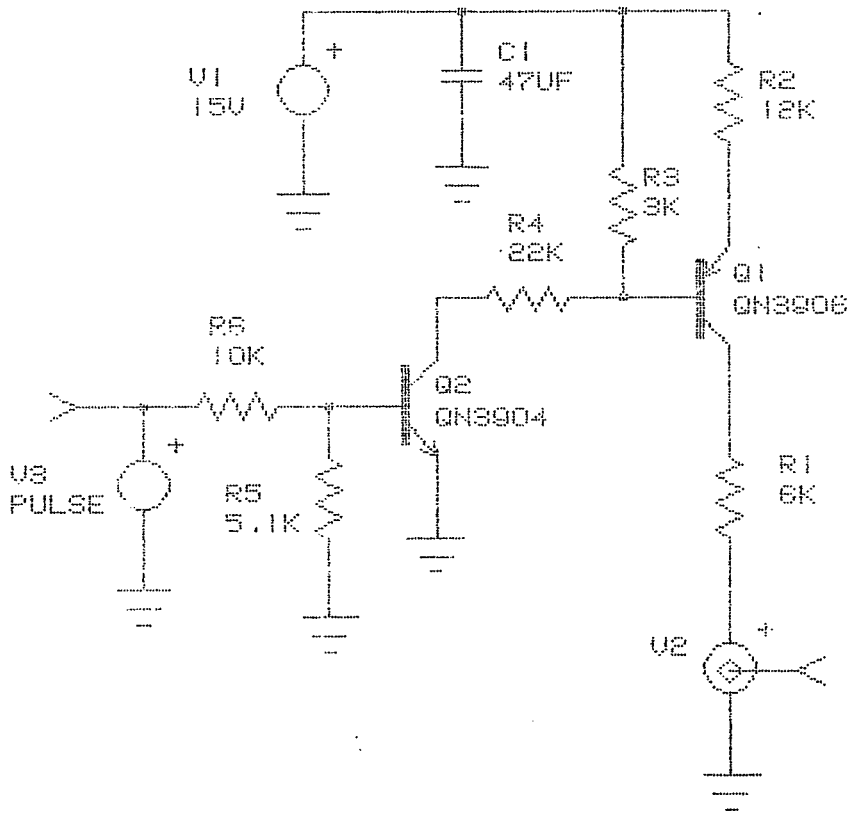
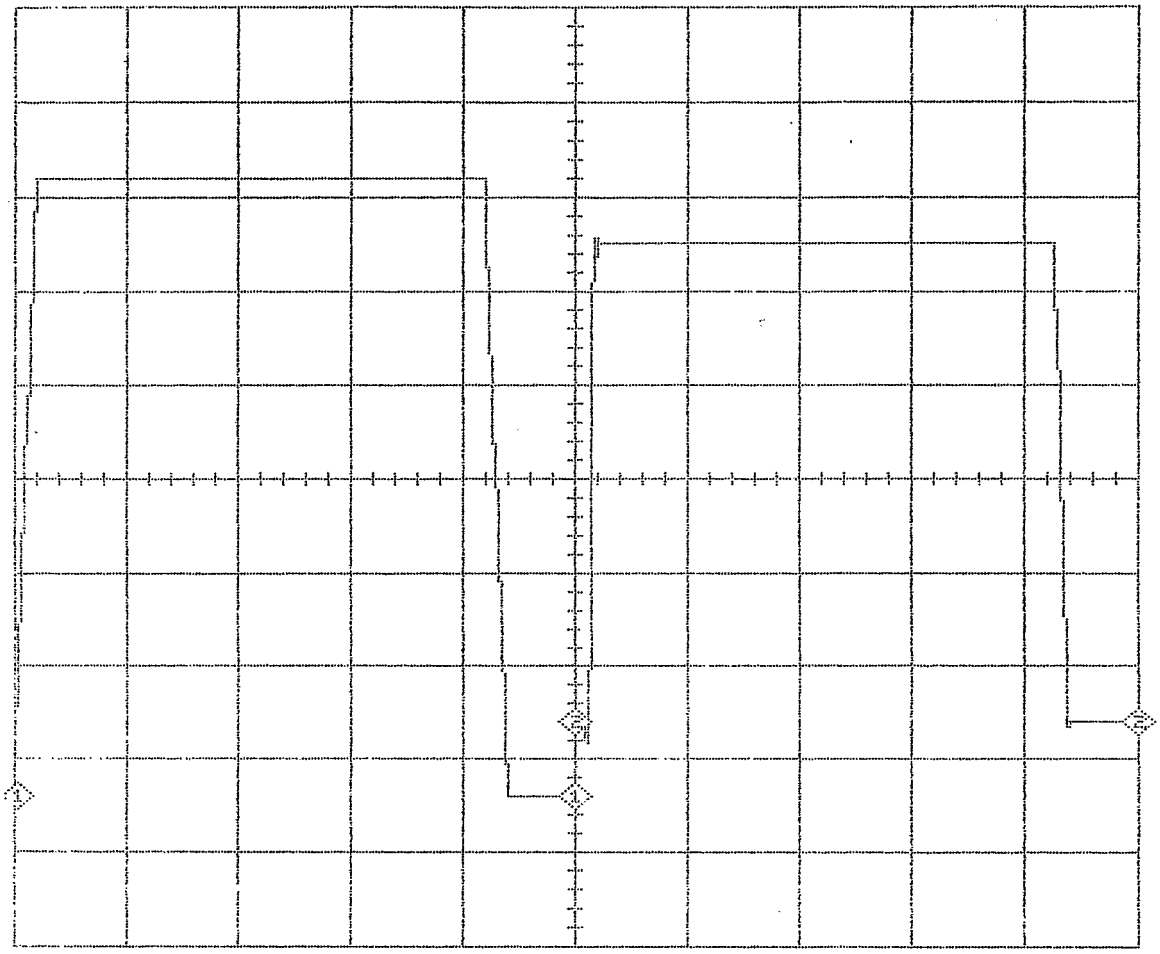


Figure 1


V1
15V
C1
47UF
R2
12K
R3
3K
R4
22K
Q1
QN3906
R6
10K
Q2
QN3904
V3
PULSE
R5
5.1K
R1
6K
U2

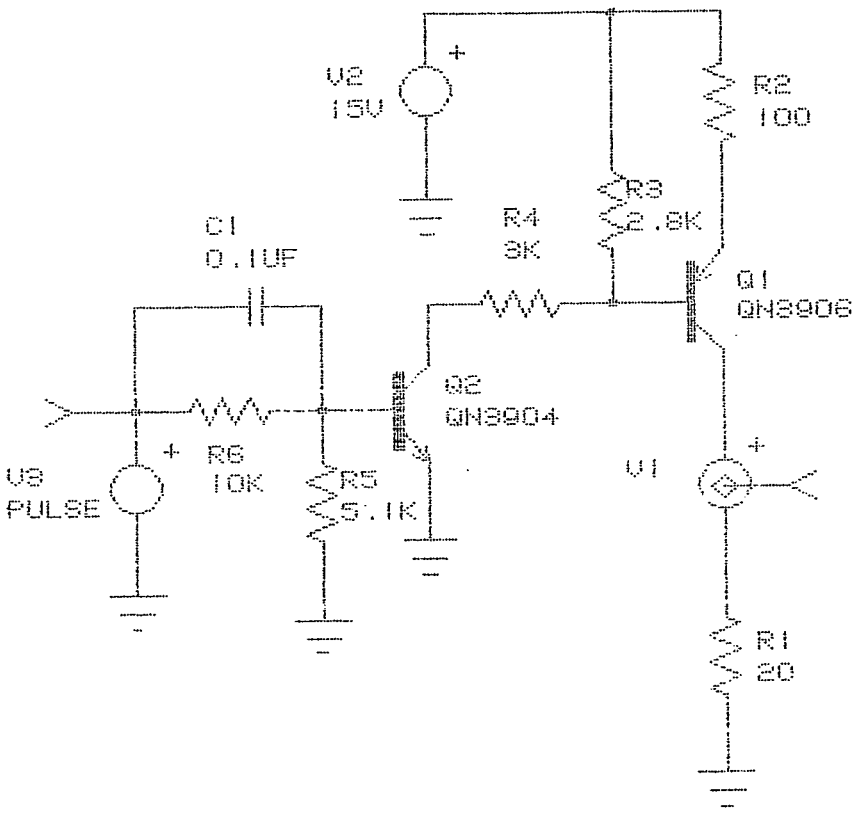
```
CURRENT1
*SPICE_NET
*INCLUDE C:\SPICE\CIRCUITS\DEVICE.LIB
.PRINT TRAN V(1) I(V2)
.OPT LIMPTS=1000
.TRAN 100NS 50US
R6 1 2 10K
R5 2 0 5.1K
Q2 3 2 0 QN3904
R4 3 4 22K
R3 4 8 3K
Q1 6 4 5 QN3906
R2 5 8 12K
R1 6 7 6K
V2 7 0
V1 8 0 15V
C1 8 0 47UF
V3 1 0 PULSE 0.2 3.5 0 2US 2US 40US
.END
```

SPICE ANALYSIS OF CURRENT1.OUT on 4-21-88 page 1



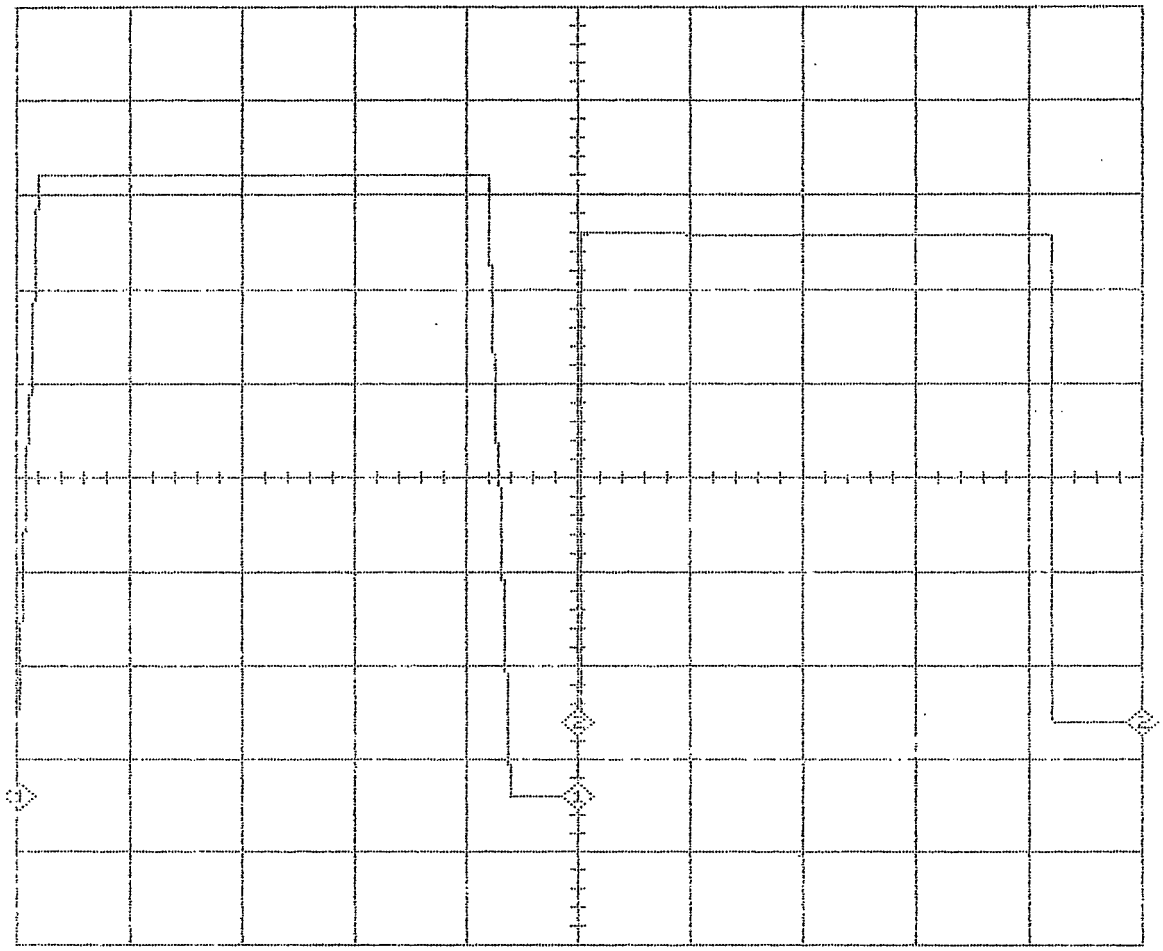
CH 1 V(1) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 500MV/DIV				
YZERO 1.90 V	VER	200MV	200MV	0.00E0V
XSCALE 10USEC/DIV				
XZERO 50.0USEC	HOR	-1.14PSEC	50.0USEC	50.0USEC

CH 2 I(V2) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 20UA/DIV				
YZERO 52.0UA	VER	-0.00E0A	-0.00E0A	0.00E0A
XSCALE 10USEC/DIV				
XZERO -227FSEC	HOR	1.14PSEC	50.0USEC	50.0USEC


V2
15V
R2
100
R3
2.8K
R4
3K
C1
0.1UF
Q1
QN3906
Q2
QN3904
V3
PULSE
R6
10K
R5
5.1K
V1
R1
20

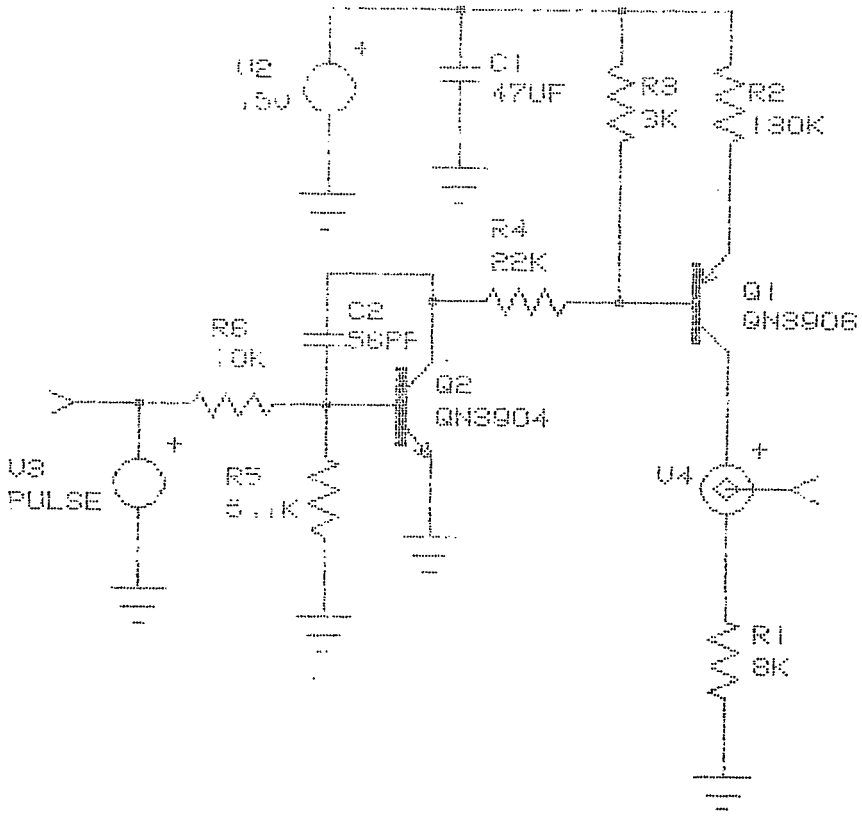
```
CURRENT2
*SPICE_NET
 .TRAN 100NS 50US
.OPT LIMPTS=1000
.PRINT TRAN V(3) I(V1)
*INCLUDE C:\SPICE\CIRCUITS\DEVICE.LIB
R6 3 2 10K
C1 2 3 0.1UF
R5 2 0 5.1K
Q2 1 2 0 QN3904
R4 1 4 3K
R3 4 7 2.8K
Q1 5 4 6 QN3906
R2 6 7 100
V2 7 0 15V
V1 5 8
R1 8 0 20
V3 3 0 PULSE 0.2 3.5 0 2US 2US 40US
.END
```

SPICE ANALYSIS OF CURRENT2.OUT on 4-21-88 page 1



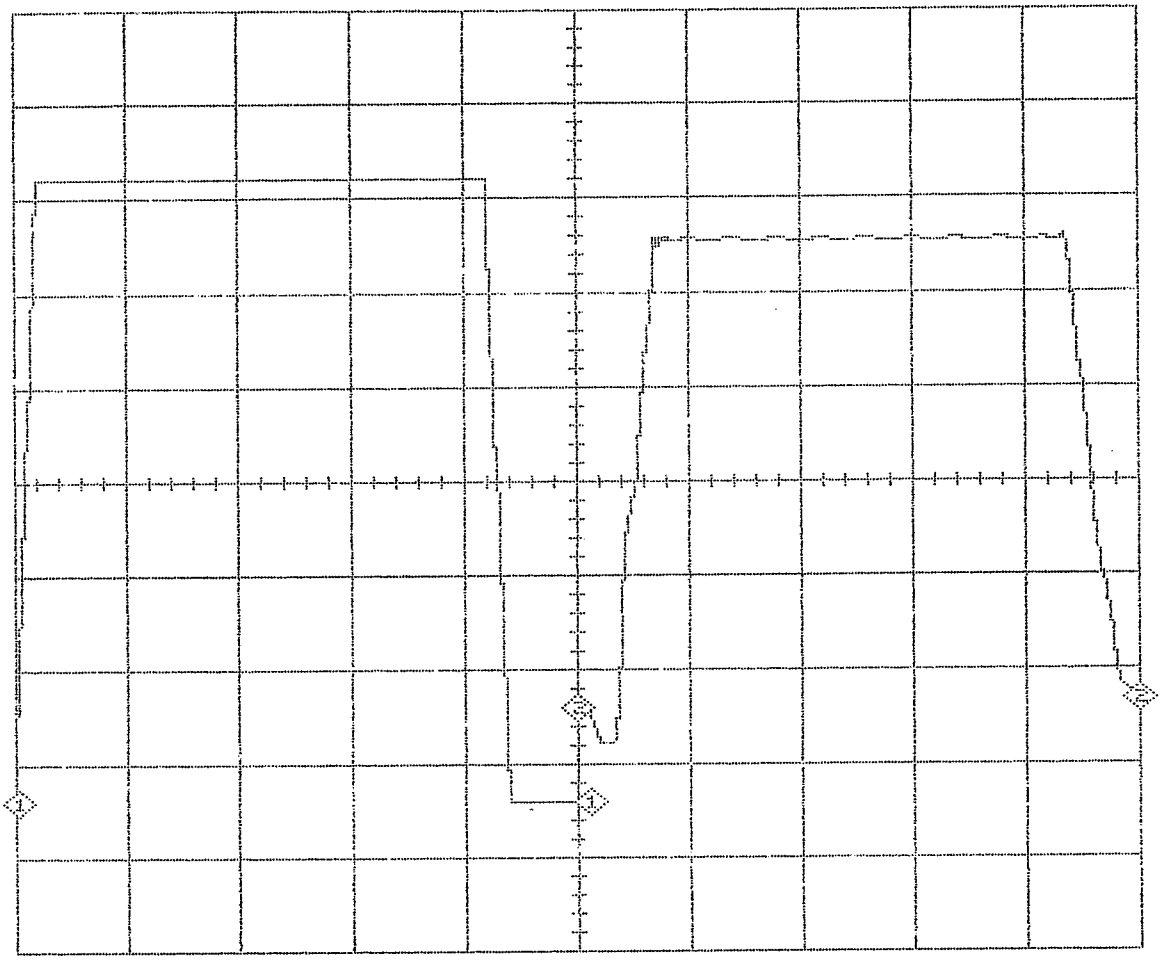
CH 1 V(3) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 500MV/DIV				
YZERO 1.90 V	VER	200MV	200MV	0.00E0V
XSCALE 10USEC/DIV				
XZERO 50.0USEC	HOR	-1.14PSEC	50.0USEC	50.0USEC

CH 2 I(V1) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 10MA/DIV				
YZERO 26.0MA	VER	-0.00E0A	-0.00E0A	0.00E0A
XSCALE 10USEC/DIV				
XZERO -227FSEC	HOR	1.14PSEC	50.0USEC	50.0USEC


U2
.5V
C1
47UF
R3
3K
R2
130K
R4
22K
C2
56PF
R6
10K
Q1
QN3906
Q2
QN3904
U3
PULSE
R5
5.1K
U4
R1
8K

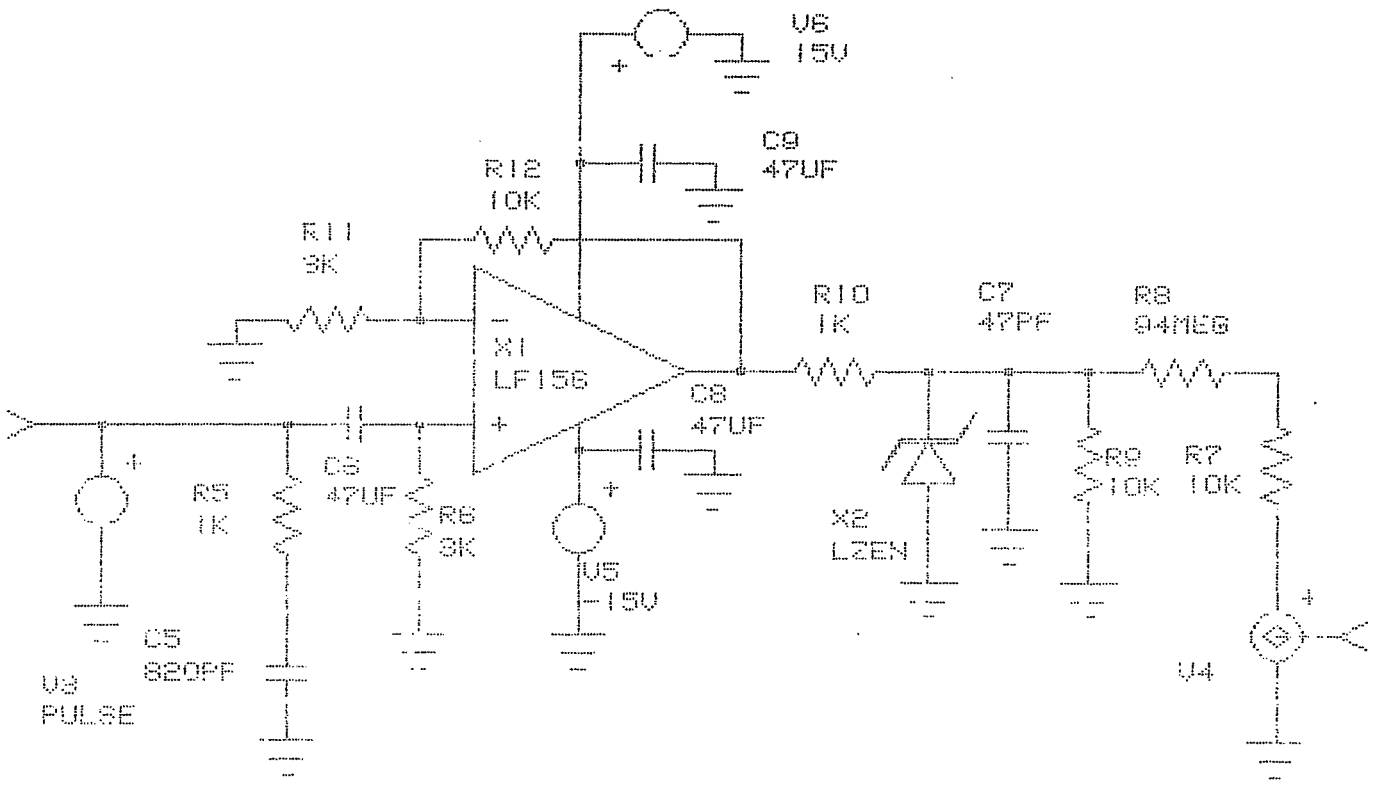
```
CURRENT3
*SPICE_NET
*INCLUDE DEVICE.LIB
.OPT LIMPTS=10000
.TRAN 100NS 100US
.PRINT TRAN V(1) I(V4)
R6 1 2 10K
R5 2 0 5.1K
C2 2 4 56PF
Q2 4 2 0 QN3904
R4 4 5 22K
R3 5 8 3K
Q1 7 5 6 QN3906
R2 6 8 130K
V2 8 0 15V
V4 7 9
R1 9 0 8K
C1 8 0 47UF
V3 1 0 PULSE 0.2 3.5 0 2US 2US 40US
.END
```

SPICE ANALYSIS OF CURRENT3.OUT on 4-21-88 page 1



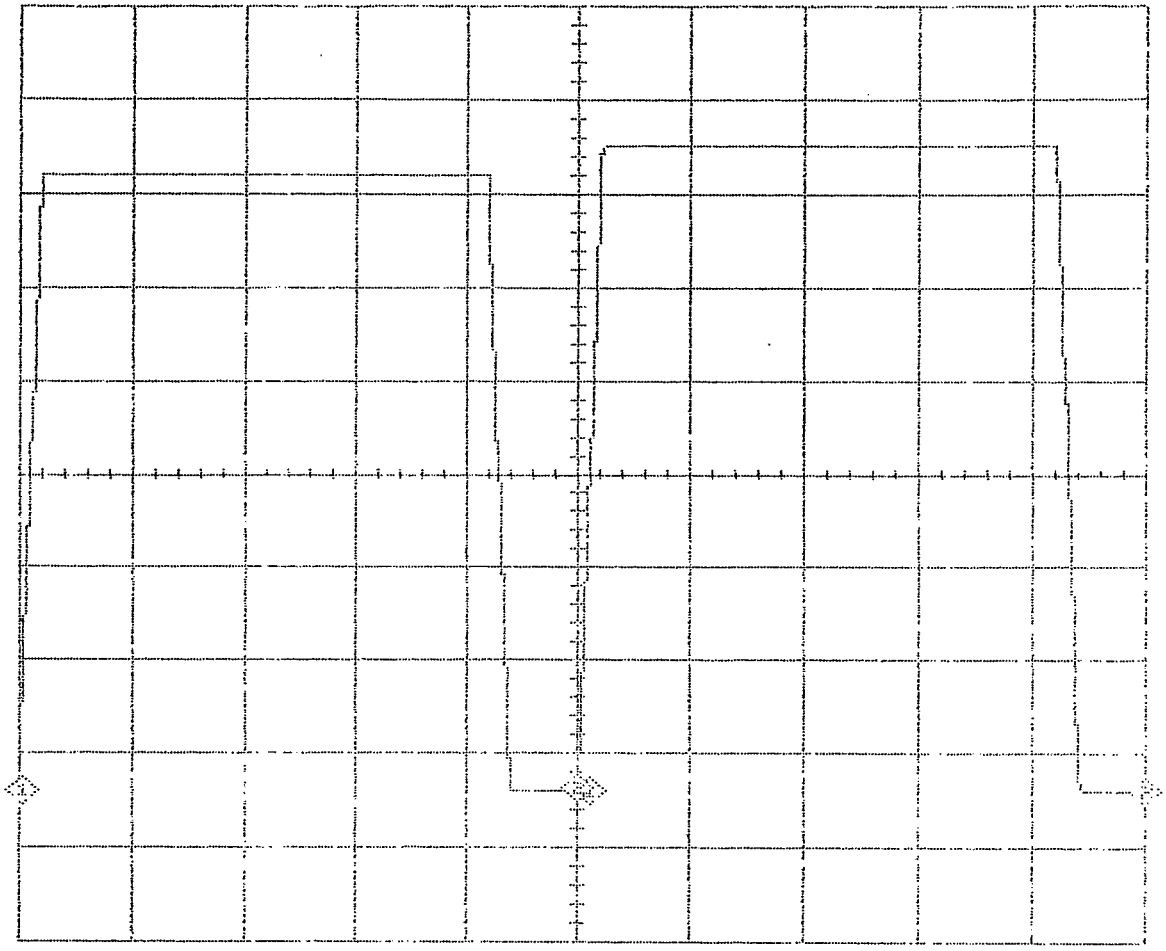
CH 1 V(1) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 500MV/DIV				
YZERO 1.90 V	VER	200MV	200MV	0.00E0V
XSCALE 10USEC/DIV				
XZERO 50.0USEC	HOR	-1.14PSEC	51.0USEC	51.0USEC

CH 2 I(V4) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 2UA/DIV				
YZERO 4.80UA	VER	-0.00E0A	145NA	145NA
XSCALE 10USEC/DIV				
XZERO -227FSEC	HOR	1.14PSEC	50.0USEC	50.0USEC


V6
15V
C9
47UF
R12
10K
R11
3K
X1
LF156
C8
47UF
R10
1K
C7
47PF
R8
94MEG
R9
10K
R7
10K
X2
L2EN
U4
C6
47UF
R6
3K
V5
-15V
R5
1K
C5
820PF
U3
PULSE

```
current
*SPICE_NET
*INCLUDE C:\SPICE\CIRCUITS\LIN.LIB
*INCLUDE C:\SPICE\CIRCUITS\DEVICE.LIB
.OPTIONS LIMPTS=10000
.TRAN 100NS 100US
.PRINT TRAN  V(1)  I(V4)
R11 4 0 3K
V3 1 0 PULSE 0.2 3.5 0 2US 2US 40US
R5 1 2 1K
C6 1 3 47UF
R6 3 0 3K
V6 6 0 15V
C9 6 0 47UF
V5 5 0 -15V
C8 5 0 47UF
R10 9 8 1K
X2 0 8 LZEN  (ZV=12V)
C7 8 0 47PF
R9 8 0 10K
R8 8 10 94MEG
R7 10 11 10K
V4 11 0
R12 4 9 10K
C5 2 0 820PF
X1 4 3 9 6 5 LF156
.END
```

SPICE ANALYSIS OF CURRENT.OUT on 5-27-88 page 1



CH 1 V(1) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 500MV/DIV				
YZERO 1.90 V	VER	200MV	200MV	0.00E0V
XSCALE 10USEC/DIV				
XZERO 50.0USEC	HOR	-1.14PSEC	51.0USEC	51.0USEC

CH 2 I(V4) vs TIME	CURSOR	LEFT	RIGHT	DIFFERENCE
YSCALE 20NA/DIV				
YZERO 68.0NA	VER	125PA	87.5PA	-37.5PA
XSCALE 10USEC/DIV				
XZERO -227FSEC	HOR	1.14PSEC	50.0USEC	50.0USEC

Item	Quantity	Reference	Part
1	5	U1,U4,U5,U6,U9	74123
2	3	C2,C5,C7	4700pF
3	7	R2,P4,R5,R7,P10,P14,P15	2K
4	4	P3,P7,P9,P13	500
5	2	EXT SW1A,EXT SW1B	INT
6	1	U2	7404
7	2	P5,P20	50K
8	1	SW2 (+)	SW2 (-)
9	4	C3,C4,C6,C18	0.047uF
10	1	P12	75K
11	4	P11,P1,R14,R30	1K
12	1	SW3 (+)	SW3 (-)
13	1	P2	200K
14	5	C1,C10,C11,C14,C15	47uF
15	1	R1	6.2K
16	1	U7	7437
17	1	C8	4.7uF
18	1	D1	CM4-84B
19	1	U8	LF356N
20	2	P6,P21	50
21	3	R3,R6,R32	51
22	1	R4	33K
23	1	D2	1N759A
24	1	R8	6.8K
25	2	R9,R31	100
26	6	P8,R13,P16,R17,R22,R27	10K
27	1	U3	7408

Item	Quantity	Reference	Part
28	1	C9	820PF
29	2	R11,R12	3.3K
30	1	C13	47PF
31	2	R15,R16	47M
32	1	C12	0.01uF
33	3	R18,R23,R28	5.1K
34	3	R19,R24,R29	3K
35	2	R20,R25	22K
36	1	C17	0.1uF
37	3	Q1,Q3,Q5	3904
38	3	Q2,Q4,Q6	3906
39	1	R21	10k
40	2	P17,P19	5k
41	1	R26	100k
42	1	P18	50k
43	1	C16	56pF
44	1	SW5 (-)	SW5 (+)
45	1	SW4(-)	SW4 (+)
46	1	R10	1k