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Two Schemes for A-Line Kicker Power Supply

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I. Introduction

The A-line kicker is used for deflecting the beam from the beam line. According to the requirement of experiment, the power supply should be operating in a long pulse. The amplitude of the pulse current is 4000 A and the rise time is less than 10 microseconds. In order to obtain this waveform, two schemes as initial idea is discussed here, each of them has identifiable advantages and weakness. Some requirements of the main elements and facilities are written in this paper. At last some problems are posed, which can be solved by measurement.

II. Main Specification of the A-line Kicker Power Supply

current amplitude	4000 A
pulse rise time	≤10 μs (from 10% to 90%)
repitition	≤10 PPS
pulse fall time	<3 ms (from 90% to 10%)
pulse width	~30 ms (from 90% to 90%)
load: inductance	2.26×10^{-6} henry
resistance	2.26×10^{-3} ohm

(The inductance and resistance of the cables are included in load)

stability of pulse amplitude $\leq 10\%$

(this includes the ripple, overshoot and undershoot)

III. Circuit General Analysis

Figure 1 is a simple principle circuit of A-line kicker power supply. Figure 2 shows the three switches states, voltage waveform of the capacitor and the current waveform of the load. At t_0 switch k_1 is turned on and C is charged at first. At t_1, charging is stopped, the voltage on capacitor C is E_H. At t_2, turn on the switch k_2, the energy in the capacitor is discharged to load L and R. During the period from t_2 to t_3. We have the equation:

$$L\frac{di}{dt} + Ri + \frac{1}{C}\int_0^t idt = E_H \,. \tag{1}$$

and

$$L\,\frac{di}{dt}\,|_{t=0} = E_H \,. \tag{2}$$

$$i|_{t=0} = 0 \tag{3}$$

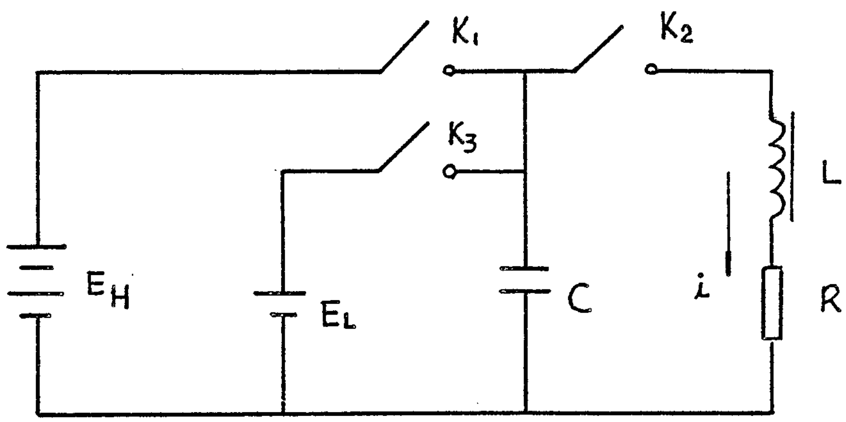

Figure 1. A-line kicker P.S. simple principle diagram.

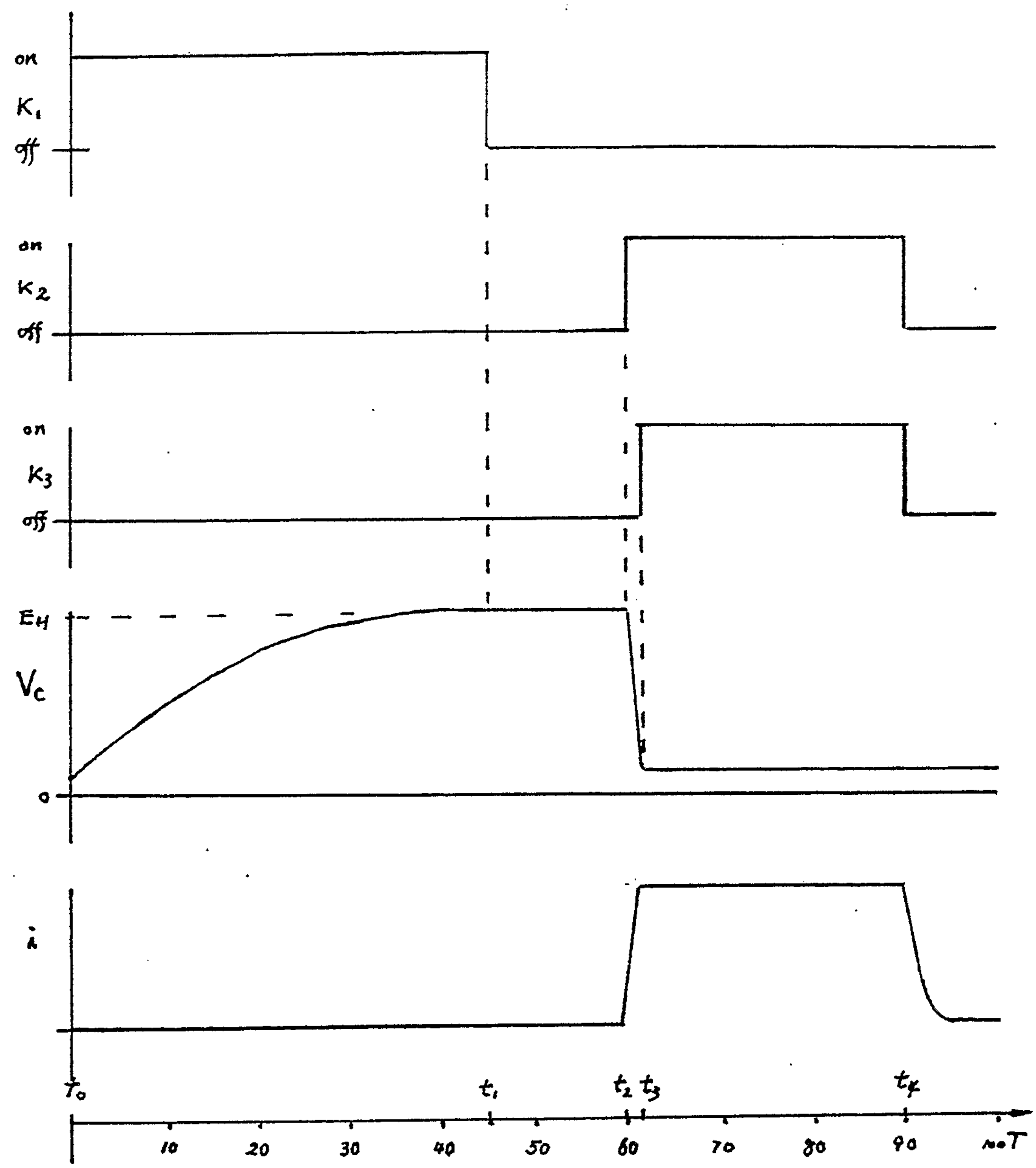

Figure 2. Switches, k_1, k_2 and k_3, status and the waveform of V_c and I_L.

Because of $\frac{4}{LC} >> (\frac{L}{R})^2$ and $e^{-\frac{R}{2L}t} < 0.01$

So, we get

$$i = E_H\sqrt{\frac{C}{L}}\ \sin\omega t \tag{4}$$

with

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}} \tag{5}$$

From the equation (4), we know that the current during the period from t_2 to t_3 increases according to sine curve. Because the rise time is defined from 10% to 90% (see Figure 3). We have the equation

$$t_r = \frac{1}{\omega} \sin^{-1} \frac{I_{tr}}{I_{max}} \tag{6}$$

with $t_r = 10 \times 10^{-6}$ second, $I_{tr}/I_{max} = 0.818$.

From equation (6), we have

$$C = \frac{1}{L} \left(t_r / \sin^{-1} \frac{I_{tr}}{I_{max}} \right)^2 .$$

$$= \frac{1}{2.20 \times 10^{-6}} (10 \times 10^{-6} / \sin^{-1} 0.818)^2 = 48.2 \ (\mu F)$$

Then, we get results following:

$$T = 2\pi/\omega = 2\pi\sqrt{LC} = 65.6 \ (\mu s)$$

$$f = 1/T = 15.2 \ (kc)$$

$$\frac{T}{4} = 16.4 \ (\mu s)$$

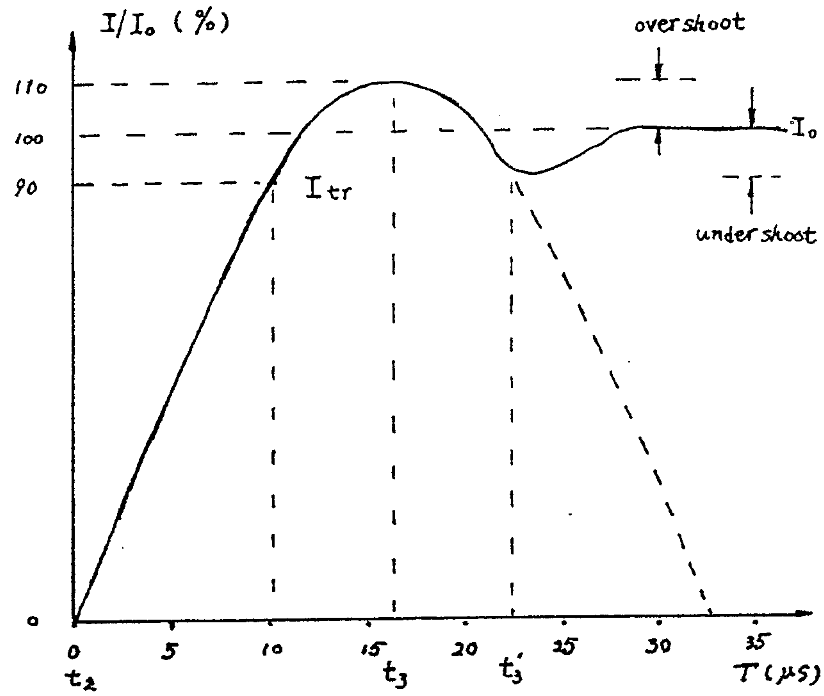

Figure 3. The waveform of the C_1 discharging current.

$$E_H = I_{max}/\sqrt{\frac{C}{L}} = 4400/\sqrt{48.2/2.26} = 953 \text{ V} .$$

$$E_L = IR = 4000 \times 2.86 \times 10^{-3} = 11.4 \text{ V}$$

$$t'_3 - t_3 = 6.4 \ \mu s .$$

When the current flowing from the capacitor C to the load rises to the peak, the switch k_3 is turned on. E_L begins to deliver the current to the load from zero to 4kA as the discharge current from the capacitor C is falling from 4kA to zero during a very short time. The switch k_3 is conducting for 30 ms. The switches k_2 and k_3 are turned off on t_4 and the current flowing through the load is cut off. The load current waveform required is got.

IV. Two Schemes for A-Line Kicker P.S.

The key elements in Figure 1 are switches k_2 and k_3. It is necessary to have the characteristic of high current rating and quick rise time for both of them. It is natural to consider either a SCR thyristor or a Gate turn-off (GTO) thyristor for these switches. Either thyristor can deliver high current and can withstand high voltage. The GTO has the added advantage in that it can turn off the high current by triggering, the operation principle of the power supply can be simplified.

(A) The circuit using GTO as a switch to control load current.

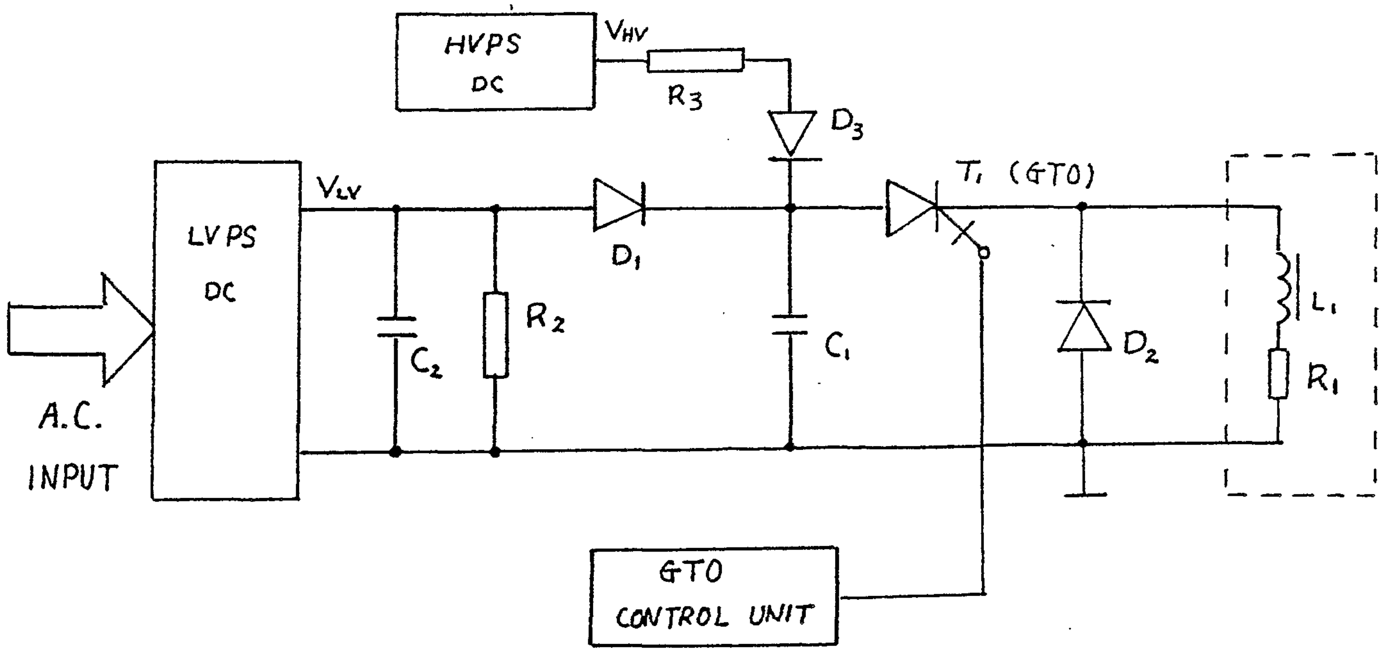

Figure 4. A-line kicker P.S. using GTO thyristor circuit diagram.

Figure 4 shows the circuit diagram. At the beginning, lower voltage power supply (LVPS) and high voltage power supply (HVPS) charge the capacitor C_1 through D_1 and D_3. When the voltage on C_1 is higher then lower voltage power supply's voltage, the current flowing through D_1 is ended, and the HVPS continues to charge C_1 until the voltage on C_1 reaches V_{HV}. This means that the current flowing through D_3 is ended and the process of charging ends. When a suitable trigger drives T_1's gate point, the GTO thyristor as a switch is turned on and the energy stored in capacitor C_1 is discharged through T_1, L_1 and R_1, and the discharging current varies according to the relation in equation (4). The voltage in C_1 decreases as the discharging current increases (see Figure 2). When the voltage falls below the V_{LV}, diode D_1 begins to conduct. The LVPS now delivers the high current to load. After 30 ms, GTO contral unit gives a trigger signal to GTO to turn-off the thyristor and end the current flowing from C_1 to L_1 and R_1. Because the current flowing through an inductor cannot be suddenly changed, the voltage across the inductor L_1 would be very high as the current varies quickly. So the voltage may reach the breakover value of the GTO. Using Diode D_2 for continuing the current can prevent this dangerous condition and lets the energy in L_1 being consumed in R_1. When the GTO is turned off, the HVPS charges the capacitor C_1 again. Thus, the next period begins. Here, resistor R_3 is used for limiting the charging current, C_2 is used to improve the LVPS output characteristic and R_2 is used for setting up an operating current for the lower voltage power supply.

(B) The scheme using SCR as a switch to control the load current.

Figure 5 is the circuit diagram. Its operating principle is described in the following:

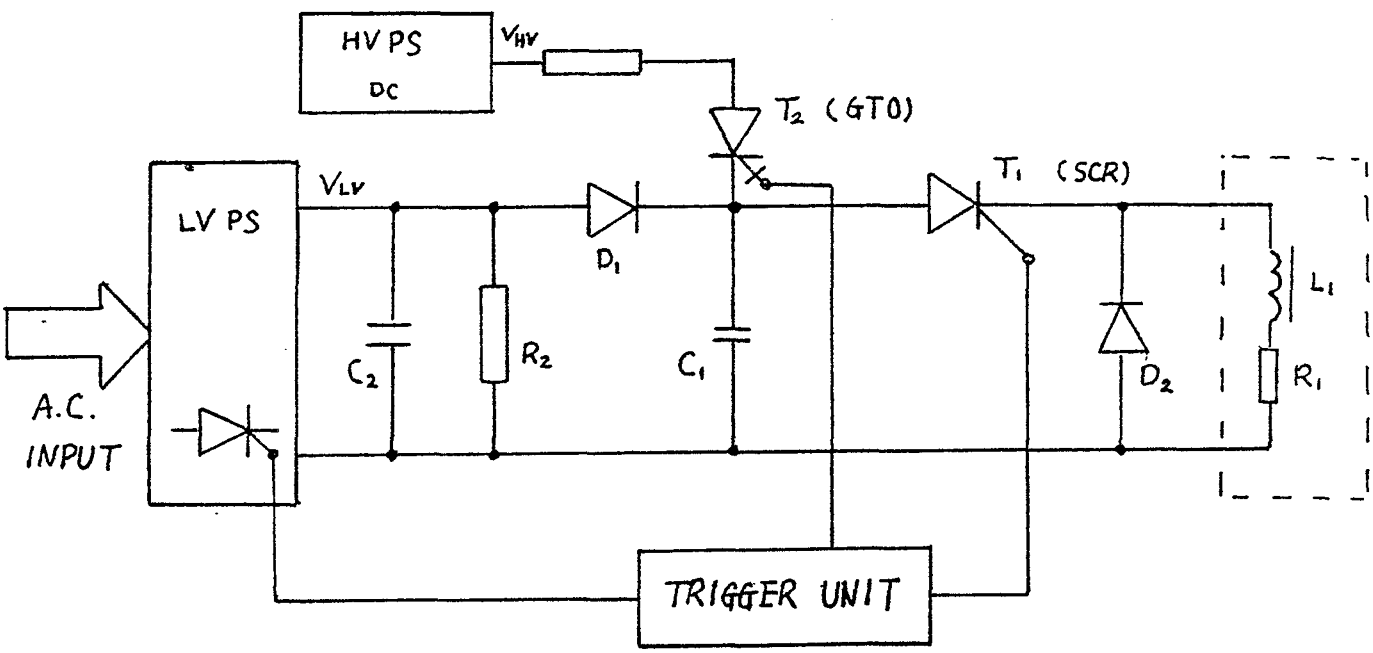

Figure 5. A-line kicker P.S. using SCR circuit diagram.

At first, the trigger control unit drives the LVPS and turns T_2 (grate turn-off thyristor) on and the LVPS and the HVPS charge the energy storage capacitor C_1. When the voltage on C_1 is higher than V_{LV}, D_1 is ended and HVPS is continuing the charging until it reaches the value which is necessary. Then, T_2 is turned off before T_1 is turned on. The energy stored in capacitor C_1 is discharged through T_1, L_1 and R_1. When the discharged current reaches almost its peak, and the voltage on capacitor falls below the voltage of the LVPS, the diode D_1 conducts and the LVPS delivers the current to L_1 and R_1. After D_1 conducts for 30 ms, the trigger contral unit gives the LVPS a signal to stop the SCR trigger of the LVPS to end the current flowing through the load. Because no current is flowing through SCR T_1, it turns off. The energy stored in inductor L_1 is consumed in R_1 through diode D_2. After that begins another identical operating period.

V. Main Elements Chosen

(1) Stored energy capacitor C_1:

According to the calculation above, we use 15 capacitors, each one is 3.3 μF/2.5 ~ 3 kV. If there are some changes we can add or reduce capacitors according to the number we find necessary during testing.

(2) T_1 in scheme (A) (GTO):

According to the reference guide of Powerex Inc. the paraments of Gate-turn off (GTO) thyristor FG 2000 AV are following:

I_T (AV) = 450 A	(conducting average current)
I_{TGR} = 2000 A	(the current turned off)
t_{gt} = 10 μs	(turn on time)
t_{gq} = 30 μs	(turn off time)
V_{TM} = 3.5 V/2000 A	(voltage across the thyristor)
V_{DRM}/V_{RRM} Rang = 4500 V/15	(repetitive foward blocking voltage/ repetitive peak reverse voltage)

$\frac{di}{dt}|_{max}$ = 300 A/μs.

A-line kicker P.S. operating situation:

Operating current: I = 4000 A.

Average current = 1200 A.

Peak current = 4400 A.

Pulse width = 30 ms

Repetitive pulse frequency ≤ 10 PPS

So, we choose five FG 2000 AV GTO thyristors working in parallel. The average working current of each one is 240 A, having a surplus of 210 A current. The peak current is 880 A, having a surplus of 1120 A current. The working voltage is around 1 kV, the surplus is more than 3 kV. The di/dt rate in operating is about 4400/50 = 88 (A/µs), the surplus of it is 212 A/µs.

Turn on time necessary is 12 µs, surplus is 2 µs. Turn off time necessary is 2 ms. The t_{gq} = 30 µs.

So it satisfies the necessary conditions completely.

(3) T_1 in scheme (B) (SCR).

Main parameters of TA 202218:

V_{DRM} = 2.2 kV	(repetitive peak forward blocking voltage)
I_T (VMS) = 2820 A	V_{TM} = 1.45 V
$\frac{di}{dt}$ = 800 A/µs	t_{on} = 2.5 µs

We use four TA202218 SCR thyristors in the circuit. Each one's operating condition is:

operating current = 1000 A

operating voltage = ~1 kV

$\frac{di}{dt}$ rate = 110 A/µs.

According to the operation condition four TA202218 thyristors can suit the requirement of the P.S.

(4) D_1 in both schemes

Diode D_1 is used for conducting high current and isolating high voltage when HVPS charges the capacitor C_1. So it is necessary to select a high current and high voltage diode.

One model RA203048 rectifier can satisfy the operation of the circuit. It's main parameters are following:

$V\ (RRM) = 3\ kV$ $I_F\ (AV) = 4800\ A$

$I_F\ (RMS) = 7535\ A$ $V_{FM} = 1.1\ V\ (6000\ A)$

According to the parameters above, one rectifier is enough.

(5) D_2 in both schemes:

This is a diode which is used for consuming the energy in inductor L_1 to resistor R_1. It has no other demand except the current and the reverse direction voltage. We select R9G02622 for this goal. The operation condition is:

Maximum current: E/R = 4000 A.

Average current $I_{av} = 10 \int_0^{\infty} i dt = 32\ A.$

Reverse direction operation voltage $V_{RDO} = 1\ kV$.

Parameters of the rectifier R9G02622:

$I_F\ (RMS) = 3455\ A$

Peak current = $I_F\ (RMS) \times 1.4 = 4837\ A$

$I_F\ (AV) = 2200\ A$

$V_{RRM} = 2600\ V$

(6) T_2 in scheme (B)

This is a Gate turn-off thysistor which is used for charging the energy storage capacitor and turning off when the voltage on the capacitor reaches the voltage required. Because the pulse repetition rate is 10 PPS (maximum) and the pulse width is 30 ms. We choose the charging time in 45 ms. In general, the time of three times RC is enough to charge capacitor full. So

$$R_3\,C_1 = \frac{1}{3} \times 45 \times 10^{-3} \quad (s)$$

$$R_3 = 15 \times 10^{-3}/48.2 \times 10^{-6} = 310\ (\Omega).$$

The peak current of charging is = 1 kV/310 Ω = 32 A and the average current is that:

$$\bar{I} = \frac{V_{HV}}{R_3} \times 10 \int_0^{\infty} e^{-t/R_3C_1} dt = V_{HV} \times C_1 \times 10$$

$$= 1 \times 10^3 \times 48.2 \times 10^{-6} \times 10 = 482 \text{ (mA)} = 0.5 \text{ (A)}.$$

The data of GTO BTW58-1500 R is:

$V_{DSM} = 1650$ V $\quad$ $V_{DRM} = 1500$ V

$V_{DW} = 1300$ V $\quad$ I_T (AV) = 6.5 A

I_T (RMS) = 7.5 A

(7) D_3 in scheme (A)

This is a diode through which the H.V. power supply charges the capacitor to a necessary voltage.

The current flowing through the diode is approximately.

I_{max} = 1 kV/310 Ω = 3.2 A

$$I_{av} = \frac{V_{HV}}{R_3} \times 10 \int_{-}^{\infty} e^{-t/R_3C_1} dt + \frac{V_{HV}}{R_3} \times 10 \times 30 \times 10^{-3} = 0.482 \text{ A} + 0.96 \text{ A} = 1.44 \text{ (A)}$$

We choose four IN3624 rectifiers working in series as H.V. charging diode. The data of IN3624 is following:

$V_{RRM} = 1000$ V

I_F(AV) = 16 A

$V_{FM} = 1.2$ V

(8) C_2 and R_2

They are the load of the LVPS when the T_1 is not conducting. They needn't be rigorously selected. We choose:

C_2 = 3300 μF/50 V and 3.3 μF/1 kV in parallel

R_2 = 2 Ω/100 W

VI. Specification Required for the LVPS and the HVPS

(1) Lower voltage power supply (LVPS)

Scheme (A) needs a dc steady voltage power supply with a 0 ~ 4500 A current output. The dc voltage can be adjusted smoothly from 0 V to 20 V. Scheme (B) needs a pulsed steady voltage power supply with a 0 ~ 4500 A, 30 ms width pulsed current output. Repetition is 10 pps. The output voltage can be adjusted smoothly from 0 V to 20 V and the rise time and fall time is less than 1 ms. It is necessary for both of them to be protected when the over current and over voltage appear. The ripple and stability required is less than 5%.

(2) High Voltage Power Supply

dc High Voltage = 2 kV

Current output I (av) = 3 A

I (max) = 6A

It's necessary to have a short circuit protection.

VII. Comparison between the two schemes

	Scheme A	Scheme B
(1) Technology	new	general
(2) Element requirement	high	general
(3) Rise time	not very short	shorter
(4) Fall time	shorter	longer
(5) Control	simple	complex
(6) Price		

VIII. Problems:

(1) The current output characteristics of lower voltage power supply: It is not clear how fast the current output from the LVPS rises from several amperes to 4000 amperes, after the LVPS set up its operating current.

(2) The conduction characteristics of RA203048 (D_1): This means the time from when the voltage is delivered to the diode to when the current of 4000 A is set up. If the time is too long, we can change to SCR, for example, TA202218.

(3) The location of the power supply and the distance from the power supply to the A-line kicker magnet: This is concerned with the using of cable.

IX. Conclusion:

Two schemes described above can satisfy the A-line kicker power supply requirement. If the shorter rise time is demanded, design (B) is better.

X. Appendix:

1 Gate turn-off (GTO) thyristor

2 Phase control SCR TA20

3 General purpose rectifier RA20

4 General purpose rectifier R9G0

5 BTW58 SZRIES thyristors

6 General purpose rectifier R310/R311/JEDEC types