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THYRATRON-PROTECT SYSTEM FOR POLARIZED PROTON MODULATORS

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Technical Note

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I. Overview

1. The thyratron-protect system described in this note is intended to protect the thyratrons of the polarized-proton modulators against repeated misfires of the associated ignitrons. To clarify operations, a functional diagram of the polarized-proton modulator is shown in Fig. 1.

2. Referring to Fig. 1, in the modulator there are two output switches which, when closed, initiate the leading edge of the pulse by discharging capacitance, C_{HV}, into the load. One switch handles positive pulses (initial voltage positive); the other switch is poled for negative pulses (initial voltage negative). Simultaneous with the closure of one of these switches, a switch associated with one of the 'low voltage' capacitors charged to V_{1P-4P} or V_{1N-4N} is operated and discharges this capacitance through the output switch to provide the main body of the pulse.

Any one switch is comprised of a parallel combination of a thyratron and an ignitron, both of which are 'fired' simultaneously. The initial discharge is through the thyratron since the ignitron is relatively slow in responding. Eventually, after a period of some tens of microseconds, the ignitron fully takes over and quenches the thyratron. Should the ignitron not respond at all -

termed a misfire in this discussion - the thyratron passes the body of the pulse. Should misfires persist, the thyratron could be irreparably damaged.

The thyratron manufacturer considers a 1% misfire duty cycle - the ignitron does not respond once in one AGS cycle out of 100 - at current levels of several thousand amperes as unlikely to cause permanent damage.* For normal operation - ignitron responding but delayed - the area under the curve of thyratron current vs. time should be about 0.1 amp-sec for no permanent ill effects.* In the case of the output thyratrons, this figure is the total for all four pulses in one AGS cycle.

There are ten channels in each thyratron-protect system corresponding to eight thyratrons in the low-voltage sections and two thyratrons in the output sections. The low voltage channels are designated 1P thru 4P for the positive pulses and 1N thru 4N for the negative pulses, with the corresponding output channels labeled ØP and ØN.

The system described below allows for an occasional misfire in a channel without shutting down the modulator, occasional being defined by numbers loaded into the channel's programmable counters. The programming flexibly allows for larger misfire duty cycles at lower current values. 'Forgiven' misfires are kept track in the channel's totalizing counter. When in any of the ten channels a particular misfire duty cycle is exceeded, the modulator is shut down.

The thyratron protect system is physically located in close proximity to the thyratrons and ignitrons. For reasons of noise immunity, electromechanical counters and relay logic were chosen to implement the system. Special interfaces to these elements were designed using discrete transistors, with by-passing for all critical junctions.

*Private communication from Barry Newton, EEV (UK).

Figure 2 shows some modulator characteristics including a listing of the current levels and timing of each pulse.

The system is dormant until a misfire occurs. This highly intermittent service should prolong indefinitely the useful life of all electromechanical elements and contacts.

II. Thyratron-protect System - Functional Description.

Figure 3 is a functional diagram showing a single channel and most features associated with the whole system.

1. The thyratron current pulse is sensed by a current transformer in the thyratron cathode leg and integrated before being applied to an amplifier having a particular input threshold level. This basically constitutes a width discriminator which provides drive to the input latch IL and misfire counter CMF when the threshold is exceeded by wide thyratron pulses. Activation of the input latch IL also allows the pulses labeled TØ' to start a countdown on the time base counter CTB.

If CMF is programmed for a count of 2, and CTB is set for a count of 50, then a single misfire changes CMF to 1 and starts a count of AGS cycles on CTB. When CTB reaches 0 after 50 AGS cycles, its output switch energizes RYTB (relay, time base), providing drive to the reset coils of both CTB and CMF. This resets both CMF and CTB to 2 and 50 respectively, with the output switch of CTB reverting back to its normal position so that RYTB is again deenergized. Since CMF never reached its terminal count of 0, the output switch of CMF never changed state so that RYMF (relay, misfire) never changed state. Hence the interlock line, comprising the normally closed contacts from this channel in series with similar contacts from all other channels, does not open and cause power to be removed from the modulator.

Had there been another misfire during the countdown of CTB, CMF would have reached its terminal count, immediately opening the output interlock line as well as locking out the reset generated by CTB, preventing the resetting of CMF. The interlock line then would stay open until reset.

Misfires which are 'forgiven' are recorded in the total misfires counter CTMF for flagging purposes only.

It is necessary to avoid a malfunction of the electro-mechanical counter caused by simultaneous application of counting and reset pulses. To avoid the application of a misfire pulse to CMF simultaneous with a reset pulse generated by CTB, the pulses counted by CTB (and therefore the reset generated by CTB) are delayed by 700 ms to 800 ms from the standard AGS TØ pulse to a region in time where no thyratron misfire pulses can occur. These delayed pulses are designated as TØ'. (For reasons of simplicity, all front panel markings referring to TØ' are marked as TØ. TØ itself is never directly used.)

2. A test system has been provided which, upon command, exercises all counters (except CTMFs) and relays in all channels. In each channel, a section of RYTB is placed in series with a section of RYMF, in series with the corresponding pairs from all other channels. These contacts are normally open and are closed when the associated counter (CMF or CTB) reaches its terminal count by counting test pulse TØMFS injected simultaneously into all channels.

When the counter with the largest count in the chain has counted down to 0 (each counter's output switch stays in its terminal state when counting below 0 to 9999 or lower) all series closures are completed and a voltage is applied to the master reset system causing the whole system to revert back to is normal mode.

In the test mode, the system is taken off line by automatically shorting the output interlock line. In the test mode, test pulses TØMFS are locked out of the total misfire accumulator CTMF in each channel.

While the test is far from exhaustive, successful completion certifies proper operation of the CMFs and CTBs of all channels as well as associated RYMFs and RYTBs and the master reset system.

3. A master reset system has been provided which, upon command, will reset all counters (except the total misfire counters, CTMFs) to their preprogrammed values, and thereby reset as well all RYMFs and RYTBs to their standby states. In addition, all latches are reset to their standby states. Resetting of the CTMFs must be done mechanically. The master reset system must be used to initialize the system when powering on.

(The type of counter used, the Sodeco NP612E, is programmed mechanically by a security key and separate pushbuttons for each of its 4 digits. The programmed number is held in mechanical memory and subsequent reset from any number is back to this programmed number, the resetting being either electrical or mechanical).

The master reset system will reset without restriction as to time it may be commanded since this system is internally timed from TØ' pulses to execute the resetting during the time interval having no thyratron pulses. The master reset system may also be used to abort or terminate a system test, described in I.2. above, while the test is in process.

III. Detailed Description

For ease of comprehension, in the description that follows with Figs. 4 thru 8, there are shown in most figures some subsystem components that physically are not grouped together. For example, the counters shown in Fig. 4 - a typical

low-voltage channel - are really mounted separately on the front panel, together with the counters of all other channels. Similarly, the channel voltage regulator shown in Fig. 4 is actually grouped with all the other regulators on a separate PC board on the back panel (which is also the heatsink for the regulator chips). Hence, for troubleshooting, the detailed system drawings are to be consulted. The physical partitioning will be more fully discussed in sec. IV.

1. Low-voltage channels. The configuration of a typical low-voltage channel is shown in Fig. 4.

A Pearson Model 110 current transformer is used in the cathode leg of the thyratron, oriented so that regardless of the output pulse polarity, a positive pulse appears at the input jack. The transformer has a 500 turn secondary (1 turn primary) and a built-in 50 Ω termination (not shown). Hence, the sensitivity at the input jack is approximately 25/500 Volts/Amp or 20 A/V. At the monitor jack (on front panel) this is reduced to close to 300 A/V. With the negative bias shown, the Model 110 will be in the linear mode at the lower thyratron currents/pulse widths, saturating at the higher levels.

An LR low-pass filter has been added to reduce the charge delivered to the integrating 1 uF input capacitor under normal (no misfire) conditions. This reduces very little the charge delivered during a wide misfire pulse input, but has a very significant effect on the short thyratron pulse when the ignitron delay is in the tens of us range. When the 1 uF capacitor voltage reaches $4V_{be}$ (2.8V), Q2 is driven on. Leak-off of the capacitor charge through the 56 K input resistor then produces a wide pulse - 50 to 100^{+} ms - to drive the counters CMF and CTMF and input latch IL.

At what level is a misfire not registered?

Both calculation - see Appendix A - and observation indicate that in the transformer linear mode, a thyratron current pulse of about 275 A initial amplitude, decreasing linearly with time to a baseline width, $\hat{T}$, of 1 ms, will be marginal. Thus a pulse 2P misfire (200A, $\hat{T}$ = 1 ms) will not cause the 1 uF input capacitor to climb over the 2.8 V threshold and activate the system. This is not a problem, representing a thyratron IT product of 0.1 Amp-sec which, as previously discussed is acceptable.

It should be noted that all low-voltage channels (1N thru 4N, and 1P thru 4P) are identical. If a channel were dedicated to a particular pulse - which could cause human error problems - then a particular channel threshold could be tailored to fit a particular pulse and even the very low level misfires could be picked up.

At what level will a normal thyratron current pulse be interpreted as a misfire?

This effect will be most severe for the largest thyratron current pulse. Experimentally it is observed that with the LR lowpass in place, a 145 V triangular pulse (corresponding to a thyratron current initial amplitude of 2900 A) and baseline width, $\hat{T} = 100^{+}$ us will just start to generate drive of sufficient width to operate the counters and latch. This corresponds to an IT product of 0.145 and is probably a satisfactory limit. Thus we are allowing somewhat over 100 us turn-on for pulse 4N which is rated nominally at 2250 A but with 20% tolerance can be as high as 2700 A. It should be mentioned that baseline widths of 50^{+} us have been observed in the modulator at D18.

Power supply 24(1N) is used to operate the resets of CMF1N and CTB1N. Similarly, there are 9 other power supplies to operate the other channels.

These supplies, as in the case shown here, will fold to about 6-7 V if the reset pulse to the counter reset coil lasts longer than 400 ms. This protects the counter reset coils from damage due to a sustained application of 24 V DC (maximum permissible duty cycle at 24 V is 25%) caused by, for example, contacts sticking in the RYTB relay. The reset current of each counter is sensed in diodes D15 and D16 which for the duration of the reset pulse switch "on" transistors Q4 and Q5, respectively. For abnormal durations of reset, the 47 uF capacitor at the base of Q7 is discharged through its associated 33 KΩ, turning on transistor Q7 with a time constant of about 1.5 s. Q7 then shorts out part of the output voltage determining resistor network, causing the output voltage to be sharply reduced.

In the test mode, test pulse TØMFS is injected at the front end into the input 1 uF capacitor. Counters CMF1N and CTB1N then start their countdown to zero (and generally beyond to 99..), producing when each counter has reached its terminal state, and gone beyond, a 'short' between terminals R_{1Na} and R_{1Nb}, awaiting similar action from the other channels, all such terminals being in series. This is further discussed in Sec. 4 below, dealing with the test system. In this test mode, CTB must be prevented from resetting itself and therefore a separate relay RYT is used to disconnect 24(1N) from RYTB1N. RYT is also used to disconnect CTMF1N since we do not wish to count test pulses as part of the accumulated total held in misfire total counter CTMF1N.

2. Output channels

The configuration of the output channels (ØP or ØN) is essentially identical with that of the low-voltage channels. The difference is in the current transformer used and the interface between the current transformer and the counters plus input latch.

Figure 5 shows the circuit diagram of this interface.

The new requirement is the need to resolve misfire pulses that may be as close together as 50 ms. This affects the interface amplifier design as well as the counter drive circuit which must be able to drop back the current built up in the counting coil during the counting interval so that the 'next' misfire (which may follow in 50 ms) properly operate the counter. This done by the near-critical damping provided by collector circuit network of the counter driver, Q5 (Q5 is off unless driving the counters).

Additionally, there was uncertainty as to the use of the Pearson Model 110 transformer in this application. When pulsing in the burst mode, there is a build up of magnetizing current in the transformer (analogous to the build up of voltage in an integrator capacitor) which may land the transformer with its square-loop BH core very near to the point of saturation. Should this occur, the next misfire will produce a short pulse that could be insufficient to take the input integrator over the amplifier threshold. This is a complicated non-linear transient problem involving, among other factors, the transformer recovery from saturation occuring at the higher thyratron currents/pulse widths. Considering that the modulator itself could not be operated with the proper sequence of pulses, at the time this problem was considered, the only practical alternative to answer the question of transformer suitability would have been to build a special pulse generator to simulate the modulator pulses listed in Fig. 2 (driving the transformer secondary). Since this is a far from trivial task it was decided to use the type of current transformer used to monitor the modulator load current, this type being much harder to saturate. This is the Pearson Model 3212 with an IT rating (rect. pulse) of 5 (appx. 10 x bigger than that of the Model 110. Preliminary bench tests indicated only small saturation

effects when this transformer was driven with 4 unipolar triangular pulses, each equivalent to 2500 A primary drive, $\hat{T}$ = 3.5 ms, spaced 50 ms apart.

The Pearson Model 3212 has a 1000 turn secondary (1 turn primary), a built-in 10Ω termination across the secondary, and a built-in 40Ω resistor between the 'hot' end of the secondary and the output terminal (none of this is shown in Fig. 5). Its use in the circuit of Fig. 5 results in a sensitivity at the channel input jack of 10/1000 Volts/Ampere or 100 Amps/Volt. At the monitor jack (front panel) this is reduced again to 300 A/V.

When the voltage across the input integrating 1 uF capacitor reaches $2V_{be}$ (somewhat less than 1.4 V), transistors Q1, Q2, and Q3 are driven on, with approximately 24 V appearing on the collector of Q3. The collector stays at this level since there is no significant discharge path for the input capacitor. At the same time, the 10 uF capacitor near the base of Q4 charges thru nominally 10 KΩ (8.2 KΩ plus 220 Ω plus 2 KΩ pot). When this capacitor reaches about 6 V, Q4 is turned on, discharging the input 1 uF capacitor. Thus a 25 ms pulse is generated at the collector of Q3, independent of the input capacitor initial voltage. Diode D4 aids in discharging the 10 uF capacitor rapidly so that another pulse can be generated, if required, 25 ms after the first one stops.

Under normal conditions (no misfires), the charge on the input 1 uF is substantially held constant between pulses. For this reason, to wipe the slate clean, TØ' is also applied to the base of Q4 to discharge the input 1 uF capacitor when no misfires have occured.

As shown in Appendix A; under normal conditions, positive thyratron pulses of amplitudes shown in Fig. 2, will, when all pulses are present in the sequence and have a baseline width of 60 us, just bring the input capacitor to the 1.4 volt threshold level. For the negative pulse sequence, the

corresponding value of baseline width, $\hat{T}$, is 50^+ us. The corresponding thyratron amp-sec numbers are 0.12 and 0.11^+, respectively. (Desensitization may have to be considered since values of $\hat{T}$ close to the above have already been observed at D18 on a partial negative sequence).

At what level is a first misfire (input 1 uF uncharged) in a sequence not registered?

As shown in Appendix A, a thyratron pulse of baseline width, $\hat{T}$ = 1 ms and initial amplitude somewhat less than 400 A would be marginal in the sense that the channel would not respond immediately. However, the contribution of charge from other normal pulses in the sequence may cause the channel threshold to be reached.

For example, if in the positive pulse sequence there is an output switch misfire on pulse 2P (200 A) with all other pulse firings in the sequence being normal, what amp-sec value will be reached by the thyratron?

This will depend in part on the value of baseline width, $\hat{T}$, of the normal pulses. As calculated in appendix A, the positive output channel will just be activated if pulses 1P, 3P, and 4P have each a value of $\hat{T} \simeq 40$ us (with the misfire pulse 2P having a value of $\hat{T}$ = 1 ms). This corresponds to a value of 0.176 amp-sec for the thyratron. For values of $\hat{T} < 40$ us for the normal pulses and a 2P misfire, the channel will not be activated; the amp-sec number will be less than above and in the limit as the ignitron delay and $\hat{T}$ approach zero, the amp-sec number will approach 0.1 (the area under a pulse of 200 A initial amplitude, and decreasing linearly to zero in 1 ms).

Constant-current charging by the total pulse waveform, of the input integrating capacitor, (with the charge held between pulses) would peg the channel activation more accurately to a constant amp-sec number, for all possible

scenarios and might be considered for introduction later on (the two output channel PC boards would have to be changed).

3. Test System. The test is shown in Fig. 6.

A test of the system is initiated by the pushbutton located on the front panel or by the computer through the T^2L compatible interface comprising transistors Q1 and Q2. This energizes test latch TL1 which allows the first subsequent TØ' pulse to energize test latch TL2. Thus the start of test is always initiated by TØ' and prevented, for example, from coinciding with a misfire pulse or test pulse TØMFS. Latch TL2 allows the test pulse TØMF which is a pulse of a few milliseconds duration and time - coincident with TØ to be injected into the front ends of all the channels.

When all the counters involved in the test have caused closure of all $R(CH\#)N_a$ and $R(CH\#)N_b$ contacts, signal TRS goes from 0 to 24 V and is sent to the master reset system to reset all system components involved in the exercise, including TL1 and TL2.

In the test mode, the output interlock line composed of the series-wired contacts of the RYMFs of all channels is by-passed by sections of a few RYTs. The redundancy in the use of more than one by-pass relay is meant to enhance reliabilty.

4. Master reset system. The master reset system is shown in Fig. 7.

The master reset relays RYMR1 thru RYMR8 provide to each of the 10 channels three pulses: RTB(CH#), RMF(CH#), and RIL(CH#). These are respectively the reset pulses for each channel's timebase counter, misfire counter, and input latch. In addition reset drive RTL is provided for the test system's two test latches.

The reset drive is generated by Q1, Q2, and Q3 and associated components and is delayed by about 100 ms relative to TØ'.

Master reset is initiated by a pushbutton on the front panel or by the computer through the T^2L compatible interface comprising transistors Q6 and Q7. This energizes master reset latch MRL1 which allows the first subsequent TØ' pulse to energize master reset latch MRL2, allowing driver Q4 to energize master reset relays MR1 thru MR8. A reset pulse of about 300 ms is produced which cannot be truncated by a randomly occuring initiation of reset. The trailing edge of the reset pulse turns on Q5 to reset MRL1 and MRL2.

5. TØ' circuitry. The TØ' circuitry is shown in Fig. 8.

The required delay of TØ' relative to TØ of 700 ms to 800 ms is produced by the ramping of the 10.9 uF capacitor in the collector of Q3 thru the 100KΩ from 24 V. A stretched out version of TØ is produced by Q1 and Q2 and turns on Q3 to discharge this capacitor.

When the 10.9 uF capacitor has charged to about 11 volts, Q4 is turned on. The AC coupling, through a suitable time constant, of this Q4 collector edge to the base of Q5, produces in the collector of Q5 the TØ' pulse which is then fed to drivers Q6, Q7, and Q8. The TØ' pulse is of about 40 ms duration at the top of the pulse (and close to 24 V amplitude).

6. Power Supply. Details of the power supply are shown in Fig. 9.

There are 14 regulated 24 V supplies of which 10 are associated with particular thyratron channels. These are designated 24(Ch.#) and have remote external current sensing in the counters' reset coil return and as previously described will fold back if the reset current draw persists. Four 24 V supplies are auxiliary and supply the TØ' circuitry, test and reset functions, etc. These do not have the output voltage foldback feature.

Since some LM317 regulator ICs were found defective by putting out excessive voltage, overvoltage sensing was provided to activate a supply shutdown. The output voltage of each of the 14 24 V supplies is sensed by an SCR (2N1597) and will fire it if the voltage of any supply reaches about 30 V, opening the contacts of relays SP'A' and SP'B' and thereby disconnecting the unregulated DC to all supplies. Resetting is executed by means of the AC on-off switch on the back panel.

A DC-DC converter energized by 24(BIAS) supplies the -15 V bias required by the current sensing transformers of the low-voltage channels.

Normal status of each 24 V supply is indicated by a brightly glowing green LED on the front panel and labeled with the appropriate designation. A low will dim this LED and light up red 'low' LEDs, also located on the front panel. A readback is provided to the computer of this alarm system via a T^2L compatible output jack.

7. Miscellaneous

A change in state of the output switch of the CMF, CTMF, and CTB of each channel occurs when the respective terminal counts are reached. This is displayed on the front panel by a red LED of the counter involved, as shown in Fig. 4.

In addition, any such event is summed into the appropriate one of three buses: a misfire fault readback bus, a timebase fault readback bus, and a misfire total readback bus. These provide T^2L compatible readback signals (on the back panel) to the computer. Thus, for example, a break in the interlock output line (modulator shutdown) is read back to the computer via the misfire fault bus.

IV. Physical Partitioning

The three counters of each channel are located on the front panel as are status lights of each counter's output switch.

All relays, latching or not, are located on the back panel which also serves as the heatsink for the regulator ICs(LM317K).

This interface circuitry has been broken up into 9 PC boards which mate with edge connectors mounted on the back panel. These comprise:

a. 4 dual-channel low-voltage channels (D09-E1717-4) and correspond essentially to Q1, Q2, Q3, and associated components of Fig. 4. The LR input filters are on the back panel.

b. 2 output channel boards (D09-E1713-4). Each board is essentially the circuit shown in Fig. 5.

c. 1 test and reset board (D09-E1725-4). This board comprises the transistors and associated components of Fig. 6 and Fig. 7.

d. 1 TØ board (D09-E1721-4). This generates the TØ' pulse and is essentially the circuit shown in Fig. 8.

e. 1 voltage regulator (VR) circuit board (D09-E1729-5) which contains the control elements for all 14 24 V supplies.

The power transformers, rectifier diodes, filter capacitors, etc. are located in the chassis between the front and back panels.

Acknowledgements

The author expresses his gratitude to John Dunning who designed the mechanical package and fabricated and debugged the prototype; Carl Eld and Lou Mazarakis who assisted in the preliminary testing at the D18 modulator.

Appendix A

1. Charging of the integrating capacitor

The circuit is shown below in Fig. A1, with the voltage driving waveform from the current sensing transformer shown in Fig. A2.

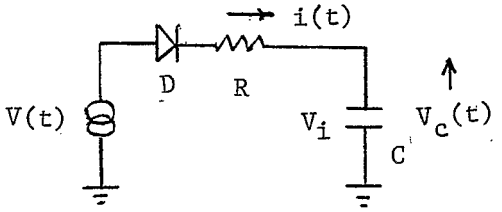


Figure A1

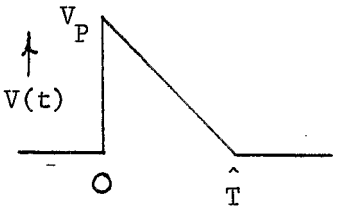


Figure A2

Initially, an ideal diode with zero offset (junction voltage) will be assumed (later in actual numerical cases, an offset voltage will be subtracted from V(t) corresponding to the diode used - i.e. 0.7 V for the Si 1N5282 and 0.3 V for the Schottky 1N6263. The diode is required to prevent V_C from discharging through the source once the source voltage has dropped below the capacitor voltage).

By the straightforward use of Laplace transform analysis,

$$V_c(t) = V_p \left[\left(1 + \frac{RC}{\hat{T}}\right) - \frac{t}{\hat{T}}\right] - \left[V_p\left(1 + \frac{RC}{\hat{T}}\right) - V_i\right] \varepsilon^{-t/RC} \qquad (1)$$

where V_i is the initial voltage on C (assumed positive polarity), and

$$i(t) = \frac{V_p}{R} \left[\left(1 + \frac{RC}{\hat{T}}\right) \varepsilon^{-t/RC} - \frac{RC}{\hat{T}}\right] - \frac{V_i}{R} \varepsilon^{-t/RC} \quad . \qquad (2)$$

At $t = t_c$, i(t) reaches zero amplitude and D prevents further flow of current in the reverse direction. The value of t_c is given by

$$t_c = RC \ln \frac{V_p \left(1 + \frac{RC}{\hat{T}}\right) - V_i}{V_p \frac{RC}{\hat{T}}} \quad . \tag{3}$$

The capacitor voltage at $t = t_c$, or the final voltage V_{cf}, the capacitor charges to, is given by

$$\frac{V_c(t_c)}{V_p} \equiv \frac{V_{Cf}}{V_p} = 1 - \frac{RC}{\hat{T}} \ln \left[\left(1 + \frac{\hat{T}}{RC}\right) - \frac{\hat{T}}{RC} \frac{V_i}{V_p}\right] . \tag{4}$$

2. Output pulse width for low-voltage channel misfires

For these channels, C (1 uF) is discharged by resistor, R_D (56 KΩ). The time interval, τ, to discharge from the initial value V_{Cf} to the amplifier threshold value, V_T, (approximately 2.8 V) is given by

$$\tau = R_D C \ln V_{Cf}/V_T \quad . \tag{5}$$

Hence for V_T = 2.8 V, and V_{Cf} = 4 V, τ ≃ 20 ms. Dropping below this value of counting pulse width would cause marginal counter operation.

Neglecting the LR input filter with its insignificant effect on wide misfire pulses, the value of V_p corresponding to a V_{Cf} = 4 V can be calculated from eq. (4) above with the transformer assumed in the linear mode, and R ≃ 1 KΩ, and $\hat{T}$ = 1 ms. $(RC/\hat{T} = 1)$. Further, V_i = 0 since in these channels C discharges to zero in the period between pulses. Thus, $(V_{Cf}/V_p) = 1 - \ln 2 \simeq 0.307$ or V_p = 4/0.307 ≃ 13 V. Adding 0.7 V for the diode, a pulse of 13.7 V initial amplitude is required. With the stated sensitivity of 20 A/V, we find a thyratron pulse

of initial amplitude of 20 x 13.7 A or 275 A and baseline width, $\hat{T}$ = 1 ms, will approach marginal operation.

It will be noted that the logarithmic relationship of eq. (5) indicates compression in the width range for a wide range of V_{Cf} values.

3. Output channels - normal firings

The appropriate value of RC ≃ 700 us (C = 1 uF, R = 700 Ω including transformer source impedance).

a. For positive pulses (see Fig. 2), using a sensitivity of 100 A/V:

Pulse	Xformer O/P	Drive to Int.
	V	V
V_p (1P)	14	13.7
V_p (2P)	2	1.7
V_p (3P)	14	13.7
V_p (4P)	10	9.7

When 1P is applied, C is in a discharged state (V_i = 0) and V_{Cf} (1P) is calculated from eq. (4), for $\hat{T}$ = 60 us, to be 0.556 V. This becomes the value of V_i when 2P is applied, assuming no leak-off of charge between pulses. Hence V_{Cf} (2P) is calculated to be 0.587 V which in turn becomes the value of V_i for the application of 3P. In this manner, V_{Cf} (3P) = 1.098 V and V_{Cf} (4P) = 1.409 V. Since the threshold is at $2V_{be}$ (at room temperature, just under 1.4 V), this will just activate the interface.

b. For negative pulses, again using sensitivity of 100 A/V and Fig. 2:

Pulse	Xformer O/P	Drive to Int.
	V	V
V_p (1N)	4.5	4.2
V_p (2N)	11	10.7
V_p (3N)	6	5.7
V_p (4N)	22.5	22.2

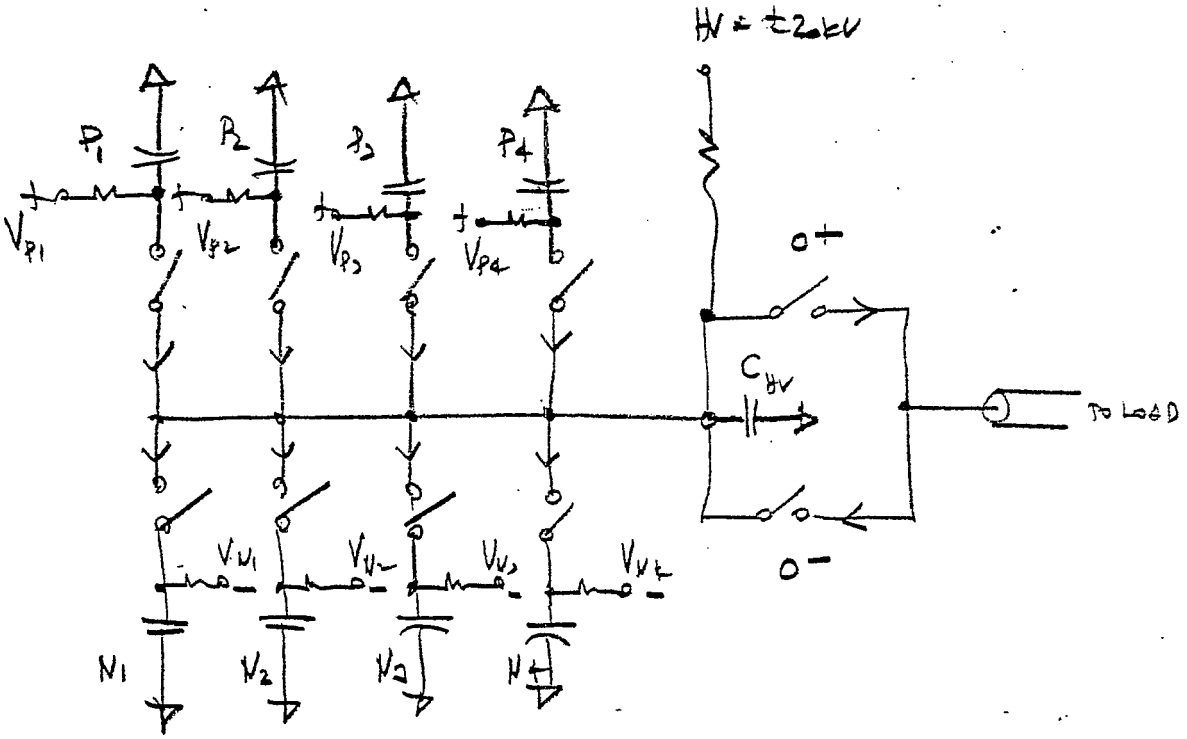
Similarly to 3a above, when 1N is applied, $V_i = 0$, and V_{Cf} (1N) is calculated from eq. (4), for $\hat{T}$ = 40 us, to be 0.143 V, which in turn becomes the value of V_i for pulse 2N. In this fashion, V_{Cf} (2N) = 0.499 V, V_{Cf} (3N) = 0.661 V, and V_{Cf} (4N) = 1.375 V. Hence for the nominal values of thyratron currents listed in Fig. 2, the negative output channel will just be activating for an ignitron delay, $\hat{T}$, of 40 us.

c. First pulse misfire-all other pulses normal. Assuming $\hat{T}$ = 1 ms (a very pessimistic assumption since the first pulse in either sequence is listed at $\hat{T}$ = 3.5 ms in Fig. 2), and $V_i = 0$, RC ≃ 700 us, one obtains from eq. (4), $V_{Cf}/V_p = 1 - 0.7 \ln 2.429 = 0.379$. A marginal situation develops when V_{Cf} = 1.4 V or $V_p \simeq 1.4/0.379$ V = 3.695 V. Adding 0.3 V for diode offset, one gets $V_{Xformer}$ = 3.995 V. At 100 A/V, this corresponds to a thyratron initial current somewhat less than 400 A.

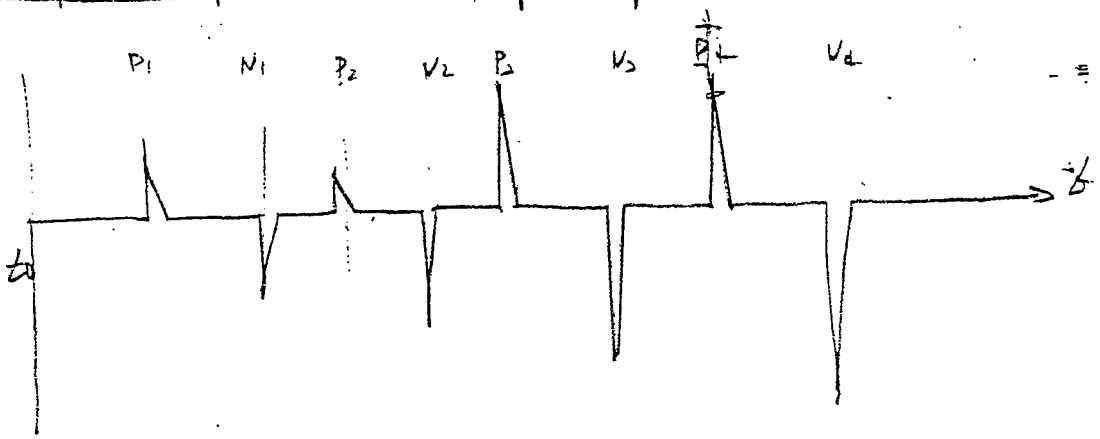
d. Positive sequence - 2P misfire, all other pulses normal. The sequence listed below is used:

Pulse	Xformer O/P	Drive to Int.	$\hat{T}$
	V	V	us
V_p (1P)	14	13.7	40
V_p (2P)	2	1.7	1,000
V_p (3P)	14	13.7	40
V_p (4P)	10	9.7	40

In the manner of previous above, V_{Cf} (1P) is calculated (with $V_i = 0$) from eq. (4) as 0.377 V. This becomes the value of V_i for the calculation of V_{Cf} (2P) = 0.811 V. Continuing in this fashion, V_{Cf} (3P) = 1.145 V and V_{Cf} (4P) = 1.354 V. This will marginally activate the channel and corresponds to an area under the thyratron vs time plot of $1/2(1400 + 1400 + 1000) \cdot 40 \cdot 10^{-6} + 1/2(200) \cdot 10^{-3}$ A-sec = 0.176 amp-sec.



Normal operating mode: pulses alternate in polarity

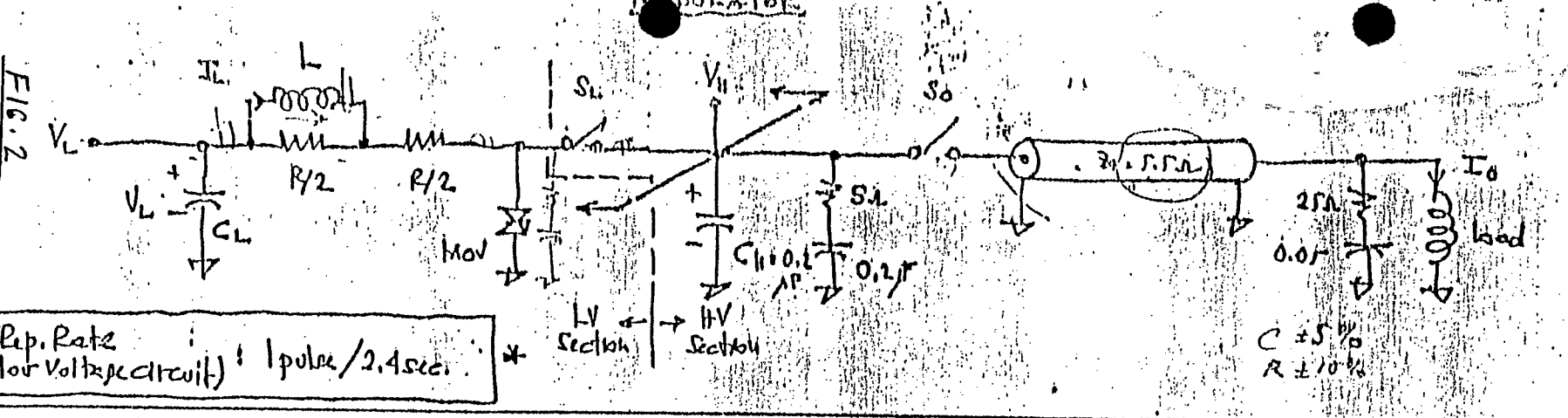


Cycle rate : ≥ 1/2.45

35ns < Spacing < 100ns between adjacent pulses

FIG. 1.
MODULATOR FUNCTIONAL DIAGRAM

FIG. 2 LISTING OF MODULATOR PULSES



* Max. Rep. Rate (Each low voltage circuit) : 1 pulse / 2.4 sec. *

Rec. No.	Ckt. No.	Time (sec)	I_o (Amp)	Pulse Width (ms)	R (ohms)	(Watts)	C_L (μF)	L (μH)	I_L (A)	V_L (Volts)	(Autom. L.) V_H (kV)	(Manual) V_H (kV)
1,	(1P),	-	1400	3.5	0.75 ,	571	2500	500	740	1050	8.3	
2,	1N ,	177	-450	3.5	2.0 ,	135	800	1500	240	-900	-2.6	
3,	2P ,	235	200	1.0	5.0 ,	21	100	1000	105	1000	1.2	
4,	2N ,	280	-1100	3.0	1.0 ,	428	1700	500	575	-1100	-6.5	
5,	3P ,	337	1400	3.5	0.75 ,	571	2500	500	740	1050	8.3	
6,	3N ,	392	-600	1.0	2.0 ,	90	300	350	320	-1200	-3.6	
7,	4P ,	450	1000	1.2	1.0 ,	125	600	250	525	1000	6.0	
8,	4N ,	515	-2250 (270° max)	3.5	0.75 ,	1500	2500	500	1150	-1690	-13.3	

±20%

R.T. Mashburn
Oct. '87

BROOKHAVEN NATIONAL LABORATORY

BY_____ DATE_____ SUBJECT FUNCTIONAL DIAGRAM SHEET NO._____ OF_____

CHKD. BY_____ DATE_____ JOB NO._____

DEPT. OR PROJECT_____

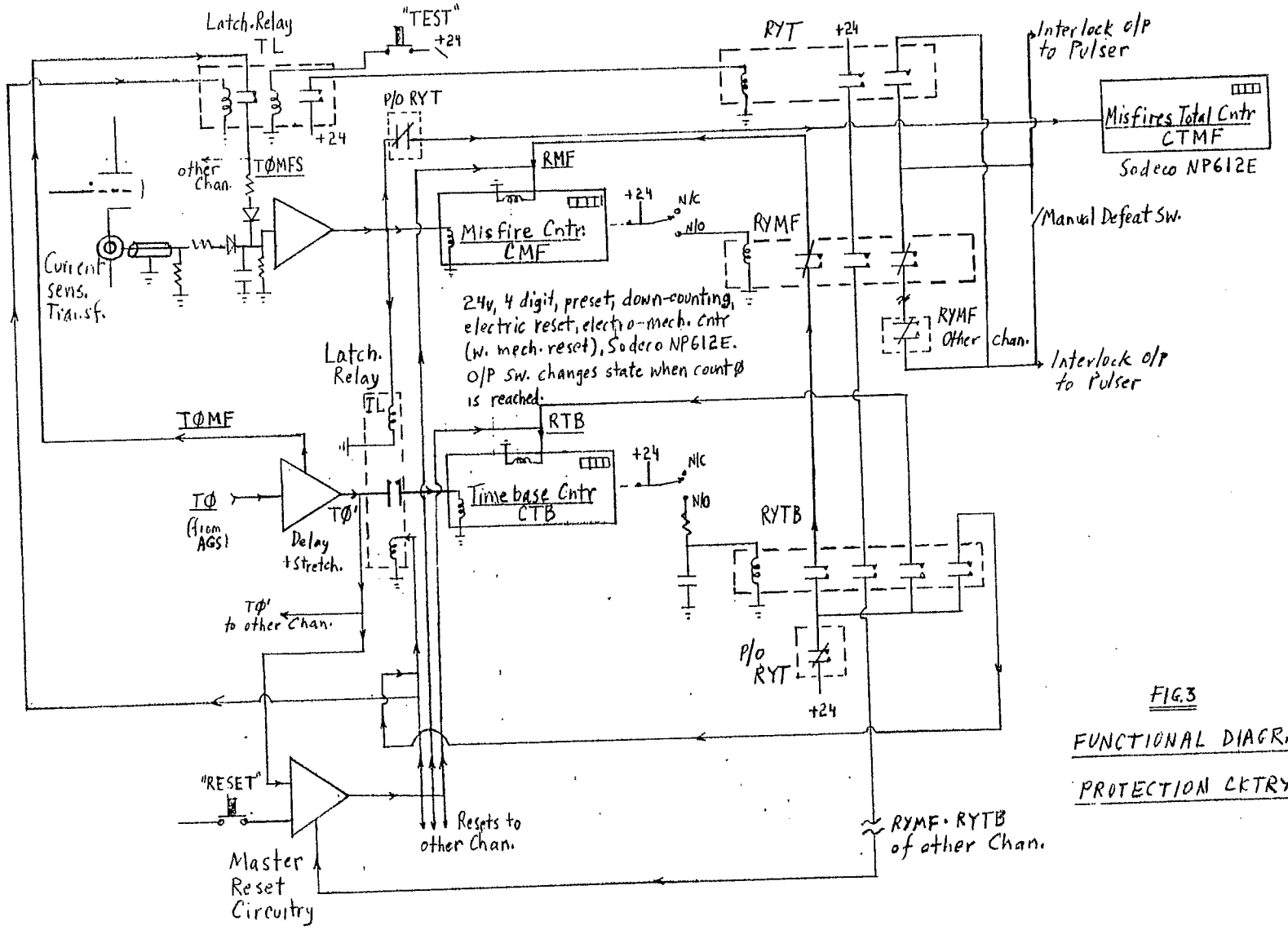


FIG.3

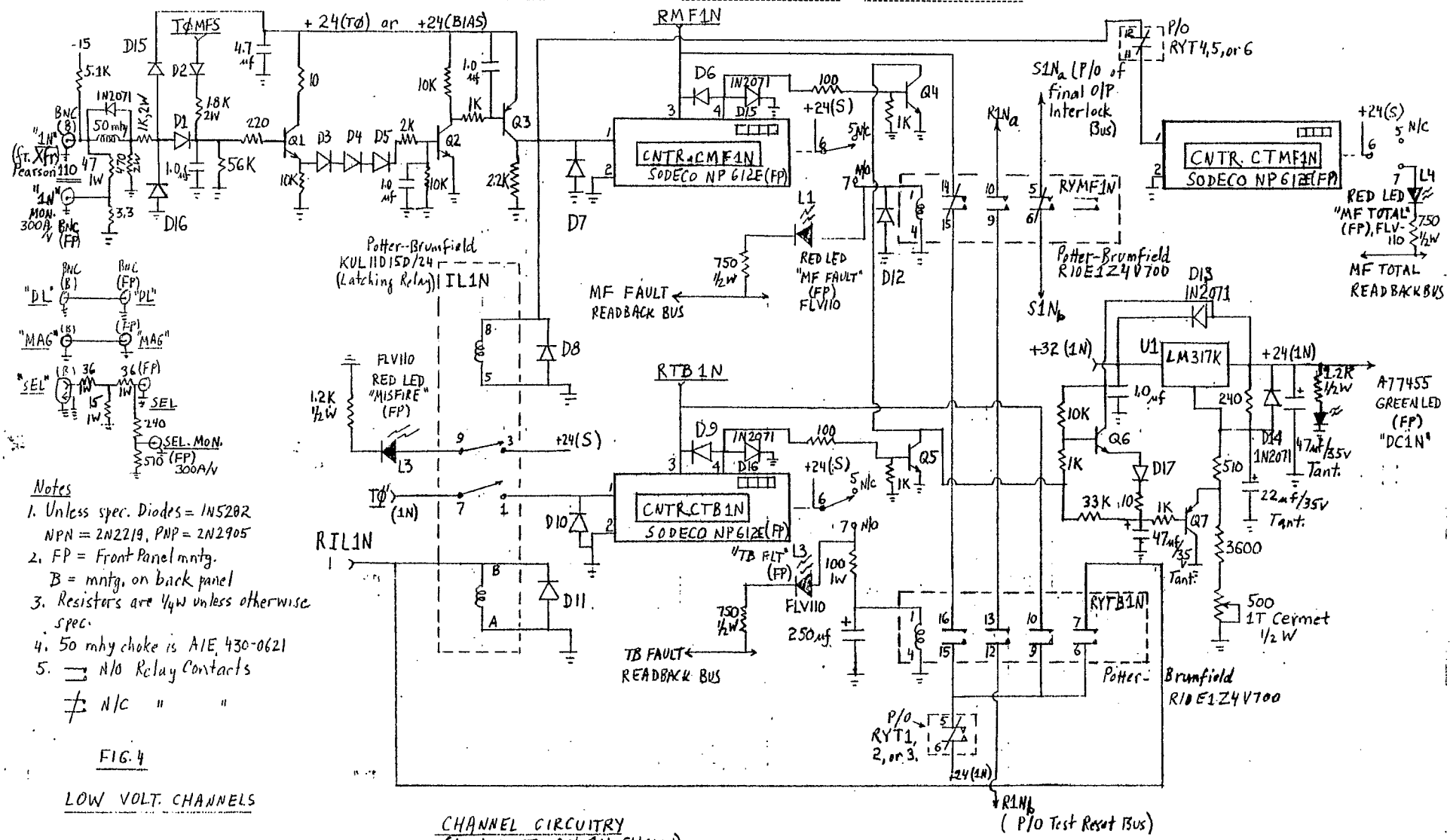
FUNCTIONAL DIAGRAM

PROTECTION CKTRY

BROOKHAVEN NATIONAL LABORATORY

BY..... DATE..... SUBJECT. LOW VOLTAGE CHANNELS (1N, 2N, 3N, 4N, 1P, 2P, 3P, 4P) SHEET NO. 1 OF 6

CHKD. BY..... DATE..... DEPT. OR PROJECT. 1N SHOWN JOB NO.



Notes

1. Unless spec. Diodes = IN5282
   NPN = 2N2219, PNP = 2N2905
2. FP = Front Panel mntg.
   B = mntg. on back panel
3. Resistors are 1/4W unless otherwise spec.
4. 50 mhy choke is AIE 430-0621
5. ⊐ N/O Relay Contacts
   ≠ N/C " "

FIG. 4

LOW VOLT. CHANNELS

CHANNEL CIRCUITRY
(LOW VOLT. CH. 1N SHOWN)

BROOKHAVEN NATIONAL LABORATORY

BY.....DATE.....
CHKD. BY.....DATE.....
.....
SUBJECT. OUTPUT CHANNELS ØP+ØN SHEET NO. 2 OF 6
ONLY MOD. FROM LOW V. CH. (SHEET 1) JOB NO.
DEPT. OR PROJECT. ARE SHOWN

1. Note that sole difference from Low-volt channels is in interface between current sensing Xformer (now Pearson) 3212) and electro-mech cntrs, as well as input latch IL.
2. Notes of sheet 1 apply.

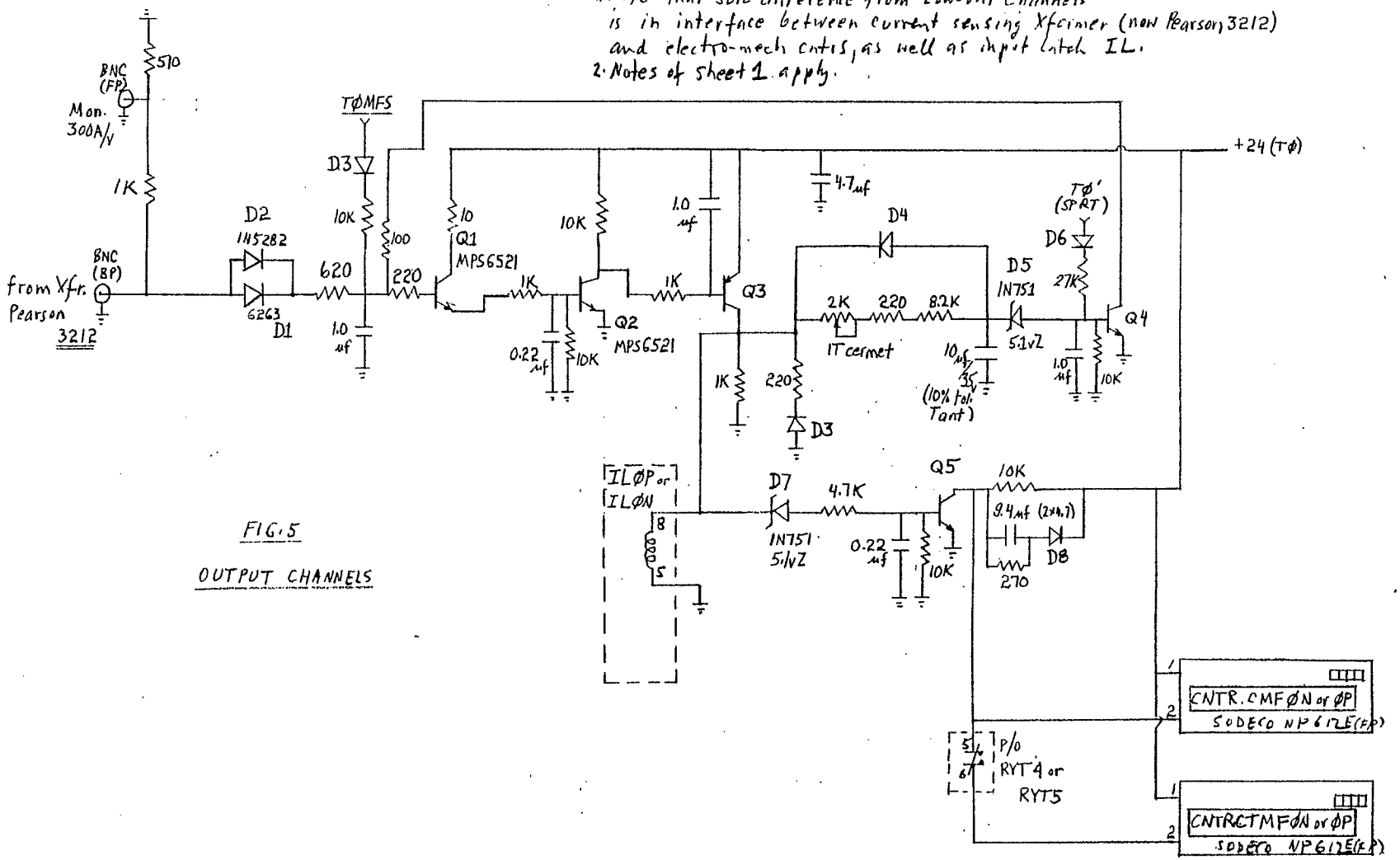


FIG. 5

OUTPUT CHANNELS

BROOKHAVEN NATIONAL LABORATORY

BY_____ DATE_____ SUBJECT TEST SYSTEM SHEET NO. 3 OF 6

CHKD. BY_____ DATE_____ JOB NO._____

DEPT. OR PROJECT._____

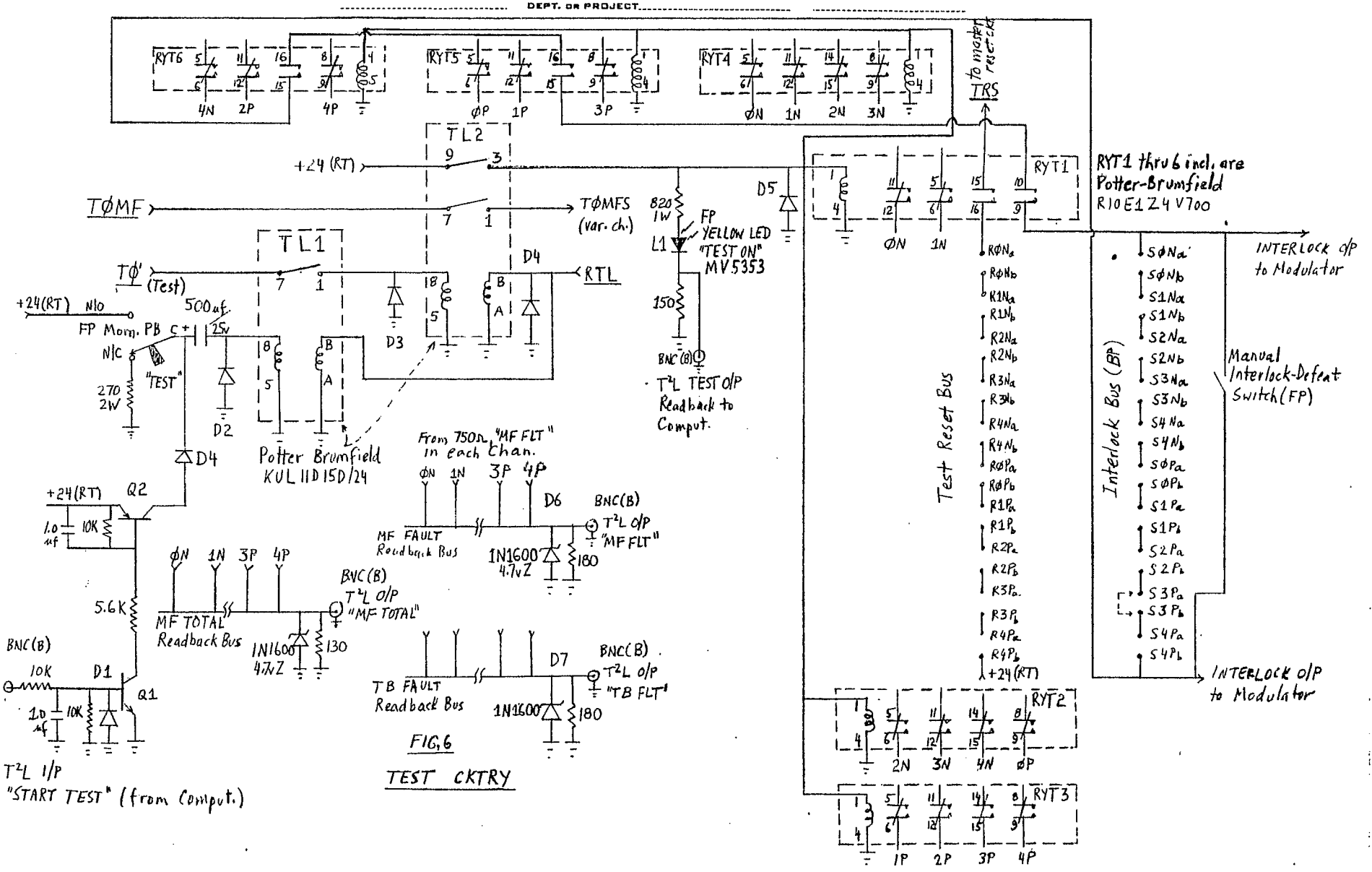


FIG. 6

TEST CKTRY

BROOKHAVEN NATIONAL LABORATORY

BY..... DATE..... SUBJECT. MASTER RESET CKTRY SHEET NO. 4 OF 6

CHKD. BY..... DATE..... JOB NO.....

..... DEPT. OR PROJECT.....

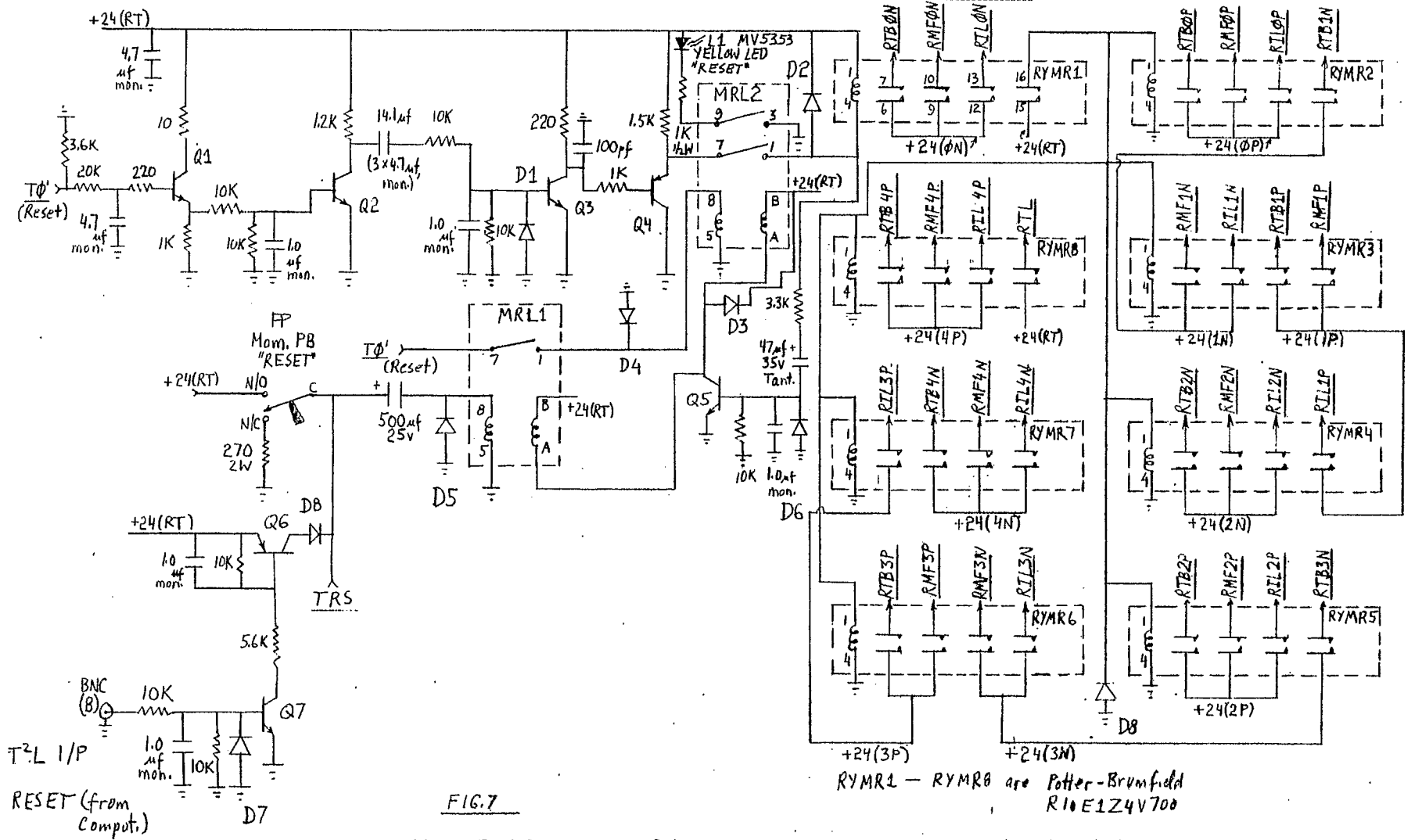


FIG.7

MASTER RESET CIRCUITRY

RYMR1 — RYMR8 are Potter-Brumfield R10E1Z4V700

LRMR1 & 2 are Potter-Brumfield KUL11D15D/24

BROOKHAVEN NATIONAL LABORATORY

BY_____ DATE_____ SUBJECT TØ' CIRCUITRY SHEET No. 5 OF 6

CHKD. BY_____ DATE_____ JOB No._____

_____ DEPT. OR PROJECT_____

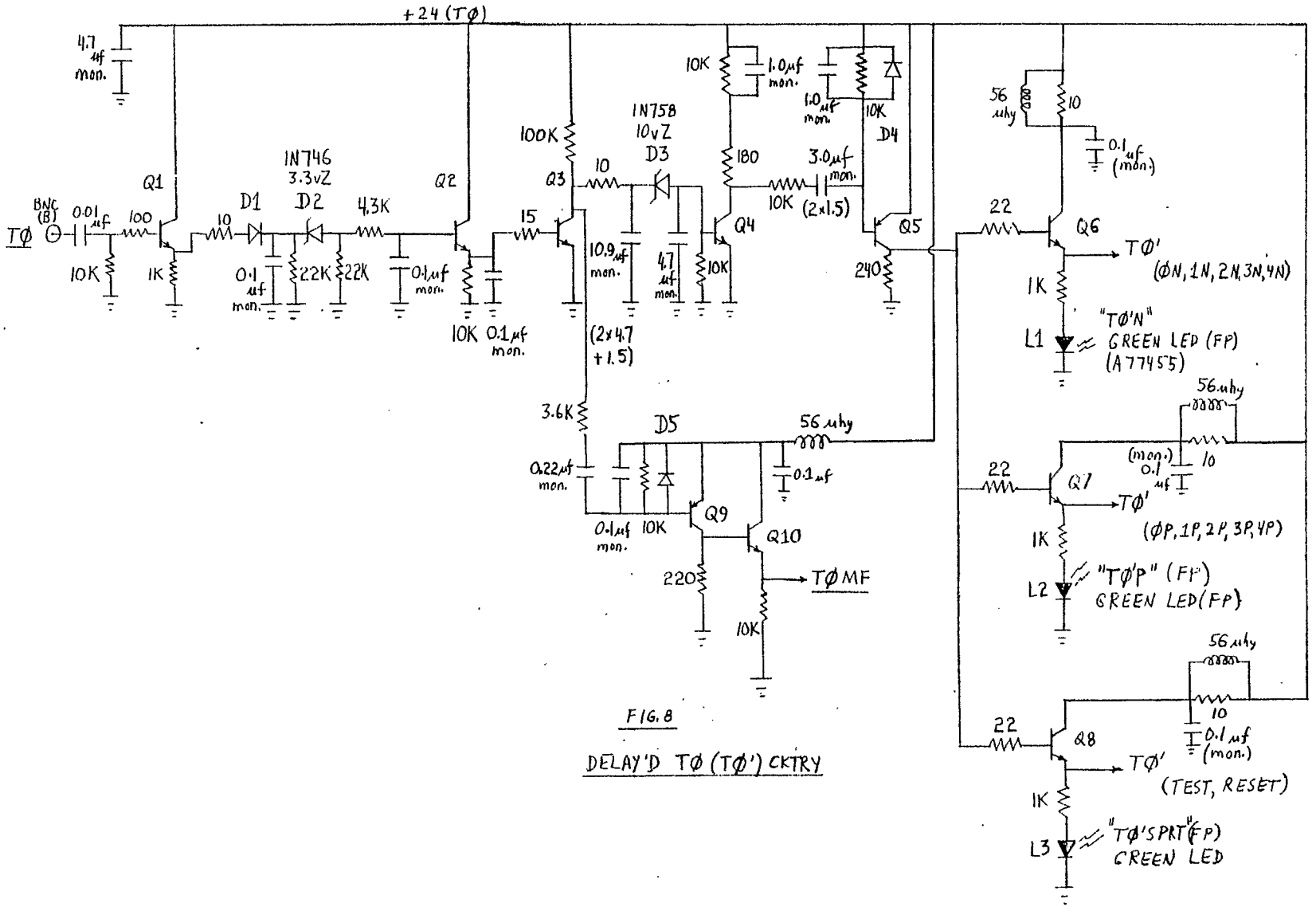


FIG. 8

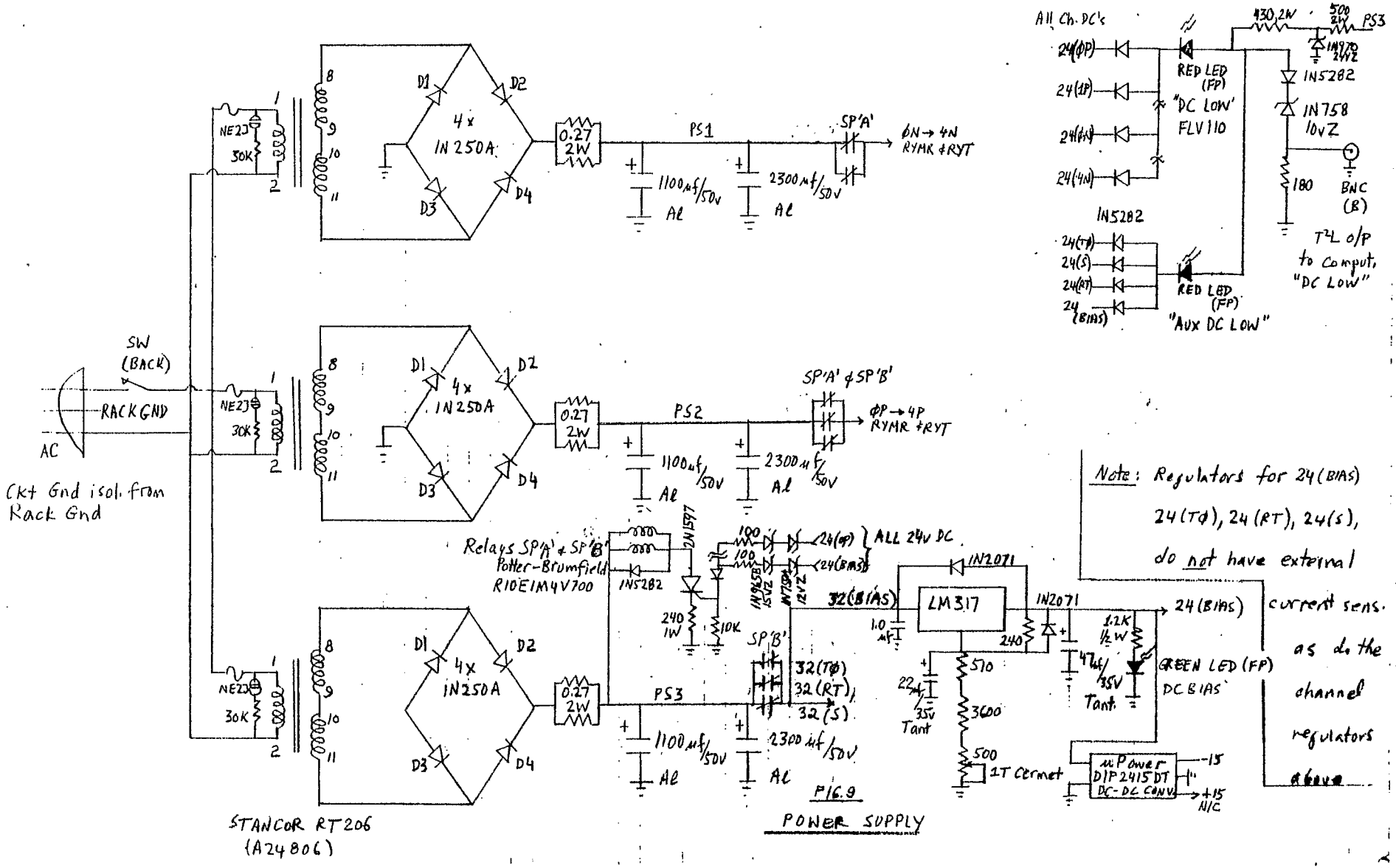
DELAY'D TØ (TØ') CKTRY

BROOKHAVEN NATIONAL LABORATORY

BY_____ DATE_____ SUBJECT POWER SUPPLY and STATUS READBACK TO COMP. SHEET No. 6 OF 6

CHKD. BY_____ DATE_____ JOB No._____

_____ DEPT. OR PROJECT_____



P16.9

POWER SUPPLY