BNL-104695-2014-TECH

AGS/AD/Tech Note No. 277;BNL-104695-2014-IR

LOW LEVEL RF DISTRIBUTION

W. Frey

March 1987

Collider Accelerator Department

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC)

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BROOKHAVEN NATIONAL LABORATORY
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Accelerator Division

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W. Frey, S. Naase, J. Woods

March 2, 1987

Introduction

The output signal (0.5 MHz to 4.5 MHz) of the Low Level RF (LLRF) source is modulated and time/frequency gated by the LLRF distribution electronics. The LLRF signal conditioning encompasses the following functions:

1. High and low frequency band split.
2. Multiplex output of the band split signals.
3. AGC of the drive signals to the high level systems.
4. Beam loading compensation.
5. Correction of cable tilt due to long transmission lines.
6. Synchronous interlock of the rf drive signals.

The LLRF distribution electronics is located in the mezzanine room (rack #4408) of the rf building (Bldg. 929). The functional assemblies are built into NIM modules. Three NIM bins are used to house and power the modules of the LLRF distribution equipment.

In general, the signal inputs and outputs of the LLRF distribution system comply with AGS and RF Group standards. The standard signals are:

1.	rf signal level	2 V p-p across 75 ohms
2.	Analog (video) signals	0 to 10 V max
3.	Pulses (triggers)	15 V max, 1 μsec, across 100 ohms

A patch panel, occupying the lower portion of rack #4408 is used to interface the LLRF distribution electronics with the AGS equipment. Figure 1 is a block diagram of the LLRF distribution electronics. Acronyms, i.e. RFM-1=rf Multiplexer-1, are used to identify individual functional modules on the block diagram.

I. LF and HF Split

The rf output (0.5 MHz to 4.5 MHz frequency range) of the LLRF source (rack #4406) is split into equal and constant amplitude signals by rf multiplexer RFM-3. Figure 2 is a block diagram of the rf multiplexer. The RFM-3 output signals have a frequency vs time function shown in Fig. 3a. Two of the outputs are fed to the Synchronous Interlock (SI) unit.

In addition to the rf drive on/off control, the SI unit gates the full range (0.5 MHz to 4.5 MHz) signals to the frequency range of the Low Frequency (LF-0.5 MHz to 2.5 MHz) and High Frequency (HF-2.5 MHz to 4.5 MHz) required by the LF and HF high level systems.

The gating is accomplished by reed relay switches controlled by two gates: a) LFRF gate from prepulse to trigger pulse L3, and b) HFRF gate from trigger pulse L2 to rf OFF trigger (SW 3 OFF), as shown in Figs. 3b and 3c. Note that there is an overlap when both the high level systems have rf applied. The overlap is the "hand off" in the acceleration cycle from the LFHL to the HFHL systems.

The gated outputs of the SI unit are fed to respective LF and HF multiplexers (RFM-1 and RFM-2). The outputs of these multiplexers is shown in Figs. 3d and 3e.

II. LFRF

The LFRF output from the SI unit is split into 4 equal signals by an rf multiplexer (RFM-1). The signals include a tuning signal, power amplifier drive signal, and monitor signals.

A. Tuning Signal

One output of the multiplexer (RFM-1) provides the rf signal for the cavity tuning bias supply. The LFHL system is located in Building 914, nominally 1230' (cable length) away. This length of RG-59 cable has attenuation proportional to frequency. This will result in 2.95 dB insertion loss at 0.5 MHz and 6.64 dB at 2.5 MHz.

A Compensating Line Drive, CLD-1A, is used to condition the tuning signal for the cable insertion loss and tilt. Thus, the signal at the end of the 1230' of cable will be a constant 2 V peak-to-peak from 0.5 MHz to 2.5 MHz.

Figure 6 is a block diagram of the Compensating Line Driver. The cable attenuation tilt is approximated by a frequency dependent attenuator (R-C voltage divider), and its output is used to control an amplifier. The amplifier will preemphasize the output to anticipate the cable attenuation. The limiter stage before the R-C divider is used to remove any amplitude variations/modulation from the signal. There are two identical but independent channels in each CLD unit. There are two CLD units in the LFRF designated CLD-1 and -2. Figure 4a illustrates a typical CLD output.

B. Power Amplifier Drive

Another output of RFM-1 provides the rf input signal to an AGC'd amplifier that supplies rf drive signal to the LFHL power amplifier located in Building 914. The AGC'd amplifier (ARF) adjusts the rf signal amplitude to maintain the desired gap voltage at the accelerating gap. The gain of the ARF is determined by the AGC input signal. Figure 7 is a block diagram of the ARF unit.

A soft clamp (i.e. the output is limited to a low value less than 1 kV at the gap), is provided to allow trouble-shooting under fault conditions. The soft clamp is actuated by switching the EXT INHIBIT line from 5 V to ground. A filter, followed by a detector, is used to monitor the signal input, and if the signal falls outside of the 0.4 - 2.6 MHz frequency range, the clamp will be actuated.

The AGC signal is developed by comparing the detected gap volt signal from the cavity with the desired gap volt function. The difference of these signals is used to generate the AGC voltage signal. The comparison is accomplished in the AGC Amplifier (AA-1) unit. There are two AA units used: one for the LFRF, and one for the HFRF. Figure 8 is a block diagram of the AA unit. *Figures 4b-4e are typical signals of the AA and ARF units.*

A CLD channel is used to remove the cable attenuation and tilt from the LFHL-RF drive signal. Figure 4f illustrates the output of CLD-2A.

C. LFRF Test Signal

A sample of the tuning rf drive signal and a sample of the power amplifier drive signal are available in the Main Control Room (MCR) in Building 911. Again, CLD's are used to remove cable attenuation and tilt. The gain and tilt adjustments are made to compensate for the RG-59 cables between the mezzanine and the MCR.

D. Local Test Signal

The fourth output of RFM-1 is available for local testing of the tuning rf signal.

III. HFRF

The HFRF output from the SI is split into four equal signals by RFM-2.

A. Tuning Signal

One of the outputs from RFM-2 provides the rf drive signal for the High Frequency High Level (HFHL) rf Main Tuning System (MTS) power supply. This signal is routed through the HFHL control console on the main floor of Building 929. Since the cable run is short, a CLD is not used.

B. HFHL Amplifier Drive

One of the outputs of RFM-2 provides the signal input to the Boussard Beam Compensation (BBC) chassis. This chassis is comprised of seven modules:

1. input/output
2. phase shifter #1 (injection)
3. phase shifter #1 control
4. phase shifter #2 (extraction)
5. phase shifter #2 control
6. phase shifter #3 (not installed)
7. phase shifter #3 control (not installed)

The operation of the BBC is essentially the same as the unit described in Reference A.

This unit differs from the original described in Reference A by the incorporation of $\pi/2$ switching in addition to the π switch. In addition, this BBC is controlled by a RELWAY interface. The RELWAY control interface is described in Reference B.

An AGC Amplifier (AA-2) is used to develop the AGC voltage for the BBC. AA-2 compares the sum of the 10 accelerating cavity gap volts to the gap voltage function and derives the AGC signal.

The output from the BBC is routed to the HFHL predriver via the HFHL control console. Figures 5b-5e are typical waveforms for the BBC.

C. HFRF Test Signal

A sample of the tuning signal from RFM-2, and a sample of the BBC output (HFHL drive signal) are available in Building 911. These signals are conditioned by CLD-3 to remove cable attenuation and tilt due to the long cable run between Buildings 929 and 911.

D. Local Test Signal

In addition, the fourth output of RFM-2 is available for local monitoring of the HFRF tuning signal.

IV. Reference Documents and Drawings

A. AGS Technical Note #201, "Operation Note Boussard Beam Compensation", W. Frey.

B. AGS Controls Group Note AGS/IN/85/041, "Auxiliary Low Level RF Controller", T. Tallerico

C. Drawings:

1. D06-E489-5 Block Diagram, Utility Cabinet 929 Mezzanine
2. D06-E422-5 Schematic Diagram Beam Compensation Input Module
3. D06-E423-5 Schematic Diagram Beam Compensation Phase Shift Module
4. D06-E437-5 Schematic Diagram BBC Interface Module
5. D06-E464-3 Schematic Diagram AGC Amplifier, High Level rf System (type 2)
6. D06-E481-4 Schematic Diagram rf Multiplexer
7. D06-E482-4 Schematic Diagram Compensated Line Driver

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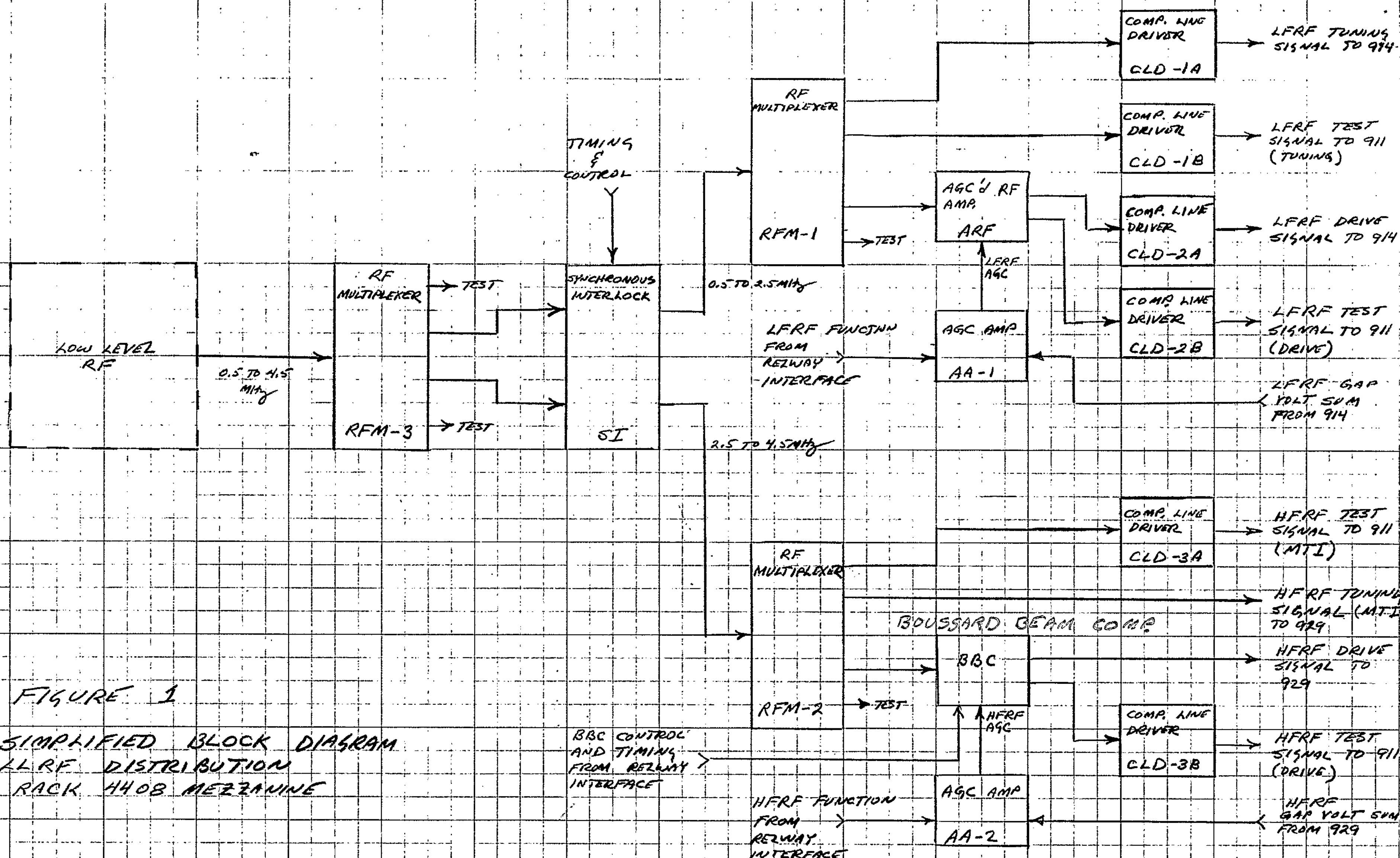


FIGURE 1

SIMPLIFIED BLOCK DIAGRAM
LLRF DISTRIBUTION
RACK 4408 MEZZANINE

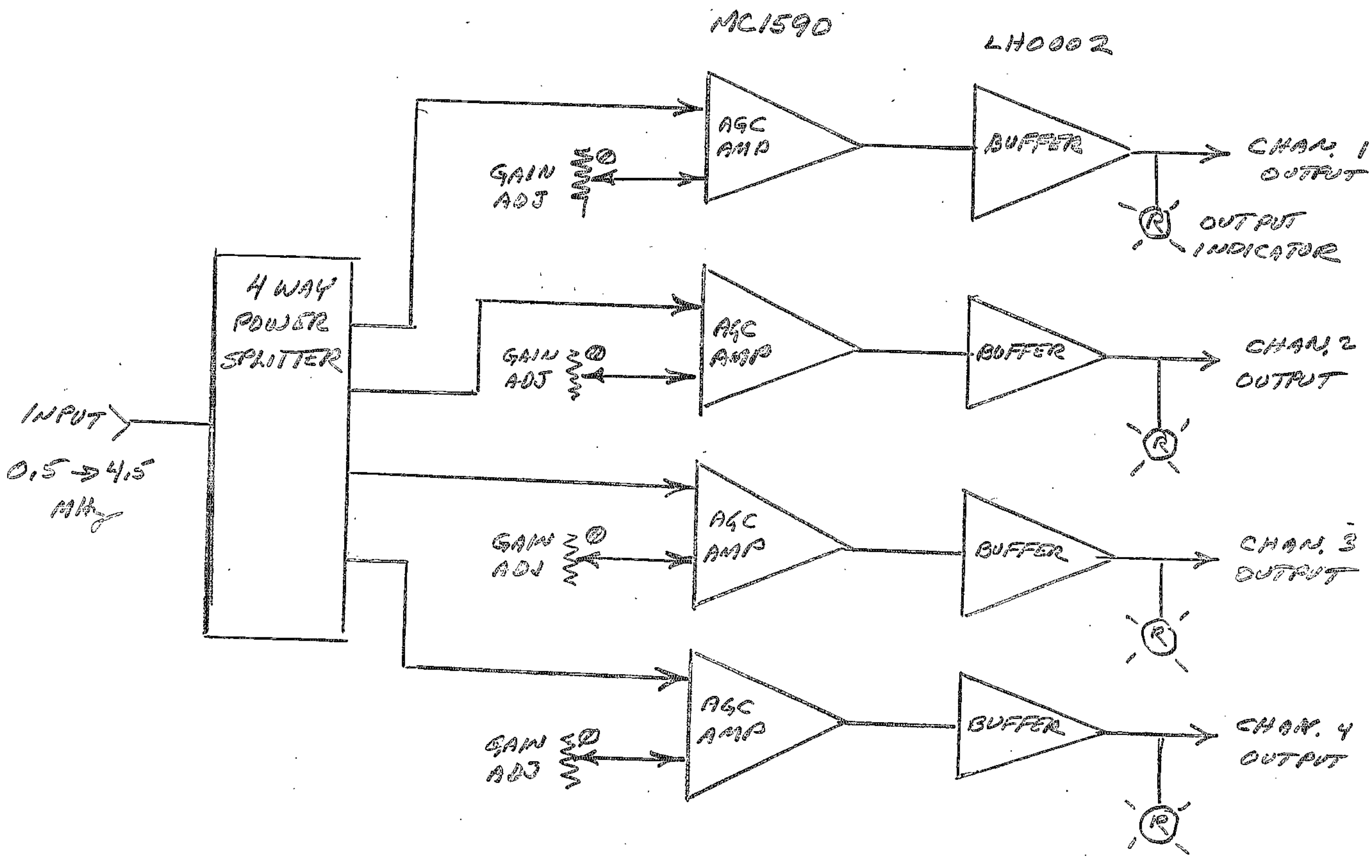
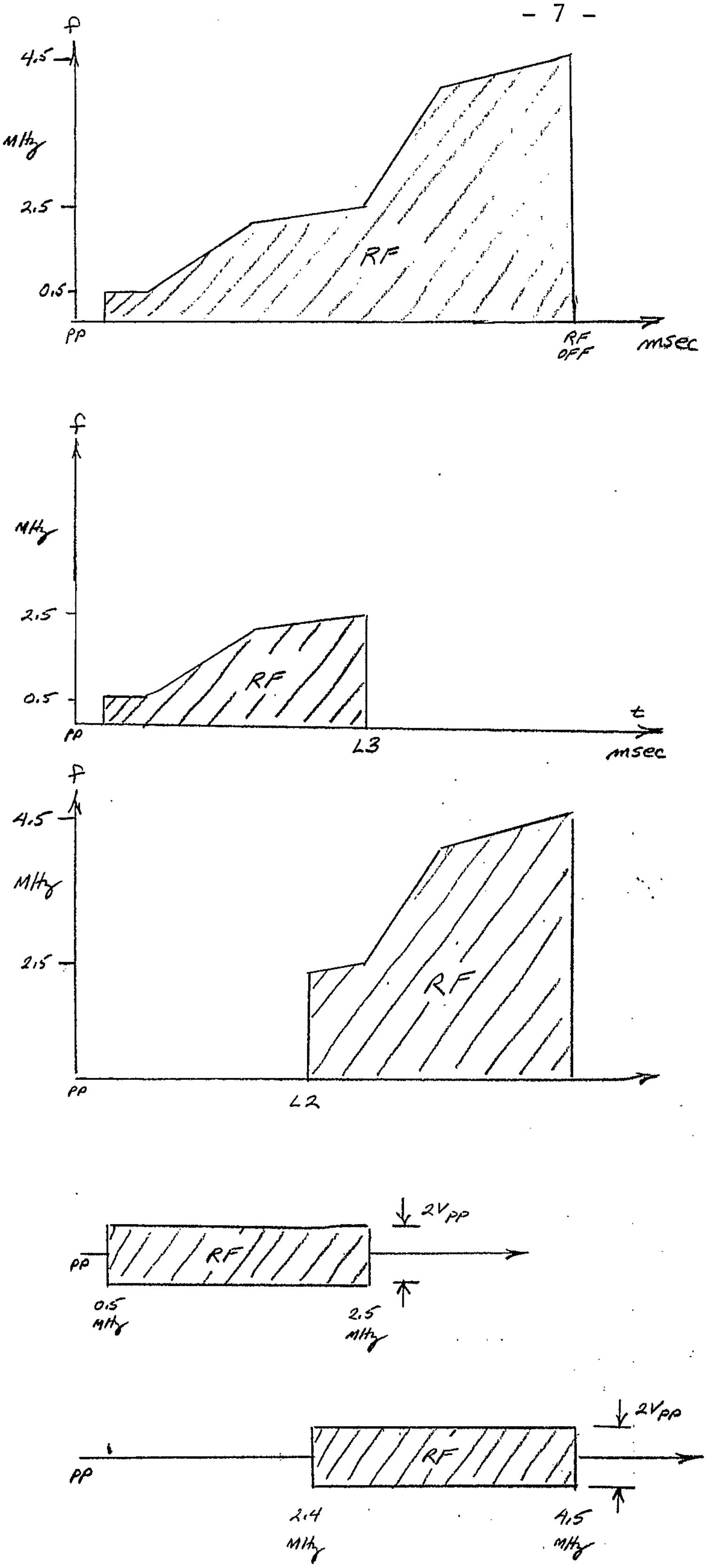


FIGURE 2
SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM
RF MULTIPLEXER



a. LLRF SOURCE FREQUENCY/TIME FUNCTION

b. LFRF OUTPUT FROM SYNCHRONOUS INTERLOCK

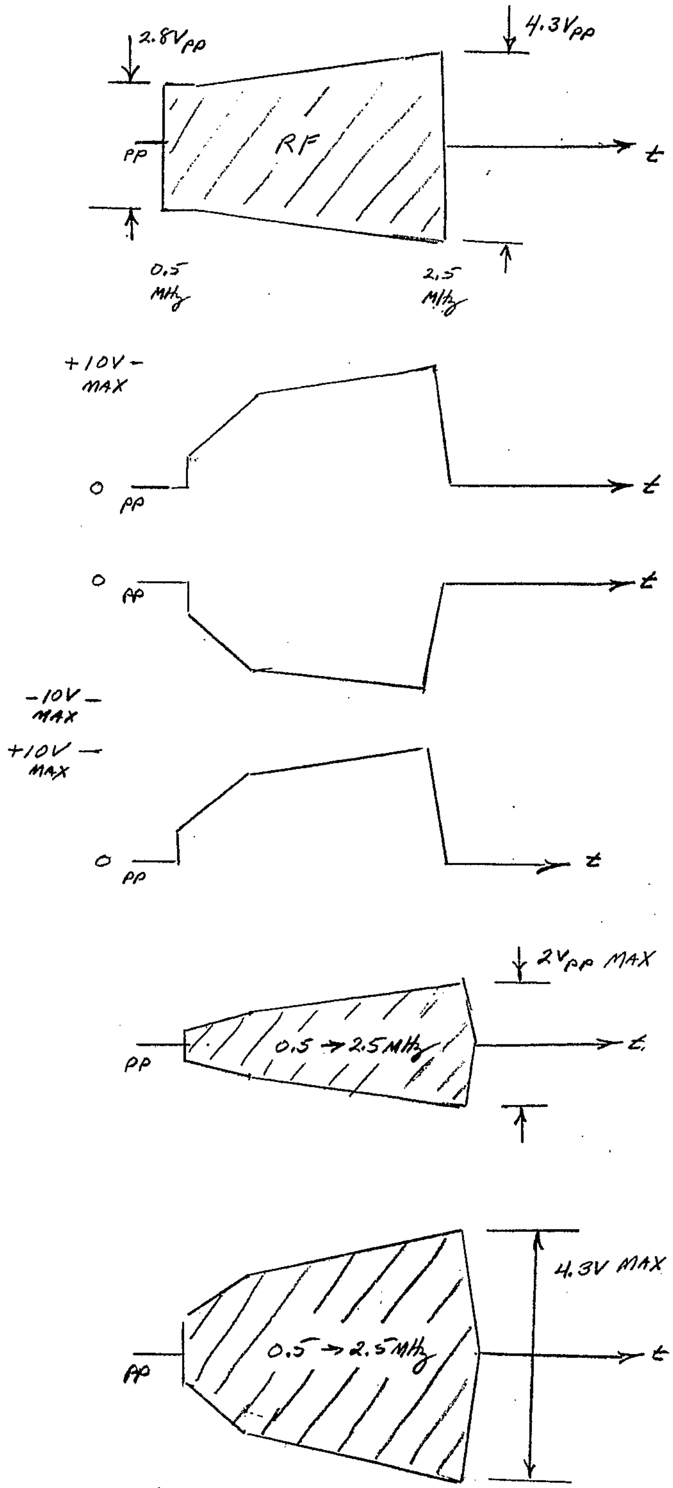
c. HFRF OUTPUT FROM SYNCHRONOUS INTERLOCK

d. TYPICAL RFM-1 OUTPUT - LFRF

e. TYPICAL RFM-2 OUTPUT - HFRF

FIGURE 3 TYPICAL WAVEFORMS

NOTE: ALL WAVEFORMS AND VALUES ARE APPROXIMATE (MAY BE EXAGGERATED) FOR ILLUSTRATIVE PURPOSES ONLY.



a. LFRF TUNING SIGNAL - CLD 1A OUTPUT

b. LFRF FUNCTION (DESIRED GAP VOLTS)

c. LFRF GAP VOLT SUM - FROM CAVITY

d. LFRF AGC SIGNAL -- A(g-h)

e. LFRF AGC'D AMPLIFIER OUTPUT (2Vpp MAX = FULL POWER OUTPUT AT LOAD)

f. OUTPUT FROM COMPENSATED LINE DRIVER

FIGURE 4.
TYPICAL WAVEFORMS CONTINUED

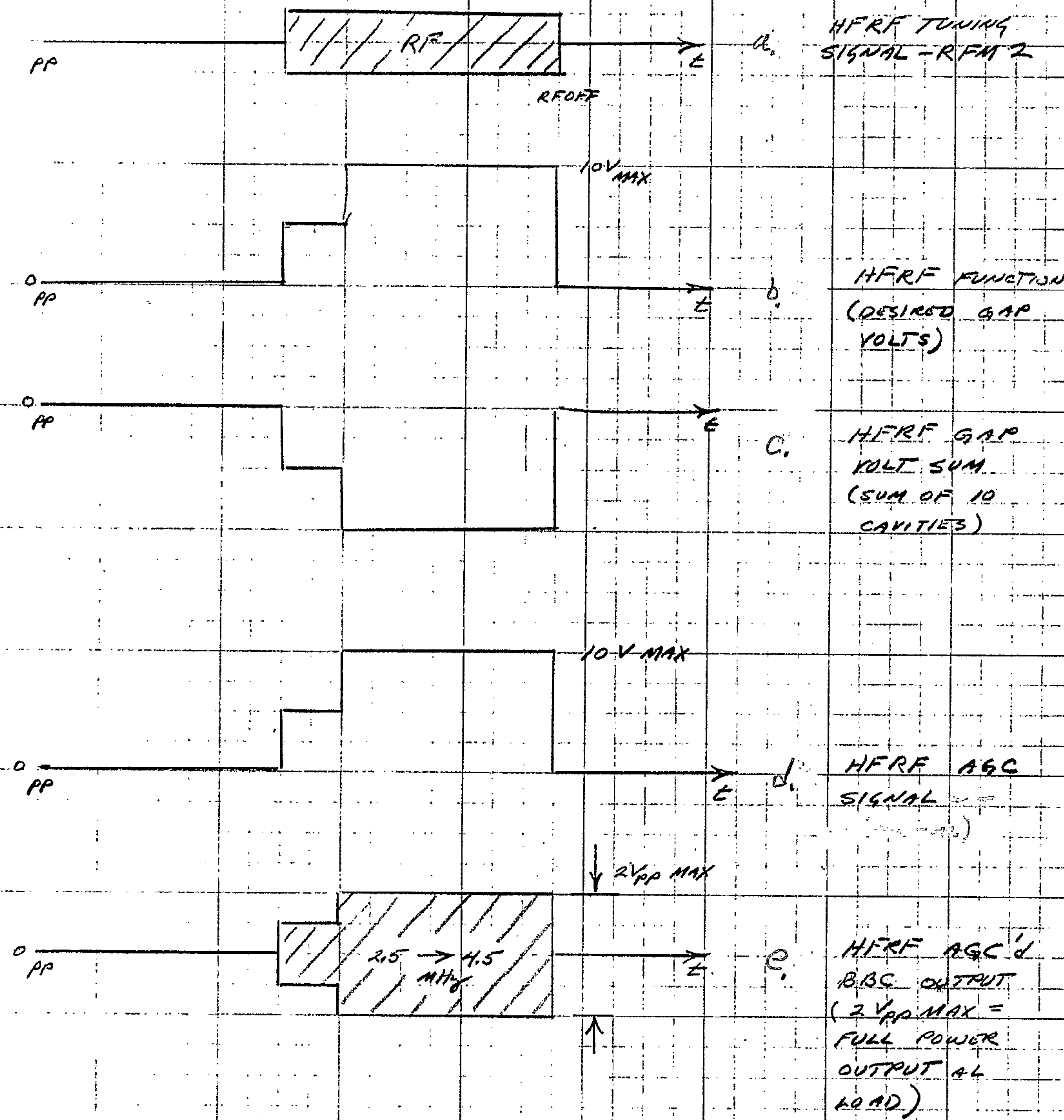


FIGURE 5

TYPICAL WAVEFORM CONTINUED

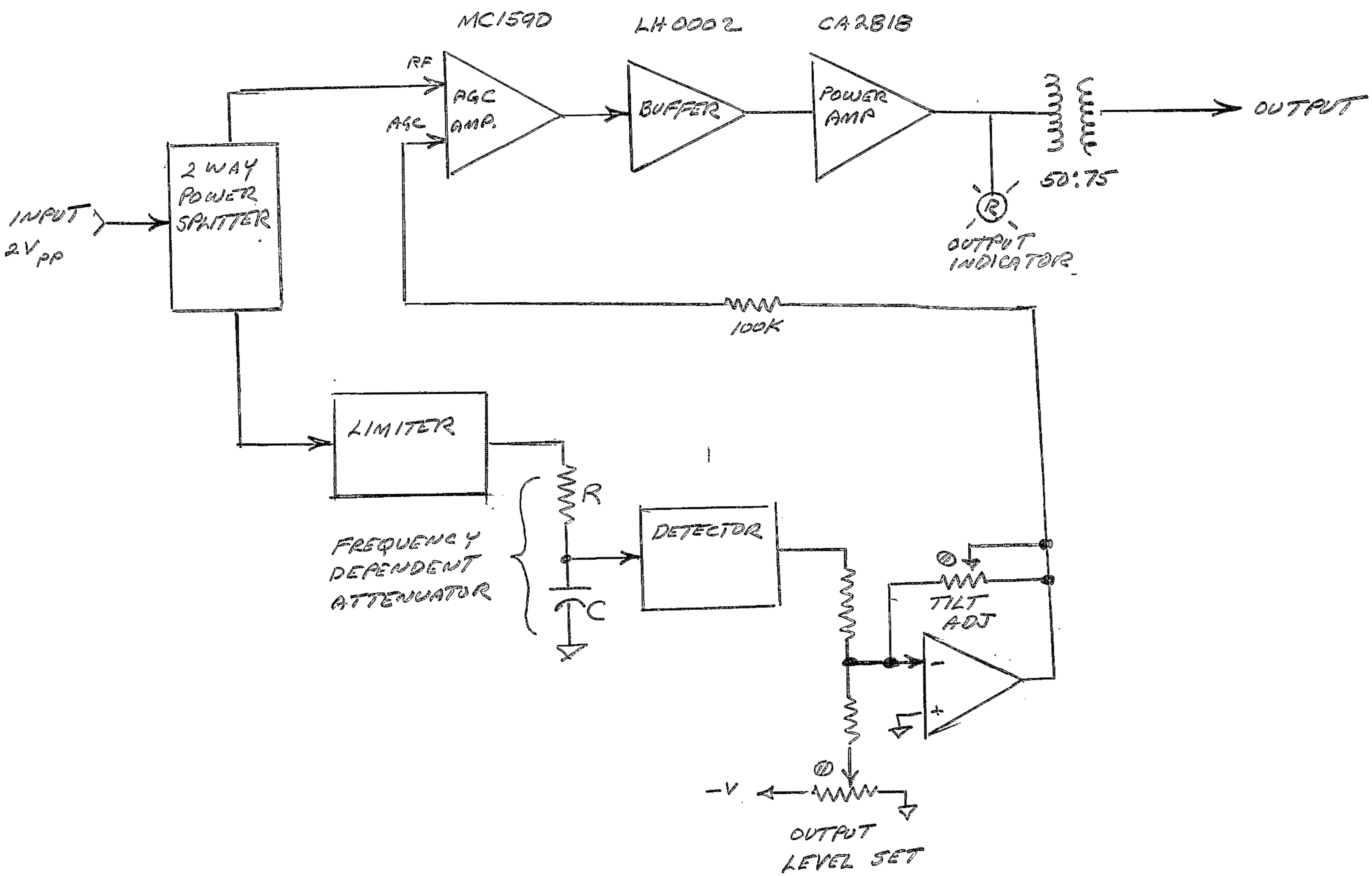


FIGURE 6

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM
COMPENSATED LINE DRIVER
(CLD)

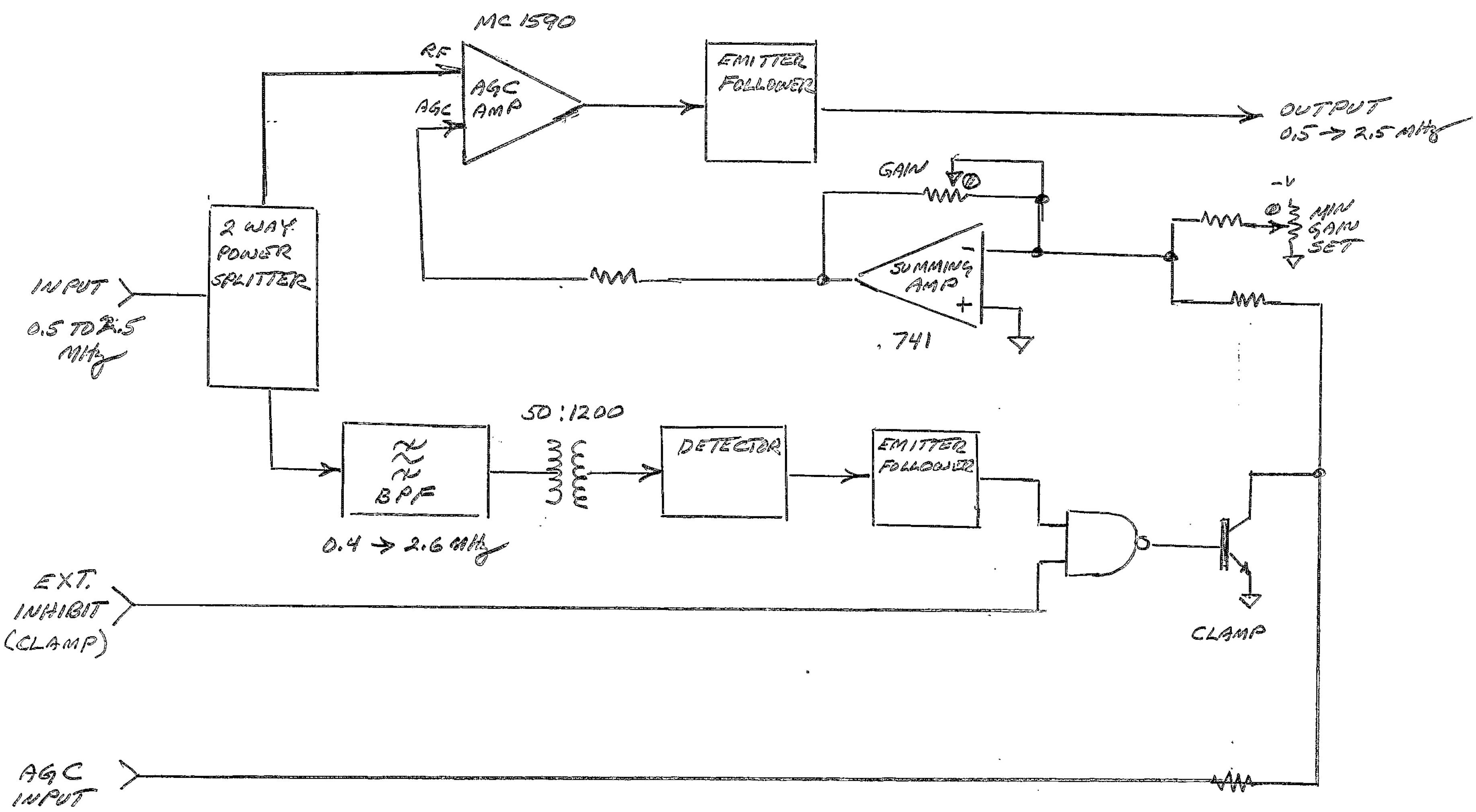


FIGURE 7
SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF AN AUTOMATIC GAIN CONTROLLED (AGC 'd) AMPLIFIER, (ARF)

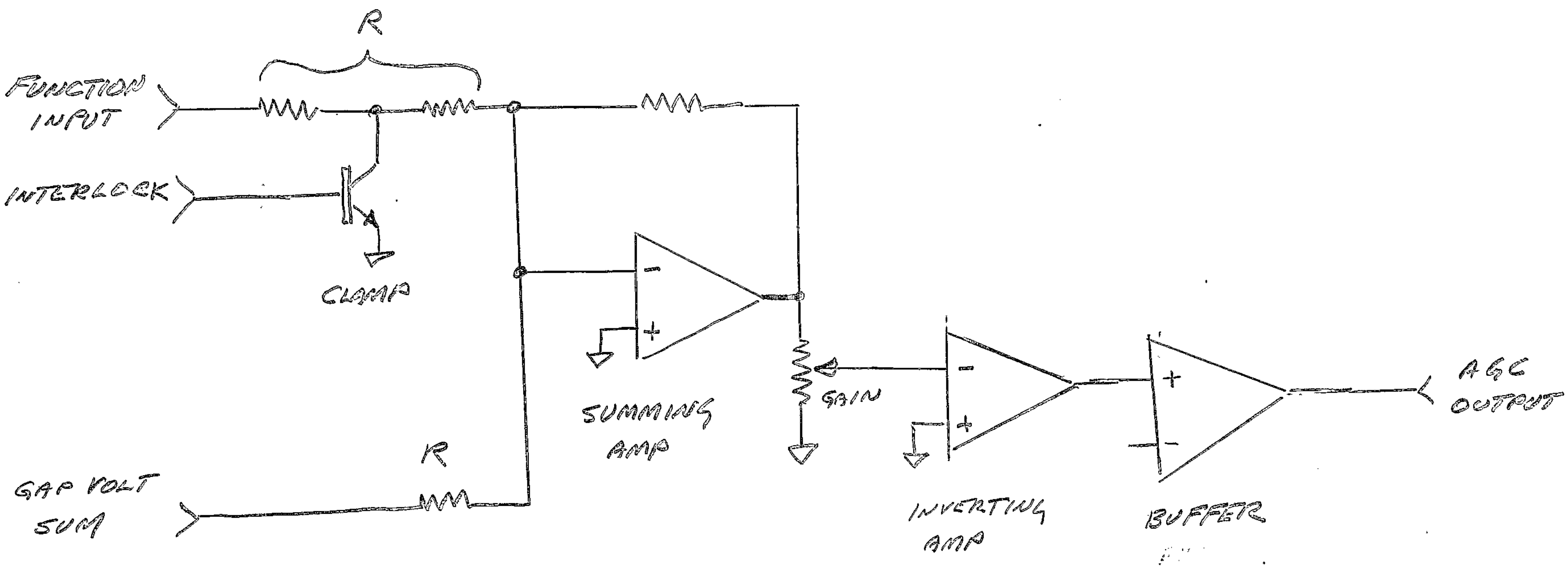


FIGURE 8
SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM
AGC AMPLIFIER (AA)