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STATUS OF THE AGS TRANSVERSE DAMPER

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Accelerator Division
Technical Note

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STATUS OF THE AGS TRANSVERSE DAMPER

by

The Damper Crew

(P. Yamin with the help of P. Cameron, Y.Y. Lee,
B. Oerter, E. Raka, V. Wong, Dexun Xi, A. Zhang)

June 14, 1991

I. INTRODUCTION

As the intensity of the AGS is increased, the amplitude of coupled-bunch oscillations grows faster than the natural damping. After the Booster becomes operational and intensities greater than 4×10^{13} become routinely available, it will be necessary to actively damp these oscillations if beam losses are to be kept acceptably low. The Transverse Damper (TD) will perform this function. The bandwidth and power requirements are calculated elsewhere.[1]

In the coupled-bunch mode, each rf bunch is affected by the wakefields of the previous bunches and performs transverse oscillations about the equilibrium orbit at the betatron frequency. In the lowest order mode, each bunch oscillates as a coherent whole; in higher order modes, for example, the head and tail of each bunch can oscillate at the same frequency but 180° out of phase. The TD as presently implemented can only damp the coherent, lowest order mode. The position of the center-of-charge of each bunch is measured as it passes a pickup, and from this measurement the TD generates a correction signal which is applied to a kicker one revolution later.

Each bunch generates signals as it passes vertical and horizontal pairs of pick-up electrodes (PUEs). Cathode followers (CFs) on each of the four electrodes match the impedance to cables leading out of the AGS ring. Here, a hybrid circuit (H) forms the sum (Σ) [up + down, left + right] and difference (Δ) [up-down, left-right] signals of electrode pairs. Σ and Δ are integrated for an entire bunch width in (I), and these integrated signals are digitized and processed in the digital processor (DP). The sequencing of these operations is controlled by the timing generator (TG) which is synchronized with the low-level AGS rf and phase-locked to the bunches. The DP first computes the Δ/Σ ratios for both the vertical and horizontal signals, and from these ratios then calculates the bunch positions and the appropriate correction signals. The results of these computations are retained in memory for one revolution and then are applied to D/A converters which drive four power amplifiers (PAs) feeding the four strip-line (SL) kicker electrodes. Figure 1 illustrates these principles of operation.

II. THE SYSTEMS

The transverse damper is composed of several subsystems--each designed separately, and each in a different place on the road to completion. This complicated situation was caused by the way in which engineering resources had to be scrounged in the early stages of the project. Nevertheless, it is all coming together.

a. PUEs and SL

The PUEs are based on the "conversion" design, and the SL is a 50-Ohm transmission line based on a CERN design. These components are essentially complete mechanically, but checking the electrical characteristics of the SL remains to be done. Installation will take place in the AGS F20 straight section during the 1991 summer shutdown. The PUEs, SL, and the arrangement in the straight sections are illustrated in Figures 2, 3, and 4.

b. Front End Electronics

This system requires the most work. The PUEs must be matched to the transmission lines through cathode followers (or a suitable passive network), and connected to integrating/baseline restoring circuits. None of this has been designed. While visiting Brookhaven in April, 1991, Elmar Schulte developed a conceptual plan for a system employing passive matching (with restricted low frequency response) coupled to a synchronous detector/integrator which recovers the low frequencies from their sidebands. Intensive work is still required.

c. Timing Generator

A TG was designed and built by Dexun Xi while he was a visitor in the Instrumentation Division. Preliminary testing has been completed, but further evaluation is required. Figure 5 is a simplified logic diagram. The AGS rf appears as input to Mixer 1, where it is raised to the 12.5-14.5 MHz range, passing through a band pass filter, BPF7. A pickup is used to determine the phase of the bunches and the PLL controls a voltage-controlled amplifier (VCO) which runs at 16 times the rf frequency. The output of this amplifier provides the timing signals.

d. Digital Processor

The DP includes the D/A converters which follow the integrators. It normalizes the PUE signals, calculates the deviation from the mean closed orbit, and uses a transfer function which is downloaded from the control system to calculate the correction signal. The digital data are stored for one revolution, and the timing is adjusted to compensate for the changing rotation frequency during the acceleration cycle. Provision is made for "anti-damping" one bunch to facilitate a tune measurement, and a local memory can store the damping data for a substantial portion of the acceleration cycle in order to provide diagnostic information. Figure 6 shows the DP logic.

Horizontal and vertical DPs are required. One is about 90% complete, and all the components are on hand to complete both units. No testing has been performed.

e. Power Amplifiers

In order to drive each of the four 50-Ohm strip lines to the approximately 200 Volts necessary for adequate damping time, a peak power of about 1 kW per line is required. This means that we need four PAs (plus a fifth spare) with a bandwidth of about 20 KHz-200 MHz. Such amplifiers are commercially available from several manufacturers at a cost of about $15,000 each. Because of the amount of the purchase (~ $75,000), a bidding process must be initiated.

f. Software

The applications (Apollo) software will control the TD, principally through an interface to the DP. Modes of operation will include: damping all bunches; anti-damping one bunch (for a tune measurement); and tracking selected bunches for an extended period. Although the hardware is specified and mostly built, work has yet to begin on the software. This will require a major effort.

III. STATUS, RESPONSIBILITIES, AND SCHEDULE

The following table indicates the assignments of responsibilities for the various aspects of the damper fabrication.

SYSTEM INTEGRATION	MECHANICAL	FRONT-END	DIGITAL	AMPS	SOFTWARE
Yamin Oerter	Cameron	Smith Ciardullo	Oerter	Zhang	Yamin Luccio

We have established a schedule and milestones for the completion of the damper, and they appear below. The reader should note that as of today (6/7/91), we are already behind.

	4/91 – 7/91	7/91 – 10/91	10/91 – 1/92
SOFTWARE	Algorithm	Code	Test
CONTROLS	Detailed Design	Assemble	Install
ELECTRONICS	Detailed Design	Assemble	Install
MECHANICAL	Assemble	Install	

References

1. E. Raka, AGS Technical Note (in preparation).

THE AGS DAMPER

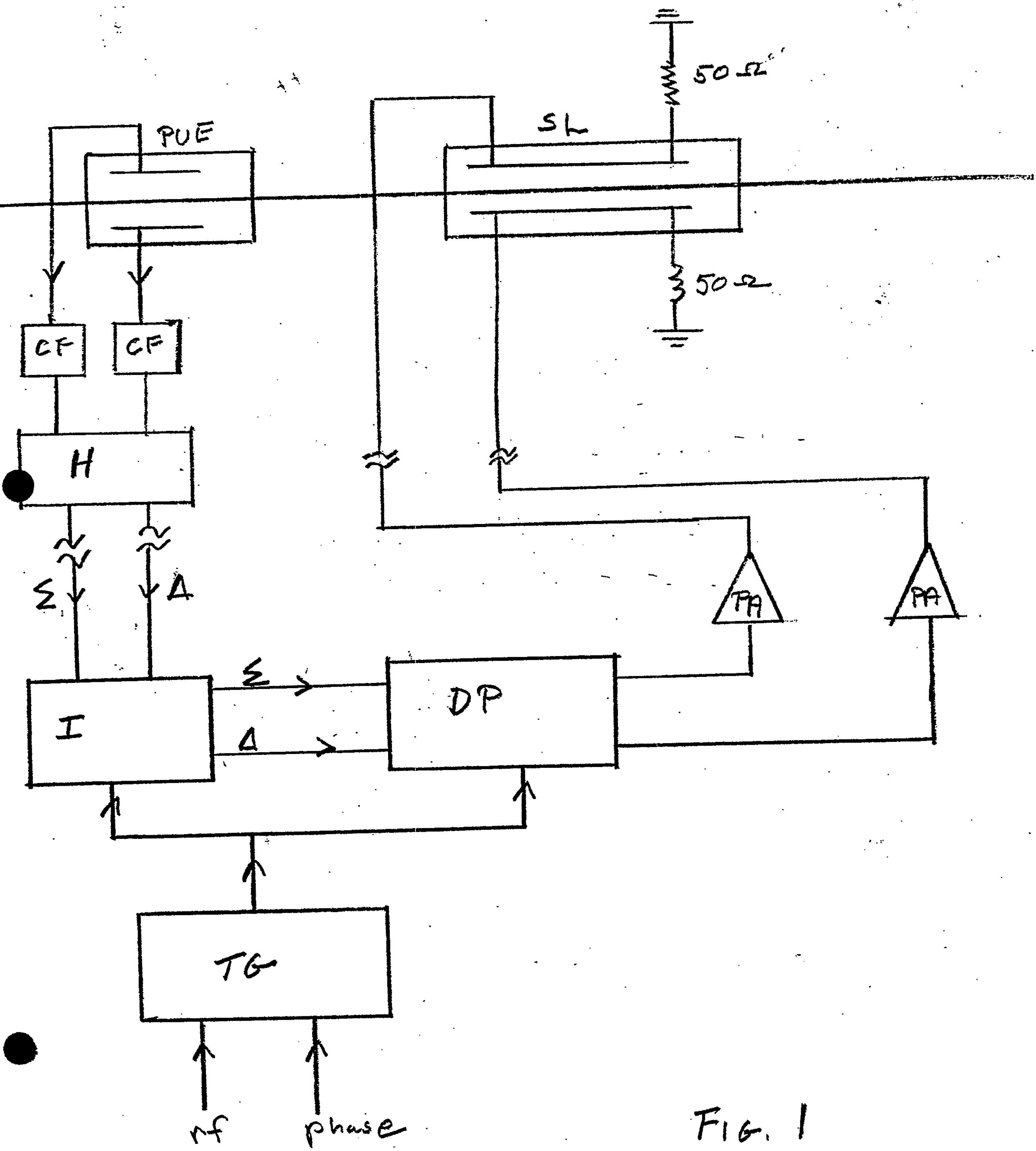
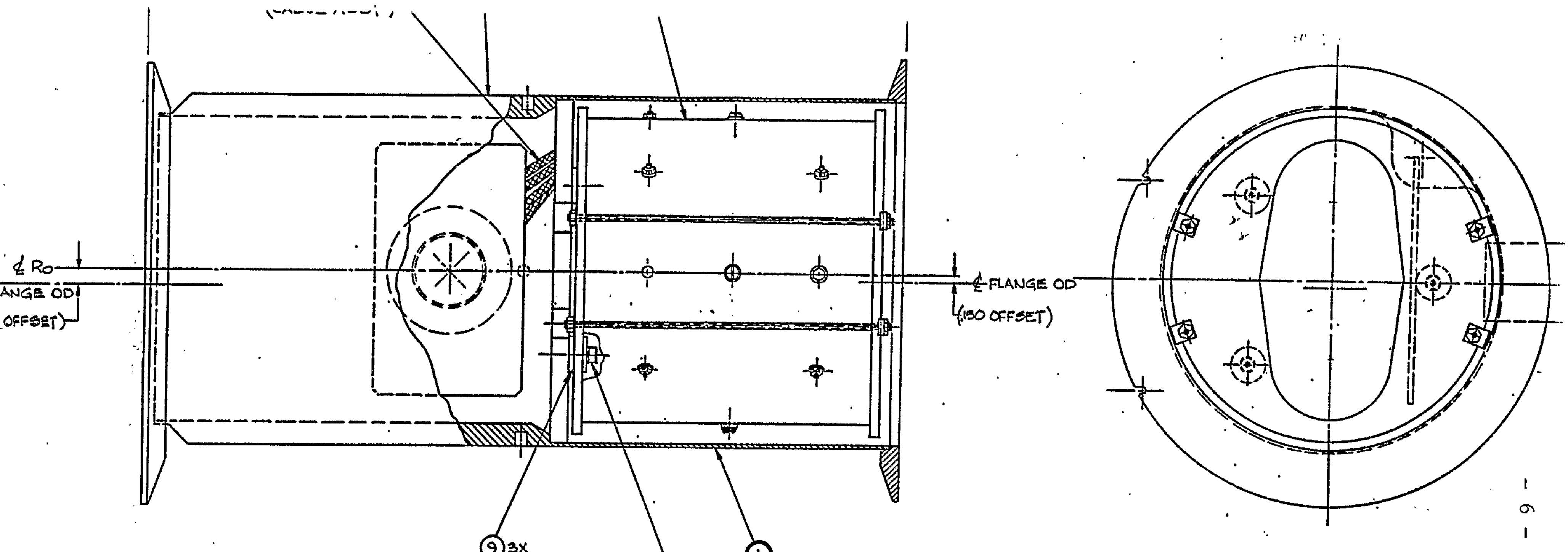
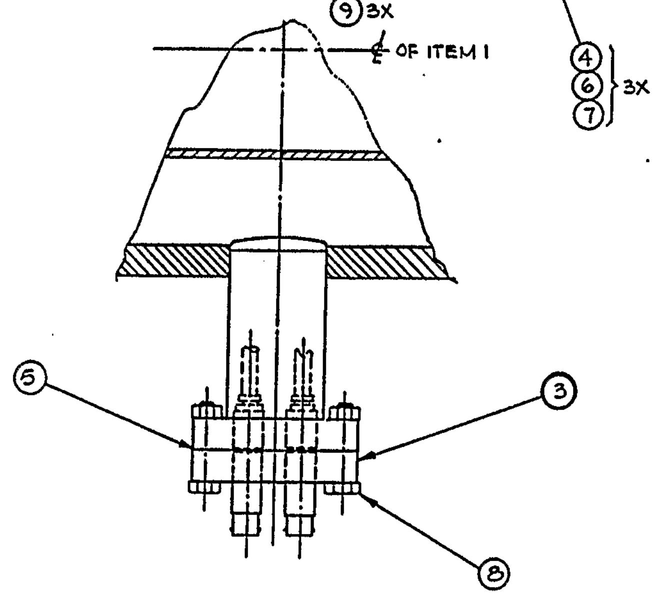


FIG. 1





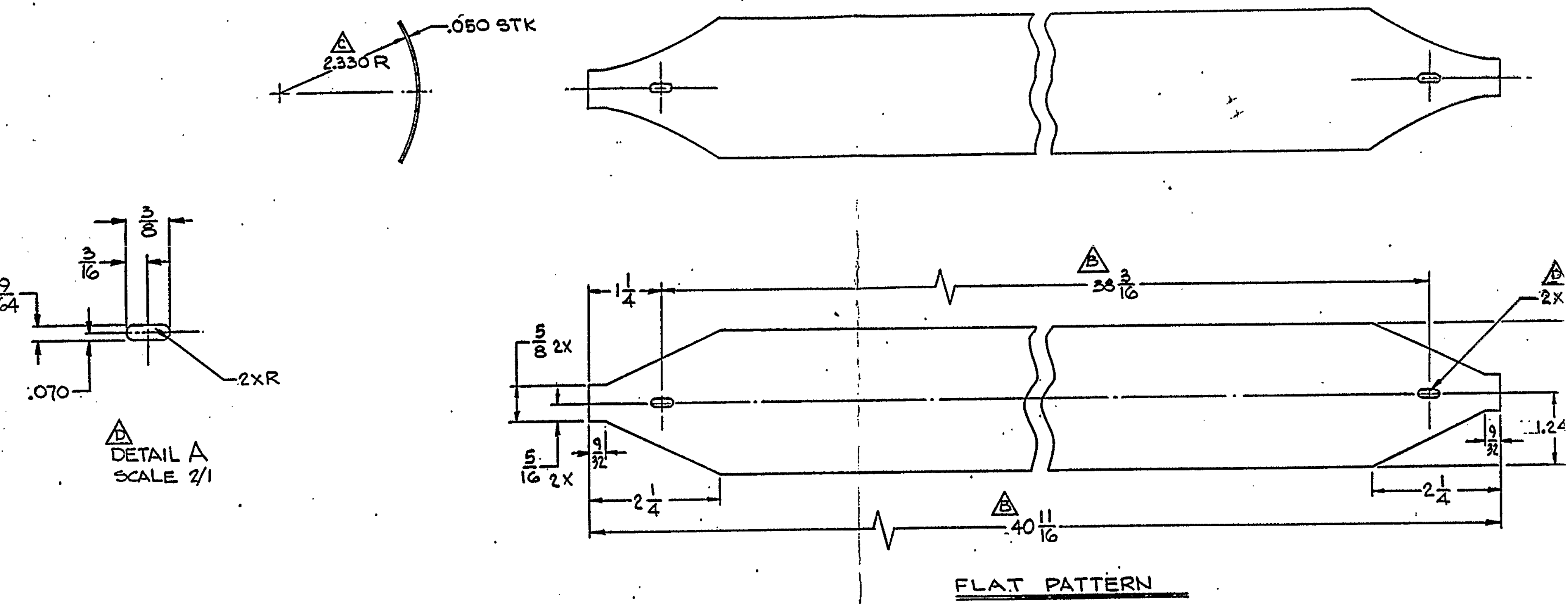
NOTES.
1. CENTER PUE, ITEM 2 AROUND THEORETICAL BEAM ℄, 'Ro'.
2. ETCH PART WITH DWG NO. "ASSY D11-M-11944-5" WITH 3/16 HIGH CHARACTERS.

AGS DAMPER PUE

QA CATEGORY A-3

NO. REQ	ACCT. NO.	I.L.R. NO.	ORDER NO.	DEPT.	D11-IM-155
3-16-90	SEE PL	1/1			BROOKHAVEN NAT... UPTON, ...
DATE	MATERIAL	SCALE		WEIGHT	AGS 10 FT STRAIGHT... PUE VACUUM...
N. Thomas	ZEBUDA				D11-M...
DRAWN BY	CHECKED BY	ENG APP	SUPVR APP		

FIG. 2



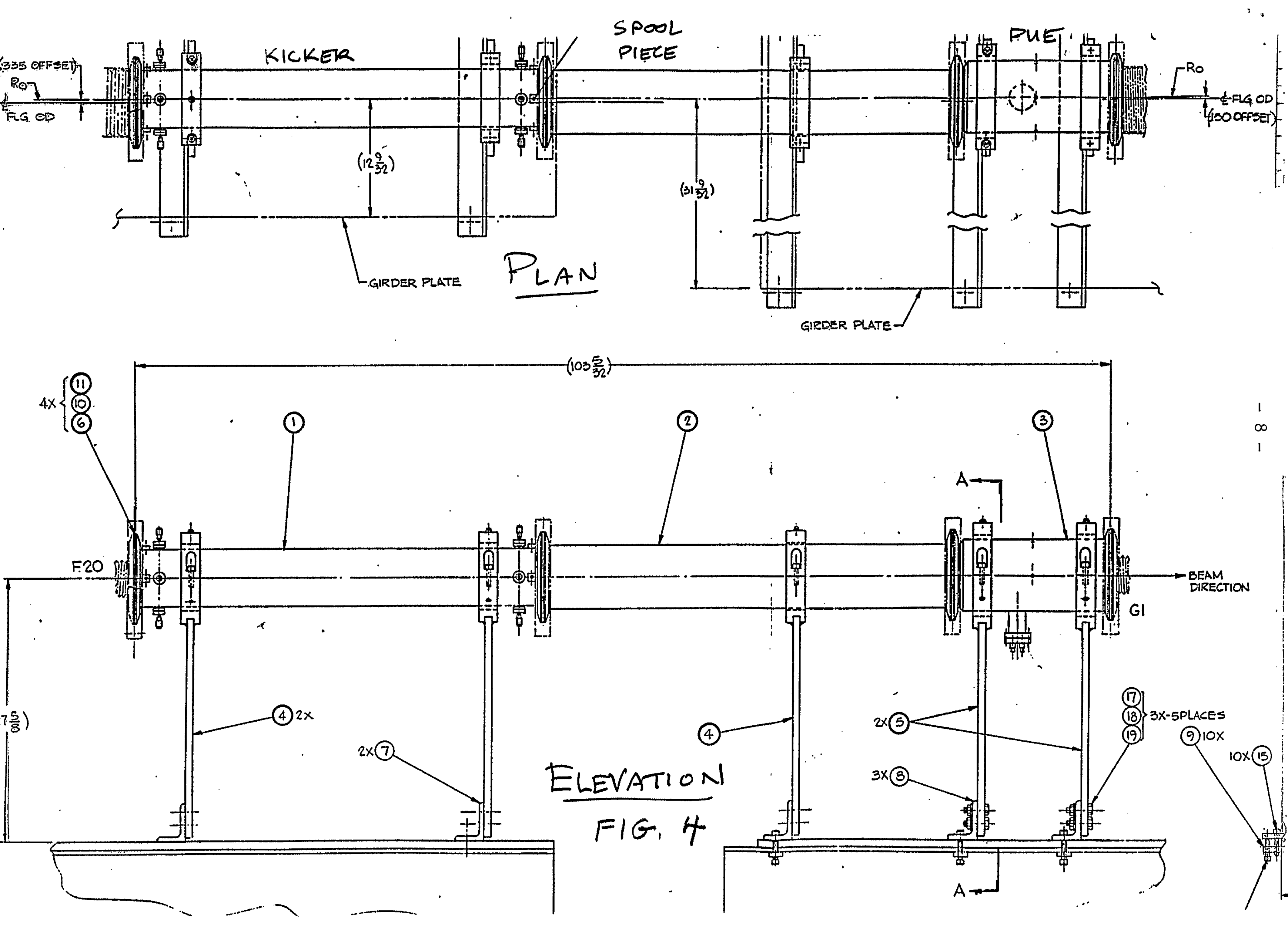
AGS DAMPER KICKER
ELECTRODE

FIG. 3

B D11-1M-155
D11-1M-155

NO. REQ	ACCT. NO.	I.L.R. NO.	ORDER NO.	DEPT.	JOB NUMBER
DEC. ± .010	ANG. ± 1/2°	MAX. .005 MIN. .002			BROOKHAVEN
TOLERANCE		BREAK SHARP EDGES			

AGS DAMPER F20 INSTALLATION



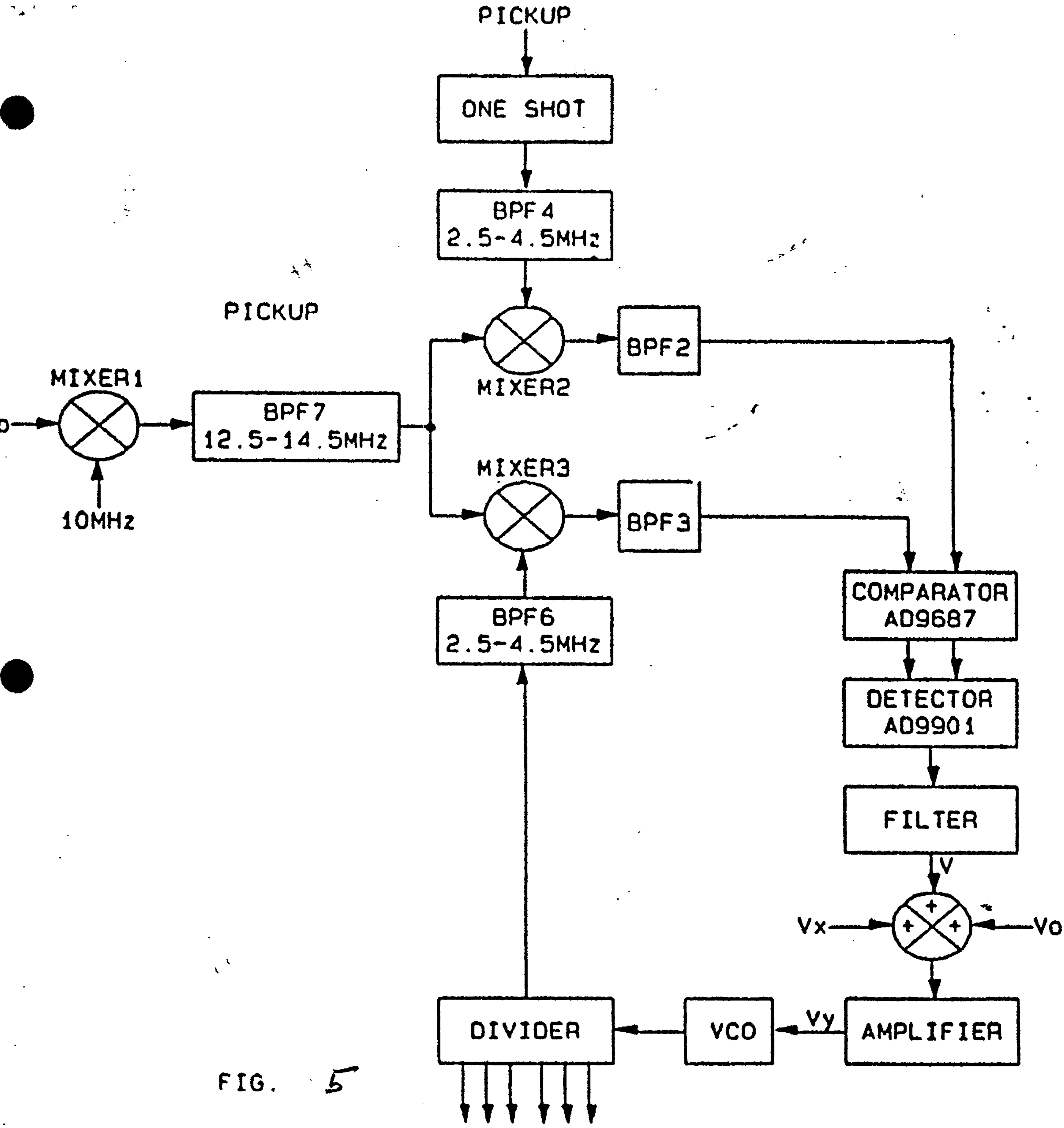

PICKUP
ONE SHOT
BPF4
2.5-4.5MHz
PICKUP
MIXER1
BPF7
12.5-14.5MHz
10MHz
MIXER2
BPF2
MIXER3
BPF3
BPF6
2.5-4.5MHz
COMPARATOR
AD9687
DETECTOR
AD9901
FILTER
V
Vx
Vo
AMPLIFIER
Vy
VCO
DIVIDER

FIG. 5

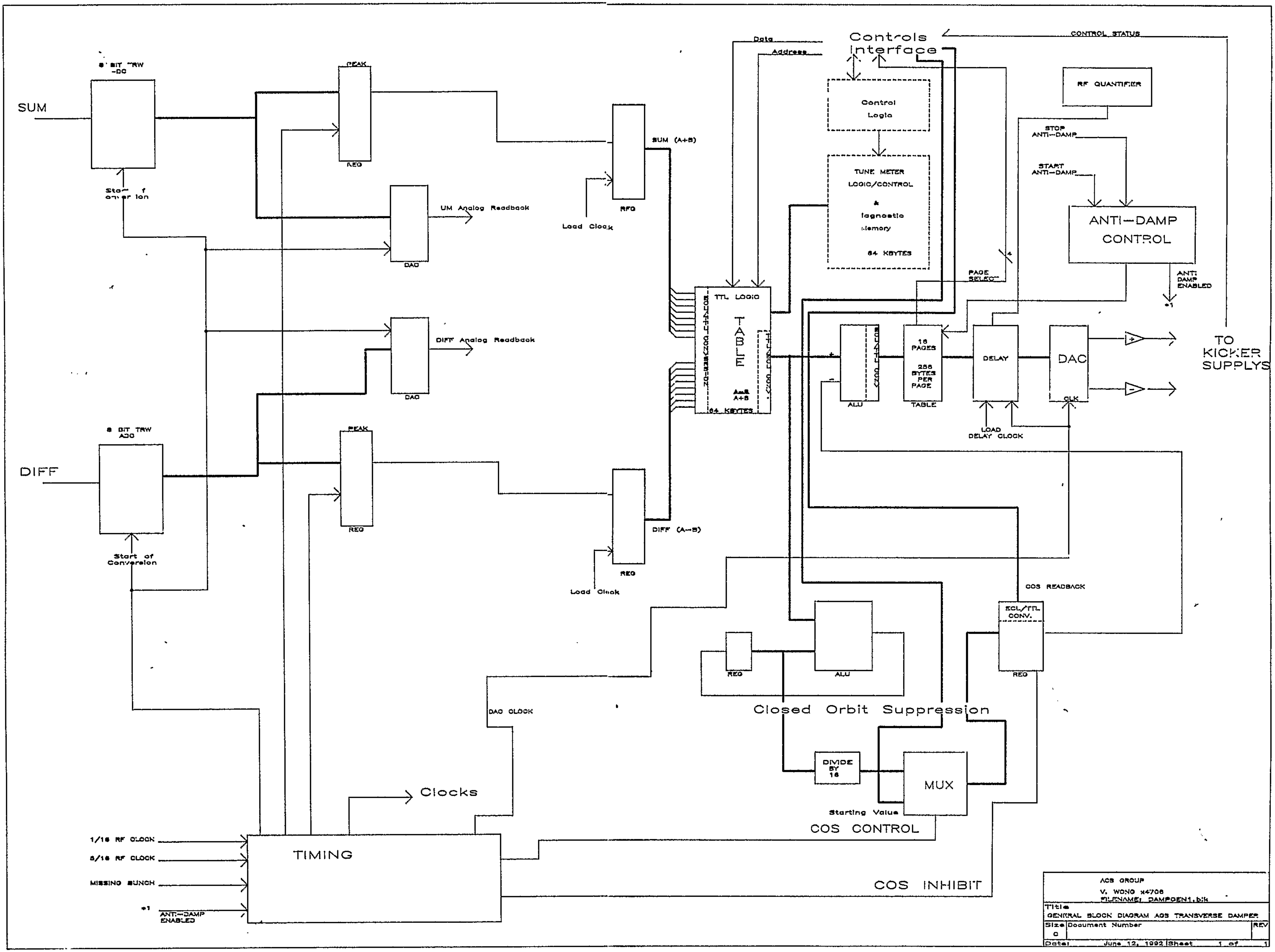

SUM
DIFF
8 BIT TRW ADC
Start of Conversion
PEAK
REG
DAC
DIFF Analog Readback
SUM (A+B)
DIFF (A−B)
Load Clock
TTL LOGIC
TABLE
64 KBYTES
A−B
A+B
Controls Interface
Data
Address
CONTROL STATUS
Control Logic
TUNE METER LOGIC/CONTROL
&
64 KBYTES
RF QUANTIFIER
STOP ANTI−DAMP
START ANTI−DAMP
ANTI−DAMP CONTROL
ANTI DAMP ENABLED
PAGE SELECT
ALU
16 PAGES
256 BYTES PER PAGE
TABLE
DELAY
DAC
CLK
LOAD DELAY CLOCK
TO KICKER SUPPLYS
COS READBACK
ECL/TTL CONV.
Closed Orbit Suppression
DAC CLOCK
DIVIDE BY 16
MUX
Starting Value
COS CONTROL
Clocks
TIMING
1/16 RF CLOCK
5/16 RF CLOCK
MISSING BUNCH
ANTI−DAMP ENABLED
COS INHIBIT
AGS GROUP
V. WONG x4706
FILENAME: DAMPGEN1.blk
Title
GENERAL BLOCK DIAGRAM AGS TRANSVERSE DAMPER
Size
C
Document Number
REV
Date: June 12, 1992
Sheet 1 of 1

FIG. 6