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BOOSTER DIPOLE and QUADRUPOLE VOLTAGE REGULATION LOOP

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I. Introduction

In this note, we present several design considerations for the Booster Dipole and Quadrupole power supply voltage regulation loop. We also define several tasks that are necessary to accomplish the design.

The Dipole and Quadrupole voltage regulation loops are expected to have the following functions.

i) The voltage reference(function generator) signal tracking. This will provide a scheme that permits the multiloop correction design. Also if a better tracking is achieved, the transfer function from the reference signal to the rectifier voltage output for the closed-loop system may be simplified. This may reduce the workload for the Dipole and Quadrupole control calculation.

ii) The power line disturbance rejection. With this function the voltage loop will play a major role among other disturbance rejection schemes such as the current feedback, the long term drift correction, etc.

iii) To reduce the effect of the rectifier system parameter variation. This will increase the system robustness.

In order to satisfy the requirements, the voltage loop should have a high DC loop gain as well as a wide bandwidth. On the other hand, high loop gain and wide bandwidth are not favorable if we are concerned with system stability and reliability. This is especially true for a multiphase rectifier system. For example, in the AGS Main Magnet Power Supply(Siemens) tests, we observed irrational response even though the

closed-loop system had a comfortable 45 degree phase margin. We believe that the voltage loop for the 24 phase rectifier with considerable commutations should have a DC loop gain that does not exceed 25-50, and a bandwidth that does not exceed 300Hz. In the design, we therefore choose moderate voltage loop gain and bandwidth to satisfy partially the fundamental requirements and ensure system reliability. We then apply other schemes, such as a couple of feedforward corrections, to improve the disturbance rejection and the reference tracking.

Since a multiphase rectifier is a nonlinear, slow rate nonuniform sampling system, the accurate models are sophisticated. Since the major parameters of the rectifier will vary considerably depending on the output level, and the system output voltage in our operation will not be fixed at a constant level, even accurate models that are available are not likely to be very useful. Therefore, we will use approximate models in the analysis. The error thus caused will not be substantial.

II. Voltage Loop

The voltage loop is shown in Fig.1, where $T1$ is the multiphase rectifier along with the triggering comparator circuits, $T2$ is the feedback circuit, and $T3$ is the regulator. We use y to denote the system output, $u1$ the voltage reference, $u2$ the possible correction input, and $u3$ the power line disturbance. In this case, $T1$ is a 24 phase controlled rectifier that will be discussed separately later. $T2$ is simply a voltage divider system, the divider coefficient can be determined according to the voltage output. For example, each power supply unit has a maximum $\pm$1100V output at the 100% tap, therefore $T2$ can be determined as 0.004, that gives rise $\pm$5V Max. at the reference comparator. We tentatively choose a simple regulator as

$$T3 = \frac{40k_3}{s + 40} \tag{1}$$

where k_3 is the DC gain of the regulator, that is adjustable.

The rectifier model $T1$ is the one that was derived from the AGS Siemens 24 phase rectifier tests[1]. The model had been applied to predict closely several other operations including an underdamped, an overdamped, and an unstable operation. The transfer function representing this model is written as

$$T1 = \frac{2.7E11k_1}{s^3 + 22500s^2 + 1.4E8s + 2.7E11} \tag{2}$$

where k_1 is the DC gain of the rectifier. A close look at this model shows that it is an approximation to a 0.5 ms time delay factor. In Fig.2, the Bode plots for both the model $T1$ and the time delay factor $e^{-0.0005s}$ are shown. Both the magnitude and phase curves are close in the frequency band from DC to 300 Hz, that is in the range of most importance for our system analysis.

If we let $k_1 = 30$, $k_3 = 50$, then such a voltage loop has a DC loop gain of 15. The two dominant complex conjugate poles of the closed-loop system are at $-1410 \pm 298i$, and represent a bandwidth of roughly 220 Hz. Note that we have the following different transfer functions for the different input terminals.

$$T_{yu1} = \frac{162E14}{s^4 + 22540s^3 + 1.409E8s^2 + 2.756E11s + 1.728E14} \tag{3}$$

$$T_{yu2} = \frac{8.1E12s + 3.24E14}{s^4 + 22540s^3 + 1.409E8s^2 + 2.756E11s + 1.728E14} \tag{4}$$

$$T_{yu3} = \frac{s^4 + 22540s^3 + 1.409E8s^2 + 2.756E11s + 1.08E13}{s^4 + 22540s^3 + 1.409E8s^2 + 2.756E11s + 1.728E14} \tag{5}$$

where T_{yu1} represents the transfer function from $u1$ to y, and so on for the other two. The dynamic responses for a unity step function at $u1$, $u2$, and $u3$ are plotted in Fig.3, where the gain for T_{yu2} is enlarged by a factor of 2.5, and that of T_{yu3}, by a factor of 75, to show clearly all three response curves in a single plot. The responses for different

transfer functions have different shapes. This property will be used in the corrections.

In the following sections(III to V), we present some design considerations, and define some tasks that must be accomplished.

III. Reference Controlled Gain Amplifier

The first problem that is encountered in the design is that the dynamic gain of the multiphase rectifier varies dramatically in its operation over its output voltage range. Since the rectifier voltage output has a certain relationship with the rectifier Phase Back Angle (PBA), we plot the curve of the rectifier dynamic gain against the PBA in Fig.4, where the voltage output level is also shown by the dotted line. Both curves are normalized to unity. In our Booster operation, the rectifier system is proposed to operate between 15 to 90 degrees of PBA during the Booster ramping part of the cycle. This implies that the dynamic gain of the rectifier will be varying between 0.3 to 1 (normalized). To apply voltage feedback for the whole cycle, we need an amplifier whose gain is complementary to the gain of the rectifier, and therefore the resulting overall gain of the amplifier and the rectifier remains constant during the operation. Note that the rectifier gain is related to the voltage output, and the voltage output is in turn determined by the voltage reference. Therefore, it is possible to build a Reference Controlled Gain Amplifier(RCGA) for our voltage loop using the reference program input. The amplifier may be implemented by an Analog Multiplier such as Burr-Brown AD-632, or a Voltage Controlled Amplifier such as Precision Monolithics SSM-2013. With these devices, if the voltage reference is used directly, then the curves are not well matched. The following circuit may provide a better match. An N-channel JFET 2N4338 from Siliconix can be used as a Reference Following Resistor that will be placed on an Operational Amplifier feedback path. The curve of the Drain-Source On Resistance versus the Gate-Source Cutoff Voltage is shown in Fig.5. The circuit is plotted in Fig.6, where the Source of the

JFET is placed at the amplifier negative input terminal, then the voltage drop on JFET Gate-Source is equal to the voltage applied to the Gate. An inverter is placed between the voltage reference signal and the JFET Gate. Consider the rectifier gain curve shown in Fig.4, and the JFET Drain-Source On Resistance curve in Fig.5, a proper choice of the inverter gain and offset that gives a rising voltage output from 4.5V to 0.5V in responding to the voltage reference from 0 to 5V results in a close gain curve match. To extend the use of this scheme to the invert part of the Booster cycle, an absolute value circuit should be added.

Once such an amplifier is designed and applied, the voltage loop will look like in Fig.7, where this amplifier is denoted as $T4$, and the DC gain from the combination of $T3$ and $T4$ will be constant. Later, we shall still use the circuit shown in Fig.1, and assume that this problem has been resolved and that the dynamic gain of $T1$ is constant.

IV. Feedforward Correction for the Power Line Disturbance

The voltage regulation loop design shown in Section II is made conservative because of system reliability considerations. To reject power line disturbances and to track the reference satisfactorily, we therefore cannot rely solely on the voltage regulation. The following correction scheme is proposed for further power line disturbance rejection. The scheme is a feedforward one, that will not introduce difficulties in the system operation and can be easily adjusted.

The worst case of the power line disturbance is a tap change that can be simulated as a step input at $u3$. The tap change step comes from the 20MVA 69/13.8KV transformer that is powering the Booster main ring system. Since the voltage loop has a limited bandwidth, the disturbance will immediately appear on the system voltage output, and then be gradually corrected after a certain time period. Thus, the voltage

output due to the step disturbance will look like the curve of T_{yu3} shown in Fig.3. It is called the transient error. This error will be stored in the magnet current. Since the voltage loop has a limited DC loop gain, there will also be a steady state error due to the step disturbance. This error will be integrated by the magnet, and appear to be a constant growth in the magnet current as time lapses. Thus, the magnet current error caused by the power line disturbance is from both the transient and the steady state voltage errors.

Since a power line disturbance can be detected, we may use this information for the correction. The correction signal will be placed at $u2$(Fig.1). It is clear from Fig.3 that both of the responses from steps $u3$ and $u2$ are impulse type, and that from step $u1$ is step type. Although the response curves of $u2$ and $u3$ do not exhibit the same exact shape, the correction at $u2$ for the disturbance $u3$ is probably the best choice. Another possible correction scheme of putting the correction signal at $u1$ needs additional dynamic circuits, thus resulting in a system that is not robust in the sense of matching the rectifier system dynamics.

The design procedure is simple. The correction signal is taken from a sensor that detects the power line disturbance. Considering that the DC gains from $u2$ and $u3$ to the output differs with a factor of k_1, we simply let the correction signal be reduced by this factor. The response curves of the step disturbance, the proposed correction, and the resulting virtual error are plotted in Fig.8. Note that the virtual curve takes the difference of the disturbance and the correction. By this design, we note that the transient error has been reduced, and the steady state error has been reduced even more, theoretically to zero. Since the current at the magnet is the integral of the voltage, the positive part and the negative part of the voltage error in the correction, that is shown in Fig.8, offset each other. Thus, the magnet current error has been reduced from what it would have been without the correction. This is shown in Fig.9.

If we design a phase-lead network to differentiate the disturbance signal, and therefore to match more closely the response curves of $u2$ and $u3$, the error may be further reduced. We do not advocate this type of schemes because of the following reason. The signal from the disturbance sensor may be corrupted by high frequency noise, therefore the phase-lead network is not suitable at this point. A carefully designed filter that is used to clean the noise may result in a better correction. The using of a filter to the phase-lead network is in fact a lead-lag network. The adjustment and the operational setup problems might be considered as not favorable to this choice.

For this correction to succeed, a good sensor of the power line disturbances is indispensable. The requirements for the sensor include the speed, the accuracy, the resistance to the power line noise, and a low long term drift. Several schemes are under consideration, and this certainly will require a dedicated effort.

V. Feedforward Correction for the Reference Tracking

The transfer function T_{yu1} is expected to be as close as possible to the reciprocal of the feedback coefficient. In our case, this is 250. With such a design, the transfer function from $u1$ to y can be viewed as an ideal amplifier, which provides a convenient system scheme for the other correction schemes such as current feedback and a computer controlled long term drift correction. Again, these require high loop gain and wide bandwidth. In this section, we propose another feedforward correction scheme that will contribute to an improvement of the response of T_{yu1}.

As far as we are concerned, the transient response is more important than the steady-state response for our application. We therefore take the rise time and the overshoot in the system step response as the criterion for the improvement of the performance of the transfer function. Consider the plot in Fig.3. There we can see that the step responses of T_{yu1} and of T_{yu2} may be considered supplementary for an ideal step

response. We therefore propose the following scheme shown in Fig.10, where $T5$ is a feedforward compensator that may be a constant amplifier, or a phase-lead network. We consider first the constant amplifier.

Let

$$T5 = k \tag{6}$$

Then the modified transfer function T_{yu1} can be written as

$$\overline{T}_{yu1} = T_{yu1} + kT_{yu2} \tag{7}$$

that is in turn calculated as

$$\overline{T}_{yu1} = \frac{k8.1E12s + k3.24E14 + 162E14}{s^4 + 22540s^3 + 1.409E8s^2 + 2.756E11s + 1.728E14} \tag{8}$$

The poles are found to be at -13600, -6118, $-1410 \pm 298i$, respectively, where the last two complex conjugate poles determine the slowest modes. If we choose $k = 1.5$, then the zero will be moved to -1373, and therefore one of the slow modes will be canceled. This improves the transfer function T_{yu1}. In Fig.11, we plot the step response under different k for this correction. From the bottom to the top, the curves are for $k = 0$, 0.5, 1, 1.5 ,2, respectively. It seems that k =1.5 is a good choice.

A phase-lead network with a limited leading phase is considered suitable in this application, because both the voltage reference signal and magnet current feedback signal are clean. Although by the use of a phase-lead network the two complex conjugate poles might be canceled, a study shows that with first order compensators, that are preferable in practice, that this is not the case completely. In Fig.12 we show the root-locus plot for the possible zero assignment by the phase-lead networks that must have a large pole and a not large DC gain. The plot shows that such a pair of zeros close to the system slowest modes, (i.e., $-1410 \pm 298i$), do not exist. Therefore, the correction result is not much more superior over the constant amplifier correction.

In another design, where the loop gain is increased from 15 to 24, the slowest system complex conjugate poles have been moved to $-1200 \pm 1255i$, respectively. Such a pair of zeros become available, and the better corrected step response is shown in Fig.13.

Reference

[1] S. Zhang, A. Soukas, J. Sandberg, A. Feltman, and J. Gabusi, 'B-dot Servo System Measurement and Modeling,' AGS Studies Report, No. 241, July, 1988.

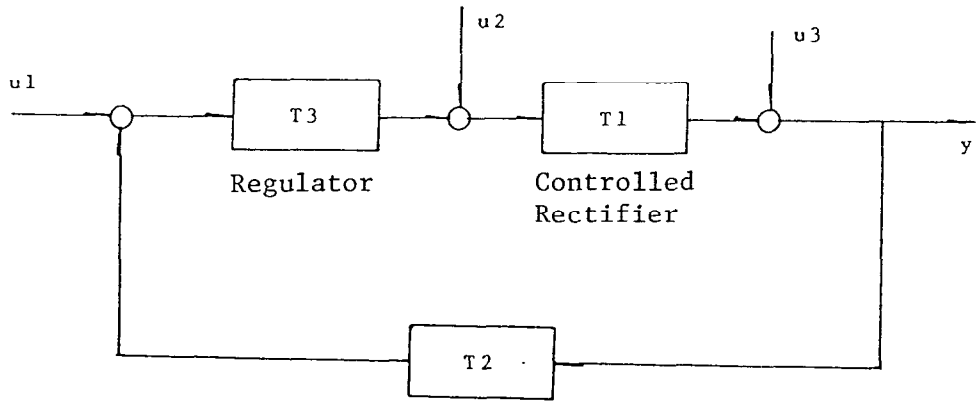

Fig.1

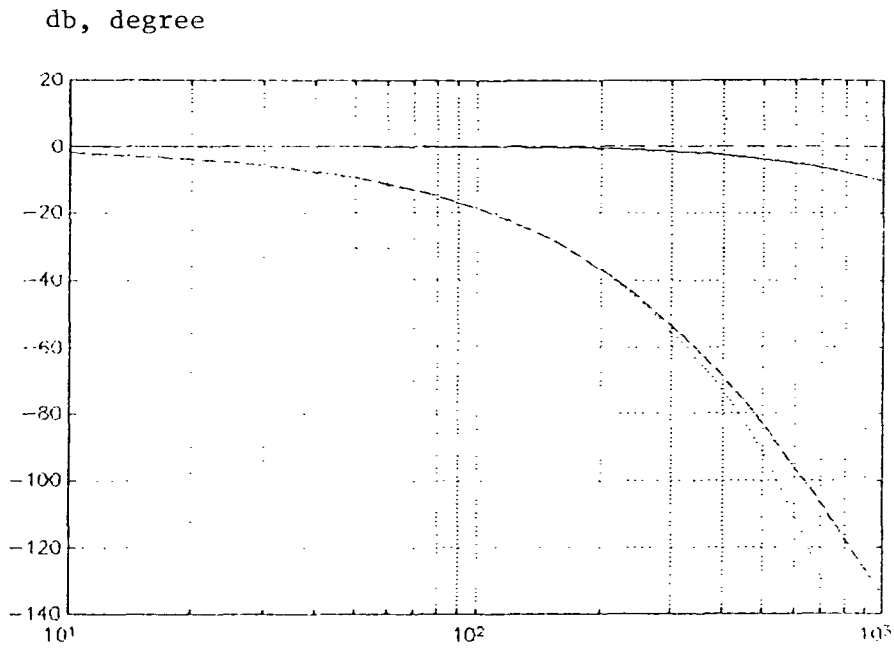

Fig.2

—·—·—·— : Delay factor Mag.

····· : Delay factor Phase

——— : T_1 Mag.

– – – – : T_1 Phase

Delay Factor: $e^{-0.0005s}$.

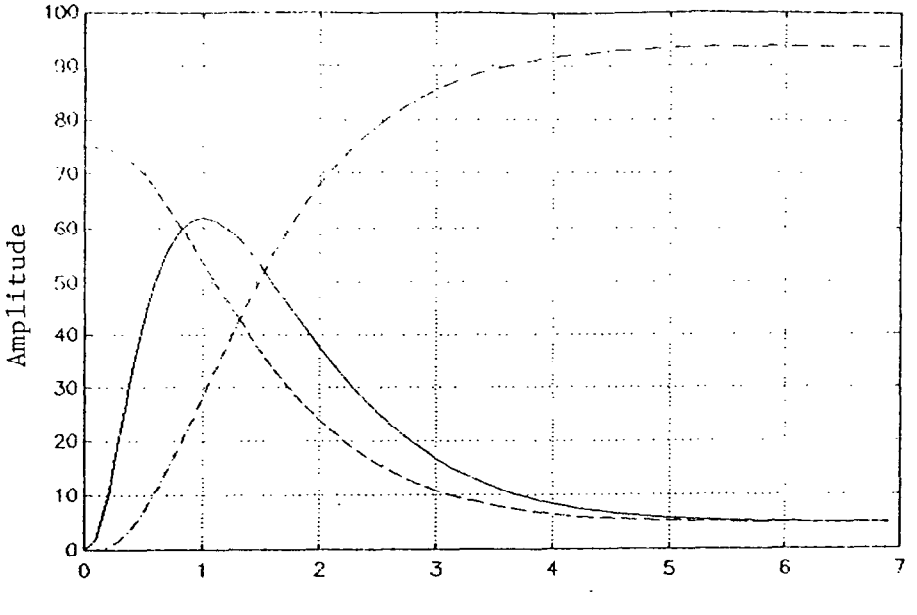

Fig.3

—·—·—·— : T_{yu1}

——— : T_{yu2} (x2.5)

– – – – : T_{yu3} (x75)

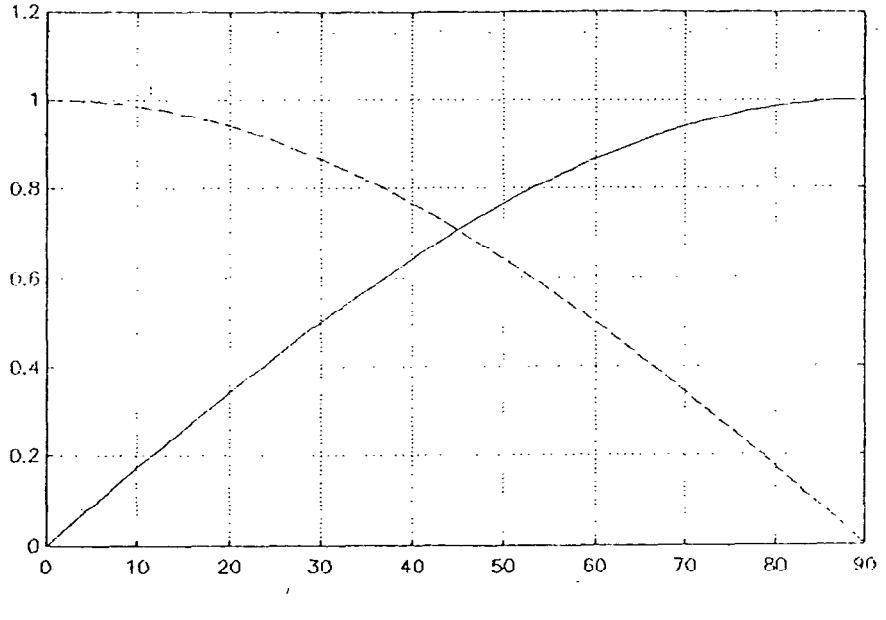

Fig.4

– – – – : Voltage output level

——— : Dynamic gain

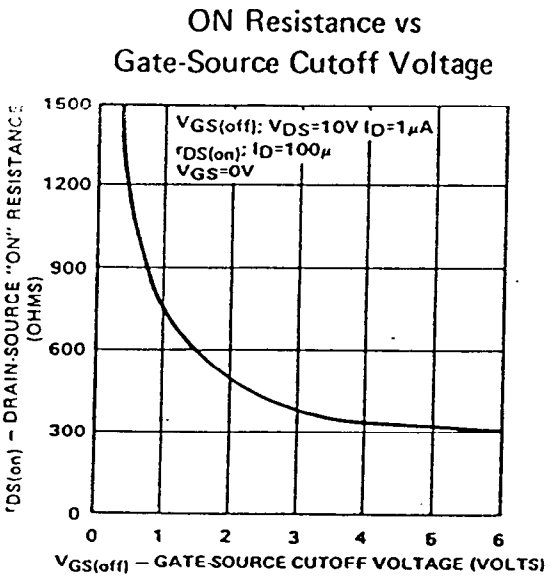
ON Resistance vs
Gate-Source Cutoff Voltage
$V_{GS(off)}$: V_{DS}=10V I_D=1μA
$r_{DS(on)}$: I_D=100μ
V_{GS}=0V
$r_{DS(on)}$ – DRAIN-SOURCE "ON" RESISTANCE (OHMS)
1500
1200
900
600
300
0
0 1 2 3 4 5 6
$V_{GS(off)}$ – GATE-SOURCE CUTOFF VOLTAGE (VOLTS)

Fig.5

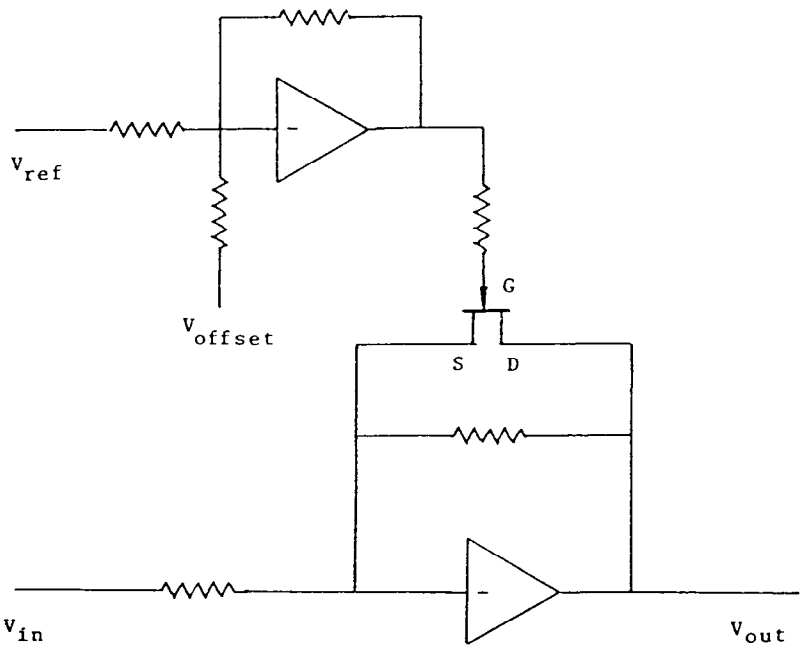
V_{ref}
V_{offset}
G
S
D
V_{in}
V_{out}

Fig.6

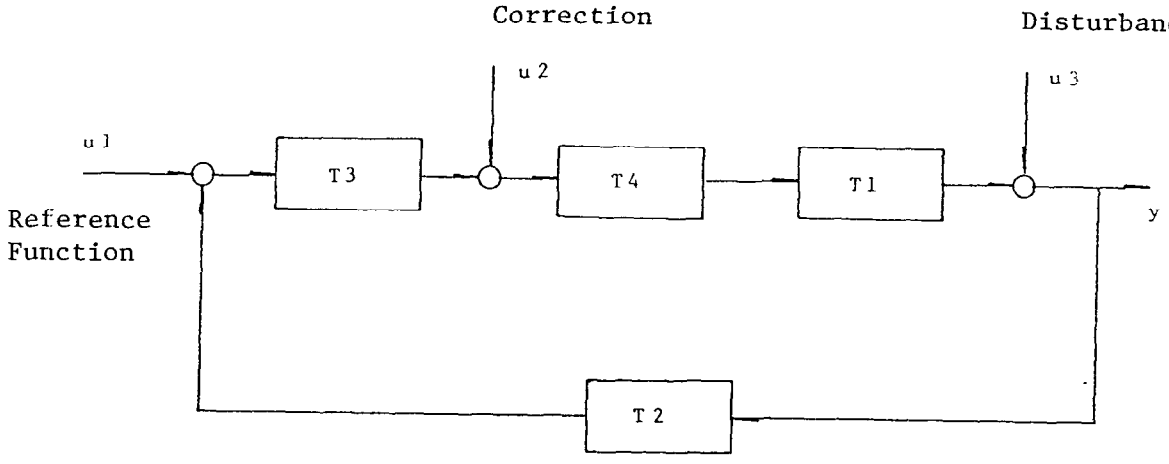

Fig.7

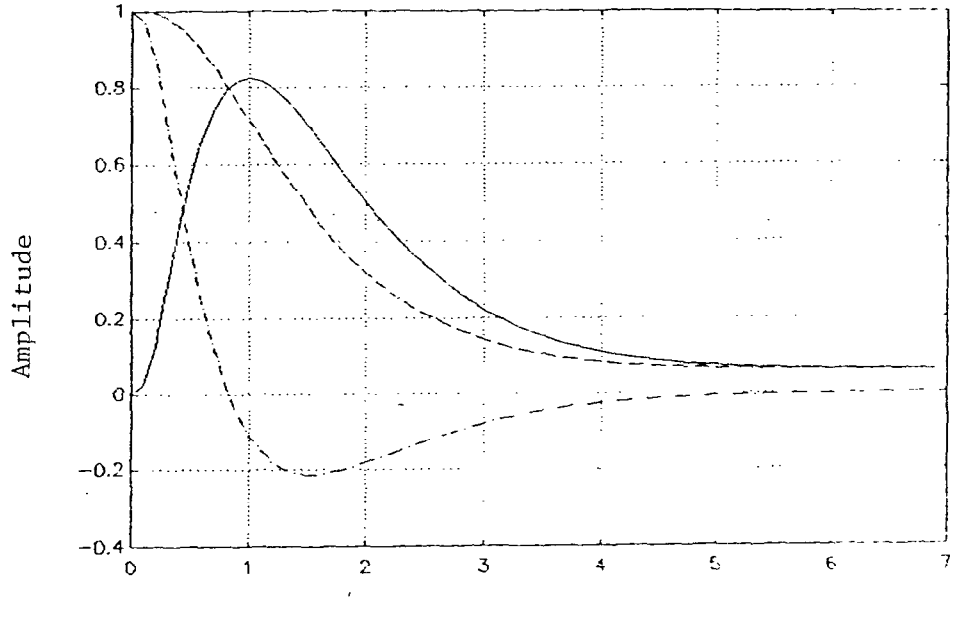

Fig.8

– – – – : The output due to step power line disturbance

——— : The output due to the correction

—·—·—· : The resulting virtual output

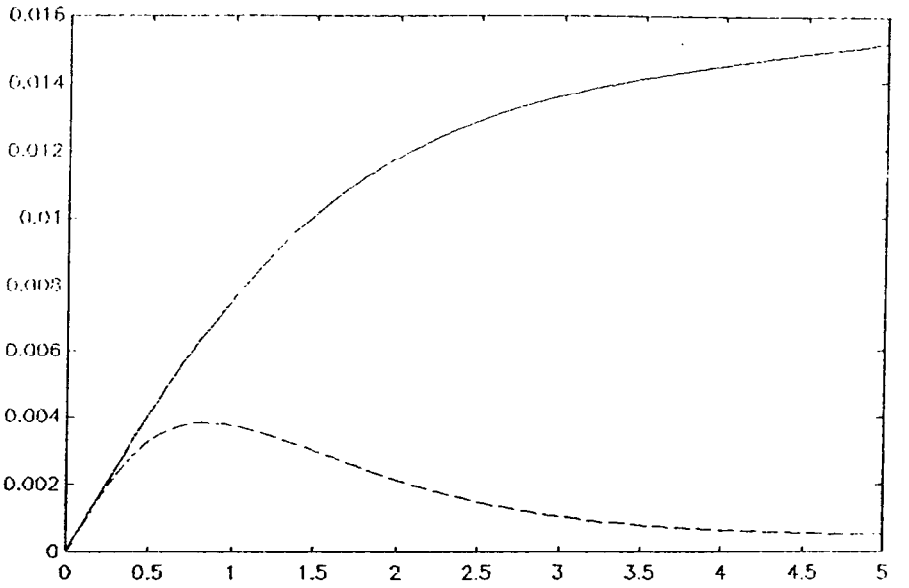

Fig.9

——— : Magnet current error without correction

– – – – : Magnet current error with correction

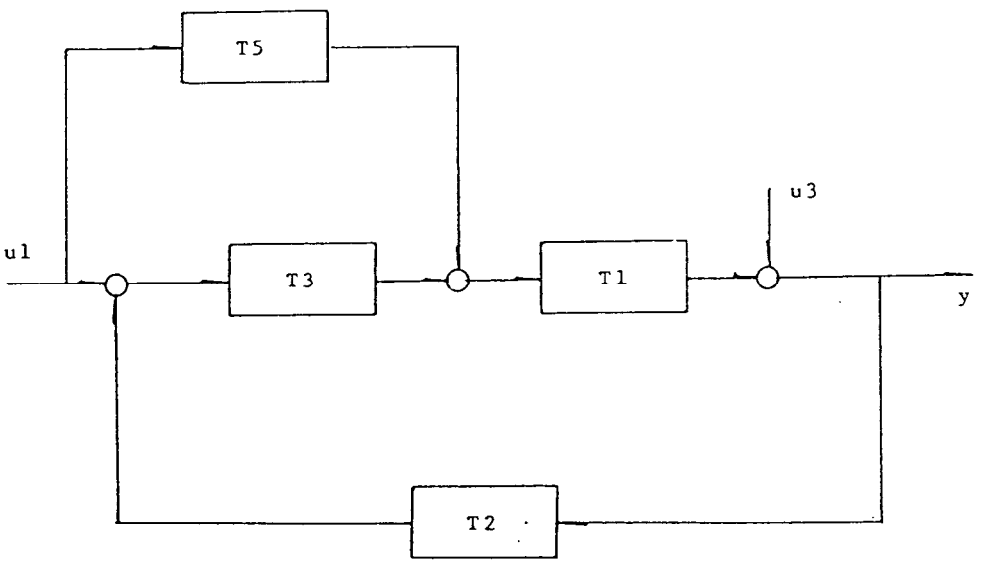

Fig.10

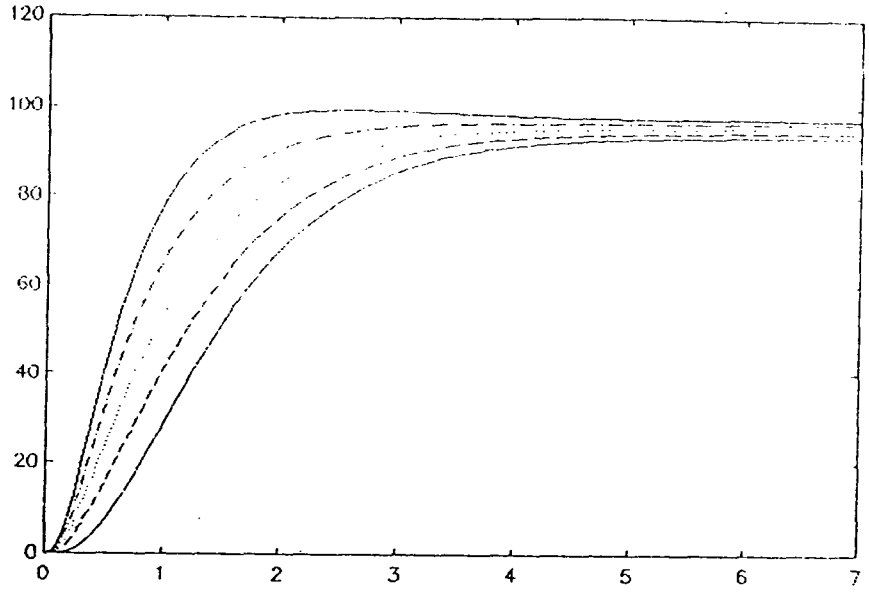

Fig.11

From top to bottom:
k = 2, 1.5, 1, 0.5, 0

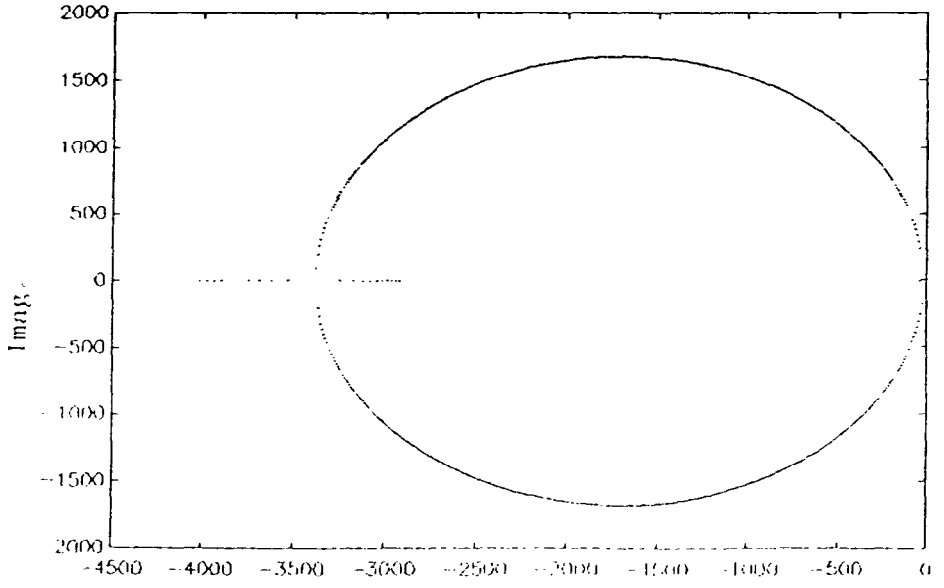

Fig.12

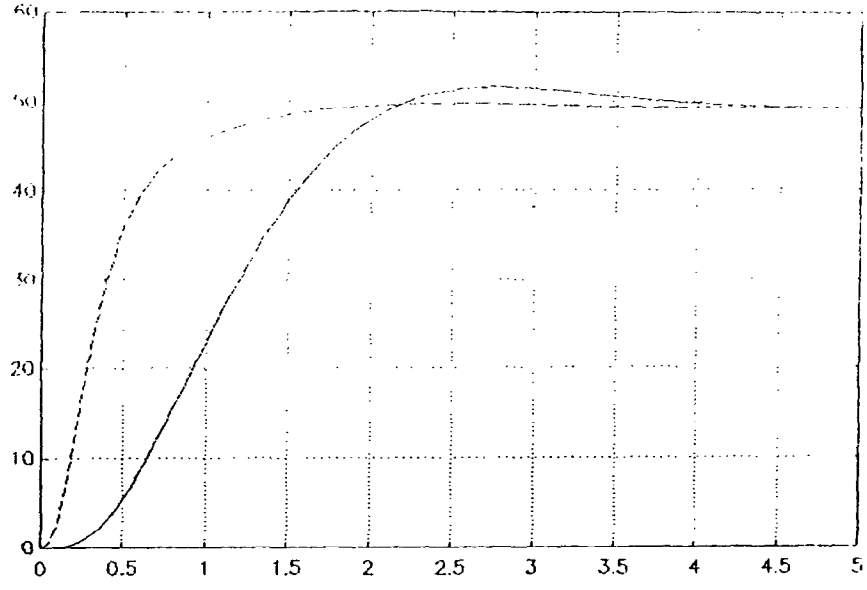
60
50
40
30
20
10
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
Time, ms
: Uncorrected
: Corrected

Fig.13