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USING THE BPM BUILT-IN TEST CAPABILITIES TO VERIFY SYSTEM OPERATIONAL STATUS

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BOOSTER TECHNICAL NOTE
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TABLE OF CONTENTS

INTRODUCTION:

This technical note is meant as a guide for using the remote built-in test capabilities of the Booster BPM system. The local electronics installed in the ring are accessed via the *ss_mouse* program. The spreadsheet program gives the user the ability to activate the BPM calibration signals, as well as to change the front end and fiberoptic transmitter pre-amp gains. Control of these parameters enables the user to verify that the proper analog PUE signals are arriving at MCR_4. In addition, the calibration signals may be used to verify the alignment of the entire analog PUE link[1].

Some of the built-in test capabilities of the BPM system may be accessed more conveniently via the *booster_orbit* program. Although slightly less flexible than Spreadsheet, booster_orbit is extremely useful as a troubleshooting tool due to its ease of use and display capabilities. The program has a diagnostic section which activates the Calibration mode of the BPM electronics, then acquires and displays the resulting SUM and DIFF integrals returned by the local processing hardware (located in the ring). Properly interpreted, the display provided by the software can be used as powerful troubleshooting aide to

. Confirm that A/C power is being delivered to each BPM station
. Report the status of major system interconnections
. Verify communication between the host and each BPM station
. Help identify gross failures of individual modules.

This paper is divided into three basic sections; The first section discusses the specific built-in test capabilities designed into the local processing electronics, as well as how to access them. The second section presents a method of using the calibration capability of the system to verify alignment of the PUE analog links. Section three deals with the use of the *booster_orbit* program to remotely verify the status of the ring electronics. In Section 3, the user is stepped through a sequence of calibration tests. For each test, some of the possible failure modes are listed as a starting point for troubleshooting the system.

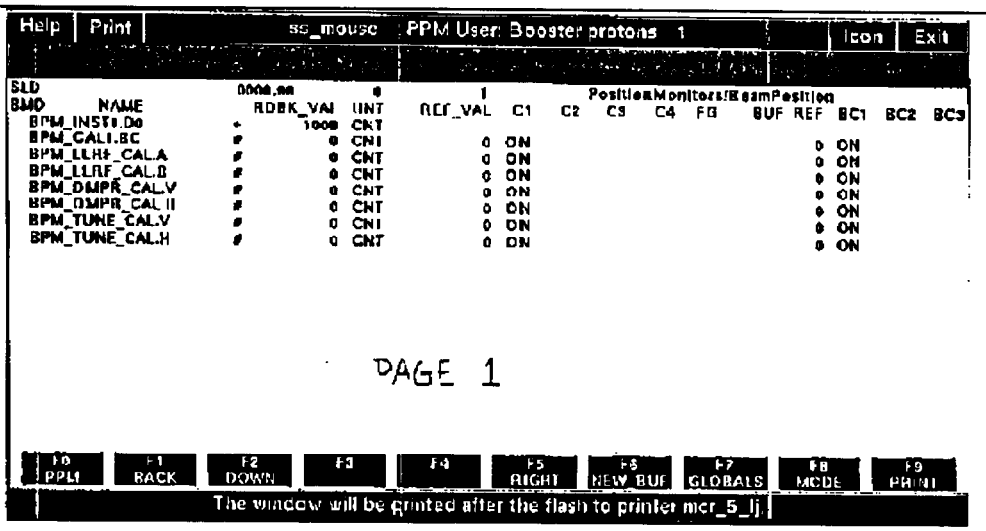
SECTION I

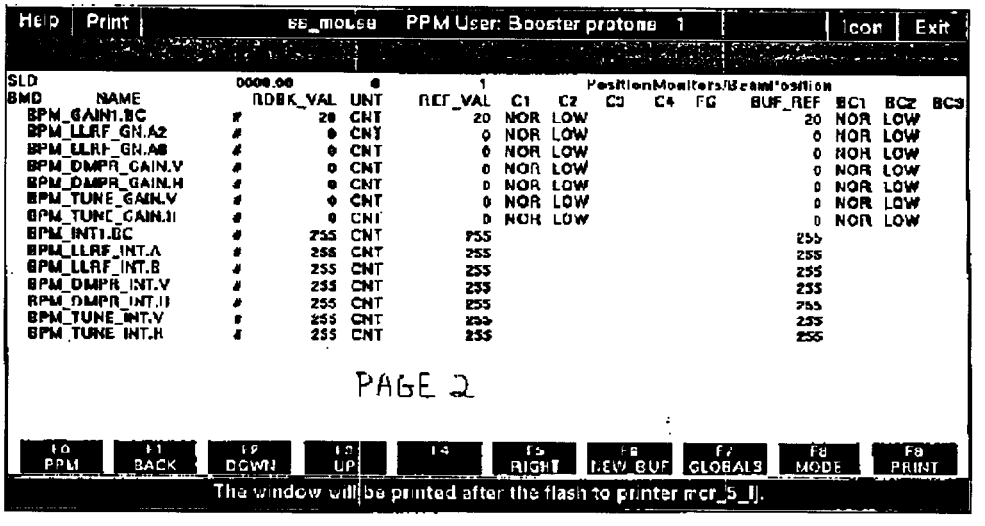
BUILT-IN TEST CAPABILITIES OF THE BOOSTER BPM SYSTEM HARDWARE

Accessing The Hardware Through ss_mouse

When using ss_mouse, the path (starting from the HOME menu) to the BPM system controller is as follows:

Controllers
Booster
Instrumentation
Position Monitors
Beam Position





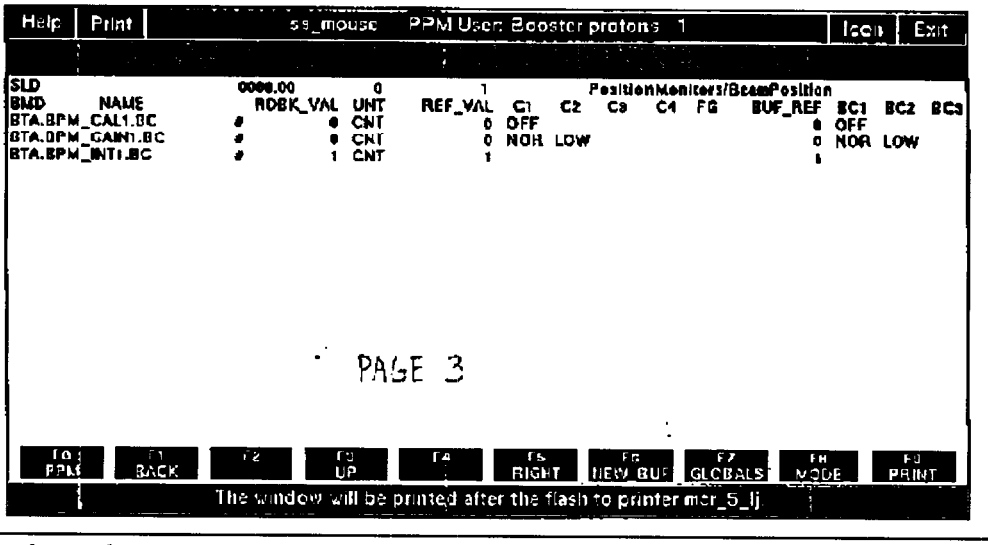


Figure 1. The Three Menu Pages for the Booster BPM Controller.

There are three menu pages associated with the Booster BPM Controller (Figure 1). The first page is used for turning the Calibration mode ON or OFF, with separate control for those BPM stations shared by the LLRF Radial Control Loop (A2 and A8) and Tune Meter (E7 and E8). Those BPM stations in the ring not separately itemized on the first page use the SLD name BPM_CAL1.BC (where .BC indicates that the SLD is of the "broadcast" variety). Column C1 turns the calibration mode ON and OFF, and the value (0-4) appearing in the REF_VAL field determines the pulse repetition frequency of the calibration signal (refer to the "Calibration and Local Timing (CLT) Module" section for REF_VAL assignments).

The page 2 menu is where the front end gains are set, as well as the number of bunches over which to integrate. Once again, the LLRF radial control loop, Damper and Tune Meter BPM stations are itemized separately. The remaining locations in the ring are controlled by the SLDs BPM_GAIN.BC (front end gain) and BPM_INT1.BC (the number of bunches, or rf cycles, over which to integrate). To set the front end gain, an appropriate value corresponding to the desired gain mode is entered into the REF_VAL column (refer to section below entitled *Changing Front End Gain Via Spreadsheet*). Column C1 controls the gain of the integrators (NOR for an integration capacitance of 1033pF or ST for an integration capacitance of 33pF, used when taking single turn orbits)[2]. The ST gain setting was incorporated to boost the relatively low output voltage of the integrators resulting for orbits measured over a low number of bunches (e.g., single turn). The value appearing in the C2 field is used to set the gain of the fiberoptic pre-amplifiers at those stations so equipped. The fiberoptic gains available are /10, x1, x5 and x50, and are independent of the front end gain.

BPM_INT1.BC (or any of the other itemized "_INT." SLDs) may take on a REF_VAL of from 1 to 255. Note that the user should be aware of the currently operating "harmonic number" of the machine when choosing a value for this item; The BPM hardware measures integration time in terms of the number of bunches passing by each individual detector; it does <u>not</u> measure integration time with respect to the number of turns of an arbitrary reference bunch. For example, for a given REF_VAL of 96, the orbit measurement would be averaged over 32 turns if the Booster is running at harmonic 3, but would be averaged over only 4 turns if there were 24 bunches in the machine.

<u>The Detector</u>

The BPM detector in the Booster has a calibration ring concentric to the split cylinder Pick Up Electrodes. Since the ring is centered along the length of the detector, a voltage applied to it will equally couple to each of the two PUEs. The resulting bunch signals simulate a transversely centered beam, providing equal test signals to the inputs of the Front End Processing (FEP) module. As a test port, the calibration ring is useful for determining whether or not the PUE cables are connected, but it cannot be used to determine if the cables are reversed (since the voltage resulting on either PUE is the same).

Calibration and Local Timing (CLT) module

This module controls the acquisition timing at each individual BPM station. When used in calibration mode, the CLT module provides the test signal to the calibration ring. The module outputs a burst of 12.5 V_{pk} pulses (the number of which is determined by the value of BPM_INT1.BC in spreadsheet) at one of 5 possible pulse repetition frequencies: 4MHz, 2MHz, 1MHz, 500kHz or 250kHz. All five of these frequencies can be accessed via spreadsheet; However, the diagnostic section of the booster_orbit program will only allow the user to specify two of the five; 1MHz or 4MHz.

Both the amplitude ($12.5V_{pk}$) and the effective bunching factor (25%) of the test pulses are fixed; Thus the integral of the bunch signal will vary linearly with prf. (This differs from an actual bunch signal due to beam, where the amount of charge per bunch remains constant, irrespective of frequency). The test pulses simulate bunches containing an amount of charge as follows:

PRF	ss value	B.F.	Sim. Q_b	Sim.Intensity
4.0 MHz	0	0.25	11.6 nC	2.2 x 10^{11}ppp
2.0 MHz	1	0.25	23.3 nC	4.4 x 10^{11}ppp
1.0 MHz	2	0.25	46.6 nC	8.7 x 10^{11}ppp
500 kHz	3	0.25	93.1 nC	1.7 x 10^{12}ppp
250 kHz	4	0.25	186. nC	3.5 x 10^{12}ppp

In the calibration mode, the BLR pulses for the acquisition electronics are generated locally (i.e., within the CLT module), to guarantee that they are phased correctly with the test signal.

Front End Processing (FEP) module

The FEP circuitry has the capability of gating-off either of its two analog input signals. Removing the calibration signal from one FEP channel causes the electronics to perceive that the beam is all the way over to one side of the beampipe. This type of simulation can be used to verify the general operating status of the Acquisition modules in the ring, since both the DIFF and the SUM integrals change when one input signal is removed from the FEP. Removing an input signal from the FEP module is accomplished by setting the gain of that channel to 0.

Changing Front End Gain Via Spreadsheet:

The different gain modes of the PUE front end can be controlled using a five bit data word in spreadsheet. Although only 3 gain states are used for purposes of position measurement (i.e., /10, x1 and x10), the data word can be used to individually set the gain of each FEP channel in order to remotely test the hardware.

In the following table, each of the five bits (B0 - B4) represents the gain applied to the PUE signal from electrode A, electrode B, or both (the function of each gain bit is listed at the top of its respective

column). B4 and B2 are turned "on" (1) simultaneously to effect a gain of x1. If a gain of x10 is desired, B0 must also be turned "on" (in addition to B4 and B2). A gain of x0.1 is effected by turning "on" only bits B3 and B1.

In addition to its particular hardware function, each bit has a weight associated with it. Column 7 lists the decimal sum of the bit pattern for each of the listed front end gain settings; These are the actual values used to set the gain in Spreadsheet.

CHANGING BOOSTER PUE GAINS VIA SPREADSHEET

	A:x1 A:x10	A:/10	B:x1 B:x10	B:/10	A:x10 B:x10	
	2^4=16	2^3=8	2^2=4	2^1=2	2^0=1	
GAIN	B4	B3	B2	B1	B0	SS ENTRY
x.1	0	**1**	0	**1**	0	**10**
x 1	**1**	0	**1**	0	0	**20**
x 10	**1**	0	**1**	0	**1**	**21**
A=x1 B=OFF	**1**	0	0	0	0	**16**
A=OFF B=x1	0	0	**1**	0	0	**4**
A=x10 B=OFF	**1**	0	0	0	**1**	**17**
A=OFF B=x10	0	0	**1**	0	**1**	**5**
A=/10 B=OFF	0	**1**	0	0	0	**8**
A=OFF B=/10	0	0	0	**1**	0	**2**

Special Notes:

1. The lowest FEP gain setting (/10) offers a somewhat extended lower end frequency response; this may prove more asthetically pleasing on the oscilloscope for longer pulses (assuming sufficient signal level to use the /10 mode).

2. When utilizing the booster_orbit program, the front end gain should be changed whenever the SUMs output is near the +10 Volt saturation point of the ADCs.

SECTION 2

VERIFYING ANALOG PUE LINK ALIGNMENT

Users of any of the analog PUE links should refer to Booster Technical Note #214, *Understanding The Analog PUE Signals* [1], for a description of the basic link components (in block diagram form). The note also describes an alignment procedure for adjusting the gain of the two fiberoptic channels in each link. The following "check-out" procedure assumes that the link has already been aligned, and should be used to provide baseline data immediately prior to using the link for data gathering purposes.

STEP 1 In Spreadsheet, turn ON the calibration mode of the BPM electronics (refer to Section 1).

The SLD name for the broadcast command to do this is **BPM_CAL1.BC**, found in the menu on page 1. Certain special locations such as A2 and A8 (LLRF radial loop locations) are not affected by the broadcast command; The calibration mode at these locations must be controlled individually. The relevant SLD names are also found on page 1.

STEP 2 In Spreadsheet, set the gain of the Front End Processing (FEP) module and the gain of the fiberoptic pre-amp.

The SLD name for the broadcast FEP gain command is **BPM_GAIN1.BC**, found in the menu on page 2. Certain special locations such as A2 and A8 (LLRF radial control loop locations) are not affected by the broadcast command; The gains at these locations must be controlled individually (the relevant SLD names are found on page 2). The decimal value to be entered in the REF_VAL column is determined from the table in section 1 entitled *Changing Booster PUE Gains Via Spreadsheet*. The value displayed in column C2 is used to set the fiberoptic pre-amplifier gain.

The total product of the FEP and fiberoptic pre-amp gains should be selected to keep the transmitter operating in its linear region (i.e., < 500mV$_{pp}$ at the input to the f/o transmitter). The calibration signal applies a voltage of approximately 200mV$_{pp}$ onto the PUEs. The voltages appearing at the input to the Meret f/o transmitter are estimated using the functional block diagram of the front end electronics in Figure 1, reference [2]. When verifying operation of the link, the FEP and f/o pre-amp gains should be set according to the following table, to ensure that the test signals remain within the linear operational range of the transmitter:

Fiberoptic Pre-amp Gain Settings For Linear Operation

FEP AUX OUTPUTS	FEP GAIN	FIBEROPTIC PRE-AMP GAIN	INPUT TO F/O TRANSMITTER
A/B	x0.1	x50	500mV
"	x1	x5	500mV
"	x1	x1	100mV
"	x10	x0.1	100mV
SUM/DIFF	x1	x1	SUM: 50mV
"	x1	x5	SUM: 250mV
"	x1	x10	SUM: 500mV
"	x10	x0.1	SUM: 50mV
"	x10	x1	SUM: 500mV

Note that the right-most column in the above table refers to the peak voltage at the input to the fiberoptic transmitter; The user should expect the actual voltage appearing at MCR_4 to be lower than the listed values, due to cable transfer losses between building 914E and the Main Control Room.

STEP 3 When using FEP modules with AUX A/B outputs, the user simply verifies that the two waveforms (plate A and plate B) have the same amplitude when viewed at MCR_4. Care should be taken to select an appropriate combination of FEP and f/o preamp gains from the above table when comparing waveforms.

When using FEP modules with AUX SUM/DIFF outputs, verifying that the gain of both analog f/o channels are equal is a bit more involved. The peak amplitude ratio of the DIFF signal to the SUM signal is checked for two different amplitudes of the calibration signal. If the ratio between the two remains constant, then the link gains are known to be equal.

STEP 3A Set the FEP gain to a value of 16 (A=x1, B=0). This will cause a large DIFF signal, approximately 1.9 times the peak amplitude of the resulting SUM signal.

STEP 3B Set the f/o preamp gain to x1. Note the ratio of the peak DIFF signal to SUM signal.

STEP 3C Set the FEP gain to a value of 17 (A=10, B=0). If the ratio of the DIFF signal to the SUM signal is the same as in STEP 3B, then the f/o channels are matched.

SECTION 3

USING *booster_orbit* TO VERIFY THE STATUS OF THE RING ELECTRONICS

The Booster BPM system has several built-in-test features which enable the operator to perform a "confidence check" on the system hardware. The diagnostic section of *booster_orbit* is used to exercise some of these features and graphically display the resulting SUM and DIFF integrals from each BPM station. Note that when the system is used in the Calibration mode, the baseline restorer pulses are generated locally (the blr pulses for each BPM station are generated at that particular station). As such, Sequencer operation connot be verified when the system is in Calibration mode.

A quick BPM system confidence check can be made by carrying out the following 3-step procedure. (The user may wish to get a hardcopy of the resulting plots from each step for troubleshooting purposes).

In this group of tests, the number of bunches over which to integrate is set to 80. This value is chosen to keep the output of the integrators from saturating. The measurement time chosen is t=20 msec after t_0, but is not critical. Note that this procedure will interfere with the operation of both the LLRF radial control loop and the tune meter; For this reason, the procedure should only be carried out at a time when no beam is present in the Booster.

STEP (1): **A=10, B=10, N_BUNCH=80, cal signal, 1 MHz, t=20 msec.**

The resulting SUM and 2xDIFF plots for this test are used to verify:

1. Communication between the ring hardware and the high level software is good;
2. Both PUE cables are connected to the BPM electronics;
3. The Calibration Ring is receiving signals from the electronics;
4. The Front End Processing (FEP) module is operating;
5. The SYSTEM SUM output of the Front End Processing (FEP) module is getting to the input of SUM Acquisition module;
6. The SUM channel acquisition functions (blr, local timing, integrator and A/D conversion) are operating properly.

The SUM display should be positive and close to 9 Volts; the 2xDIFF display should remain at offset levels (near 0 Volts). If this is true for all of the Horizontal and Vertical locations, then go to step 2.

SUM DISPLAY:

- A data point on the SUM display which is saturated at either +10V or -10V indicates a bad SUM ACQ module.

- A data point on the SUM display near zero amplitude could indicate:

    - the Cal/Local Timing module is not outputting any calibration signal.
    - the cable between the BPM electronics and the Cal Ring is broken/disconnected.
    - both PUE cables are disconnected from the BPM electronics (or are broken).
    - the cable connected to the SYSTEM SUM output of the FEP module is either broken (check SMA center pins) or disconnected from the input to the Acquisiton module.
    - both x1 gain bits (B4 and B2) are stuck "OFF".

- A data point on the SUM display which is at half amplitude (relative to other neighboring points on the display) indicates that the Cal/Local Timing module is outputting a signal, and that the signal is making it to the Calibration Ring. This leaves one or more of the following possibilities:

    - one of the PUE cables is broken/disconnected;
    - one of the gain bits (B4 or B2) is stuck "OFF";
    - either gain bit B3 or B1 (the /10 bits) is stuck "ON";

- A data point on the SUM display which is approximately one tenth amplitude relative to the other points (but greater than 0) might indicate:

    - gain bit B0 is stuck "OFF";
    - both gain bits B3 and B1 (the /10 bits) are stuck "ON".

2xDIFF DISPLAY:

- A data point on the 2xDIFF display which is saturated at either +10V or -10V indicates a bad DIFF ACQ module.

- A data point on the 2xDIFF display which has a large non-zero (but not saturated) positive amplitude might indicate:

    - the Plate B PUE cable is disconnected/broken
      If this is true, then the current SUM display will be at half amplitude; In addition, STEP 2 will yield a 2xDIFF

display identical to this one, and STEP 3 will result in a 2xDIFF display of 0 Volts.

- gain bit B2 is stuck "OFF" (similar symptoms as disconnected Plate B PUE cable, but not as likely);

- gain bit B1 (plate A /10) is stuck "ON".

- A data point on the 2xDIFF display which has a large non-zero (but not saturated) negative amplitude might indicate:

  - the Plate A PUE cable is disconnected/broken
    If this is true, then the current SUM display is at half amplitude; In addition, STEP 2 will yield a 2xDIFF display of 0 Volts, and STEP 3 will result in a 2xDIFF display identical to this one.

  - gain bit B4 is stuck "OFF";(similar symptoms as disconnected Plate A PUE cable, but not as likely)

  - gain bit B3 (plate B /10) is stuck "ON".

STEP (2): **A=10, B=0, N_BUNCH=80, cal signal, 1 MHz, t=20 msec.**

This test is used to verify:

1. The SYSTEM DIFF output of the Front End Processing (FEP) module is routed to the input of the DIFF Acquisition module;
2. The DIFF channel acquisition functions (blr, local timing, integrator and A/D conversion) are operating properly.

All data points on the SUM display should decrease in amplitude by a factor of two (relative to the plot in STEP 1); The 2xDIFF plot should consist of positive values (simulating beam at the top/outside of the beampipe), with each data point at approximately twice the amplitude of its corresponding point on the SUM display.

SUM DISPLAY:

- A data point on the SUM display which is saturated at either +10V or -10V indicates a bad SUM ACQ module.

- A data point which remains pinned at the "STEP 1" amplitude indicates that gain bit B2 is stuck "ON" (only true if the current 2xDIFF display is at 0 Volts).

2xDIFF DISPLAY:

. A data point on the 2xDIFF display which is saturated at either +10V or -10V indicates a bad DIFF ACQ module.

. A data point on the 2xDIFF plot which remains "pinned" near zero could indicate one (or more) of the following:

  . verification of a broken or disconnected Plate A PUE cable, but only if this was indicated from the results of STEP 1;

  . the DIFF ACQ module is bad;

  . the system DIFF output of the FEP module is not connected to the DIFF Acquisition module, or there is a recessed SMA pin;

  . gain bit B2 is stuck "ON" (can only be true if the SUM did not drop down to half amplitude from STEP 1).

STEP (3): **A=0, B=10, N_BUNCH=80, cal signal, 1 MHz, t=20 msec.**

This test is used to:

1. Further test the DIFF channel acquisition functions

All data points on the SUM display should remain at the same amplitude as in STEP 2; The 2xDIFF plot should consist of all negative values (simulating beam at the bottom/inside of the beampipe), with each data point at approximately twice the amplitude of its corresponding point on the SUM display (but opposite in sign).

SUM DISPLAY:

. A data point on the SUM display which is saturated at either +10V or -10V indicates a bad SUM ACQ module.

. A data point which remains pinned at the "STEP 1" amplitude indicates gain bit B4 is stuck "ON" (only true if the current 2xDIFF display is at 0 Volts).

2xDIFF DISPLAY:

. A data point on the 2xDIFF display which is saturated at either +10V or -10V indicates a bad DIFF ACQ module.

. A data point on the 2xDIFF plot which remains "pinned" near zero could indicate one (or more) of the following:

  . verification of a broken or disconnected Plate B PUE cable, but only if this was indicated from the results of STEP 1;

- the DIFF ACQ module is bad;

- the system DIFF output of the FEP module is not connected to the DIFF Acquisition module, or there is a recessed SMA pin (if this were true, you will have seen the same results in STEP 2);

- gain bit B4 is stuck "ON" (can only be true if the SUM did not drop down to half amplitude from STEP 1).

REFERENCES:

1. D. Ciardullo, "Understanding the Analog PUE Signals," BNL Booster Technical Note #214, November 30, 1992.

2. D. Ciardullo, "Estimating Beam Intensity from the Booster BPM System," BNL Booster Technical Note #206, February 11, 1992.