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A DIGITAL VOLTAGE to FREQUENCY CONVERTER for the BOOSTER GAUSS CLOCK

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A DIGITAL VOLTAGE to FREQUENCY CONVERTER for the BOOSTER GAUSS CLOCK

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I. Introduction

This note presents a new type of Bipolar Voltage to Frequency Converter. The Digital Voltage to Frequency Converter (DVFC) digitizes an analog input signal, converting it to a 17 bit digital number (16 bits magnitude plus 1 sign bit). This number is added to an accumulator at a fixed rate such as 1 Mhz.

Every time the accumulator overflows a pulse is output. If the overflow is negative a down count is sent out, if it is positive an up count is sent out. The residue, or remainder in the accumulator after an overflow, provides the current sum for the next addition or subtraction.

Section IV. describes the DVFC. Section VII. lists the detailed specifications. The basic Gauss Clock Unit will be mounted in the Booster dipole reference magnet NO. 32. Two additional units will be mounted in the two reference quads, NO. QH 25 and NO. QV 25 located in building 930A.

II. Background

Instrumentation grade Bipolar Voltage to Frequency Converters are no longer commercially available. The last widely available unit (~1970) appears to have been the Hewlett-Packard 2212B operating to about 100 Khz. This type of VFC used an integrator capable of bipolar operation with charge balancing done by a constant voltage - time feedback pulse of the correct polarity.

The HP 2212 forms the heart of our presently operating AGS "Slow Gauss Clock". It puts out both up and down pulse trains, or counts, as a function of input voltage polarity. The output frequency is a function of the magnitude of the input analog voltage.

The present AGS "Fast Gauss Clock" is made around a Burr-Brown VFC Integrated circuit. It is unipolar and runs to a full scale frequency on the order of 1 Mhz. It can only respond to a single input voltage polarity and therefore produces only up counts.

In the AGS, Booster, as well as many other accelerators, the requirement is to have a high frequency gauss clock that

operates in a bipolar fashion. The high rate accommodates large variations in B dot and the bipolar operation covers acceleration, flat top, and deceleration.

A bipolar VFC with a full scale on the order of 1 Mhz would integrate the two systems into one box. Several schemes were investigated for the implementation of a bipolar VFC for the Booster and AGS.

Scheme one used a very accurate unipolar VFC fed by a precision absolute value circuit, fig 1. A problem with this scheme, shown by R. Thern, would cause the VFC system to put out pulses, near a zero voltage input, with incorrect polarity. See appendix 1 for a more detailed explanation.

The next scheme involved a unipolar VFC with input offset so that at zero input voltage the VFC chip would output half of it's full scale frequency, fig 2. The final VFC system output would be generated by a digital circuit which would heterodyne the VFC chip output with a fixed oscillator at half scale frequency.

In practice the maximum usable full scale frequency of the system would be about 1 Mhz since VFC component linearity errors increase with full scale frequency. Only half of this scale is available for up counts, and half for down counts, so the effective range is decreased by a factor of two and is 500 Khz.

Even with "good" linearity, the up and down regions of the VFC characteristics will not match and would require calibration. The offset technique is in use at CERN, but their VFC operates with relatively low resolution (200 to 800 Khz).

To obtain a full scale range of 1 Mhz up and down (as required by the low level RF system at injection), we next considered using two VFCs set up so one would operate for positive input voltages and the other for negative inputs. The first problem is to clamp the inactive VFC's integrator so that its output does not drift off to the power supply rail. This would cause saturation recovery errors. Unipolar VFC chips have a unipolar charge pump to reset the integrator after a pulse, so charging the integrator in the wrong direction causes the chip to go open loop and results in recovery times on the order of tens or hundreds of milliseconds. At least two schemes to clamp the VFC integrators were proposed. Although adding to complexity, this problem seemed soluble.

An additional problem was how to get good operation near zero volts input. What appeared to be an optimum solution for this design was to use three VFC chips, as shown in fig 3. Two would cover the gross ranges of approximately +/-5 mV

to +/-5 Volts, and one would operate with the offset technique from +5 mV to -5 mV. Precision analog circuits would select which VFC to port to the outside, and indicate up or down polarity.

This scheme however, causes an error that could be as high as in the scheme of fig. 1. At the transition points of +5 mV and -5 mV both the center VFC, and the respective +/- 5 mV to +/-5 Volt VFC would be running at exactly the same frequency. The problem is at hand off from one chip to the other. Their phase relationship would be undetermined since each has been running independently.

The VFC chips used in this scheme are synchronous VFC's which run on the same 2 Mhz clock. The fraction of clock pulses which appear at the output of each VFC chip determines it's output frequency. Two VFC's operating on the same clock do not necessarily use the same clock pulses to generate a lower frequency. Their phase relationship is not well defined and changes over time with small frequency changes.

Multiple pulses, or lost pulses would occur routinely. Some sort of synchronization technique near hand off may be possible.

The Digital Voltage to Frequency Converter (DVFC) described here grew directly from attempts to overcome some of the problems outlined in the above schemes and from analog experiments.

III. VFC Requirements and Definitions

A key point in the design of a VFC for our application is that the VFC bandwidth, full scale frequency, and resolution are separate issues. The signals we are converting generally represent relatively slow waveforms, such as the dB/dt of a main magnet.

The magnet voltage, and therefore B dot, is influenced by several power supply ripple frequencies, generally under 2 Khz for the fundamental. Harmonics of the ripple frequencies and rectifier commutation certainly cause much higher frequency components, but these components are attenuated by the accelerator beam pipe.

With present technology, the DVFC to be described may have a maximum input signal bandwidth of about 250 Khz. Some passive integration of the analog input signal may even be desirable to limit the bandwidth to the range of 20 Khz to 50 Khz, and hence reduce the effects of noise.

With 16 bit Analog to Digital Converters a frequency

resolution of about 15 Hz out of 1 Mhz is available. To get full 16 bit resolution across a bipolar scale, such as -10 V to + 10 V, the system uses a positive ADC and a negative ADC in an autoranging environment. This technique is not the same as "stacking", a questionable way of generating more bits in one digital word across a continuous voltage range.

The maximum frequency for the new design remains at 1 Mhz, the original goal. It will be seen from the description of the DVFC that a full scale frequency of up to 10 Mhz is relatively easily implemented, but, the resolution would drop by a factor of 10, and hence greater accuracy is sacrificed.

IV. The Digital Voltage to Frequency Converter

The DVFC (fig 4) consists of instrumentation amplifiers and low pass filters feeding sampling 16 bit ADC systems, a gating system for choosing digital words from the positive or negative ADC, and an accumulator. The ADC system digitizes the input waveform and adds or subtracts the resulting binary number from the accumulator's sum register in 2's complement arithmetic. Accumulator overflow in the positive or the negative direction results in an up or a down count.

The instrumentation amplifiers have cross connected floating inputs. When the input signal is positive on one, it is negative on the other. The amplifier stage will have low pass filtering to prevent digital aliasing with high frequency noise signals (such as the RF system).

Both 16 bit 500 Khz ADC's will have scales of 0 to 10 volts. Since the instrumentation amplifiers are cross connected, only one ADC will be in scale at any given time. Each ADC board outputs an ADC underflow bit when it is out of range in the negative direction (000...000 or below). A 2 to 1 line data selector chooses which ADC board's number will be entered into the Arithmetic Logic Unit (ALU) input based on the ADC underflow bits.

ADC Underflow bits are also used to direct the ALU to add or subtract the new number from the accumulator. In the event of inconsistent ADC underflow bits, both underflow or both in range, the ALU is halted for a one microsecond cycle. This is the same as a zero addition to the accumulator.

Each new ALU result is saved in the sum register. If the operation does not result in an overflow, there is no up or down count.

If the operation results in an overflow, an output pulse is directed to the up or the down output port as appropriate.

The same pulse is also ported to set or reset the sign register, since the sign of a 2's complement result is incorrect on overflow.

V. The Pick Up Coil

A long coil is used to generate the DVFC input voltage. It consists of two separate, isolated, center tapped windings, one for the primary dipole gauss clock, and the second for the "hot" standby spare clock. Both coils are wound to give full scale voltage, 10 V, at 10 T / Sec.

The coils are wound over each other on an Extren coil form which is then curved to match the magnet curvature and bolted to an Extren base. Extren is a "G-10 like" material with a better temperature coefficient then G-10.

The base is supported in a standard section of dipole beam pipe so the coil is along the beam center line. The coil and Extren supports have been designed to maintain position and be relocatable to approximately 10 mils.

The pickup coils will be connected to the DVFC front end by RG-22U, double shielded twisted number 18 wire. The ~20 foot length of RG-22U will be run in steel electrical conduit from the magnet to the DVFC rack.

VI. System Errors

Many standard errors appear in the system. They are, however, very well defined and generally caused by a specific system block. An important difference between the DVFC and schemes using separate VFC chips is that now there is only one system oscillator (the accumulator with overflow), so no synchronization of separate independent VFCs is needed.

The analog instrumentation amplifiers will be powered by isolated power supplies to minimize common mode pickup. Their linearity is very good at about .001%. Drift with temperature is also very good at .25uV/deg C, and temperature stabilization will minimize this error.

The front end of both ADC boards is enclosed by G-10 walls. A copper plate, which runs under all of the IC's and hybrids, is held at constant temperature by a thermoelectric heat pump and a closed loop commercial heat pump controller.

The instrumentation amplifier and the sample and hold

circuit will have some significant noise output, probably on the order of several uV's P-P. This is below the ADC LSB of 153 uV, but, still an additive error. The system noise including coil connections is expected to be significantly higher. Some of these parameters are listed in section VII.

VII. Booster Dipole Gauss Clock Specifications

Coil

Form Length : 104 inches long, 2.64 meters
(dipole magnetic length used is 2.40 meters)

Width : .384 inches, .975 cm

Inner winding : 40 turns of #30 wire center tapped
Outer winding : 38 turns of #30 wire center tapped

Form follows the magnet center line

Positioning : Coil and base assembly are fixed and relocatable to +/- 5 mils

DVFC

Analog to Digital Converter: Burr Brown ADC701KH
16 Bits + sign bit
500 Khz Sample rate

DVFC Input bandwidth (-3dB) : 40 Khz

ADC board front end temperature control : 0.1 degree C

Internal Clock : 10 Mhz oven stabilized
Stability of internal clock : $3 / 10^7$ per year

Full scale frequency : 1 Mhz at 10 V input (B dot = 10T/Sec)

Voltage to Frequency Resolution : 153 uV or 15 Hz

Repeatability : $2 / 10^5$

Output pulses : 20 Volts, 100 Nano Seconds wide
on two lines, Up and Down counts

(Note : Most users will receive Gauss Clock information from the Gauss Time Line generator. The Gauss Time Line generator provides predetermined magnetic field triggers based on accumulated Up and Down pulses from the Gauss Clock.)

VIII. Conclusion

Implementation of a bipolar VFC using unipolar VFC chips appears difficult, if not impractical. Development of a linear bipolar VFC, with bipolar integrator, would require a large amount of R&D.

A new bipolar DVFC can be built using commercially available state of the art components. DVFCs share many of the same errors as the analog counterparts, but the errors are well defined. It's primary advantage over separate VFC chips is that it contains one common phase continuous oscillator.

Thanks to M. Brennan, B. Culwick, R. Frankel, A. Soukas, R. Thern, and several others who have made very useful comments. D. Mangra designed the mounting system for the dipole pick up coil and did calculations for the thermoelectric cooling system. G. DeGregory and R. Horton are currently building the first production DVFC.

IX. Future Work

1. Measurement of the reference dipole field and calibration of the gauss clock by Hall probe and NMR will be addressed in a separate technical note. The Artificial Gauss Clock and switching system from the primary clock to the "hot" standby clock will also be documented in a future note.

2. The quadrapole gauss clocks.

3. The AGS gauss clock will be constructed similar to the Booster dipole clock. It will be located near the AGS reference magnet in the basement of the MG set building.

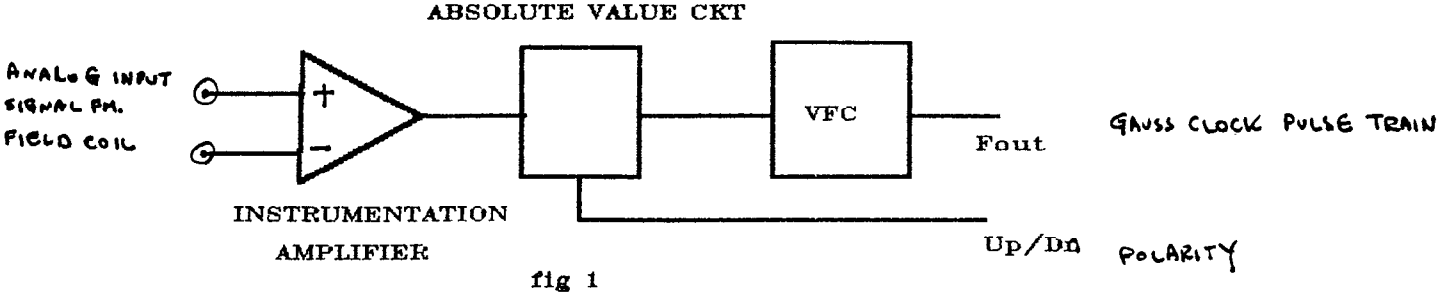


fig 1

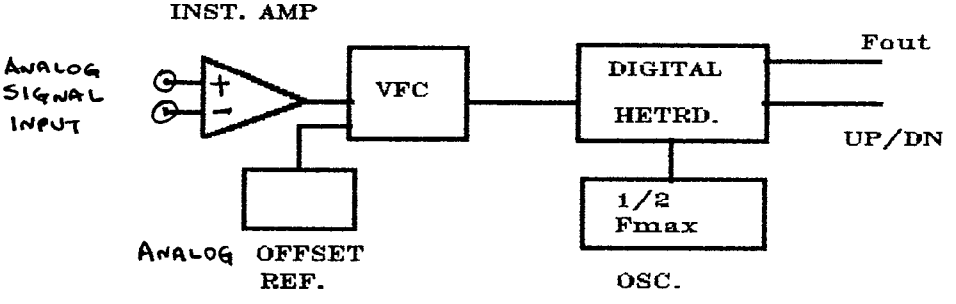


fig 2

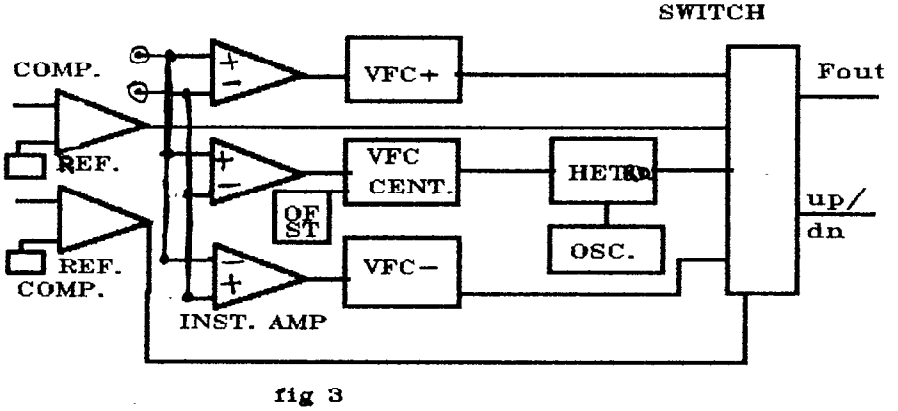
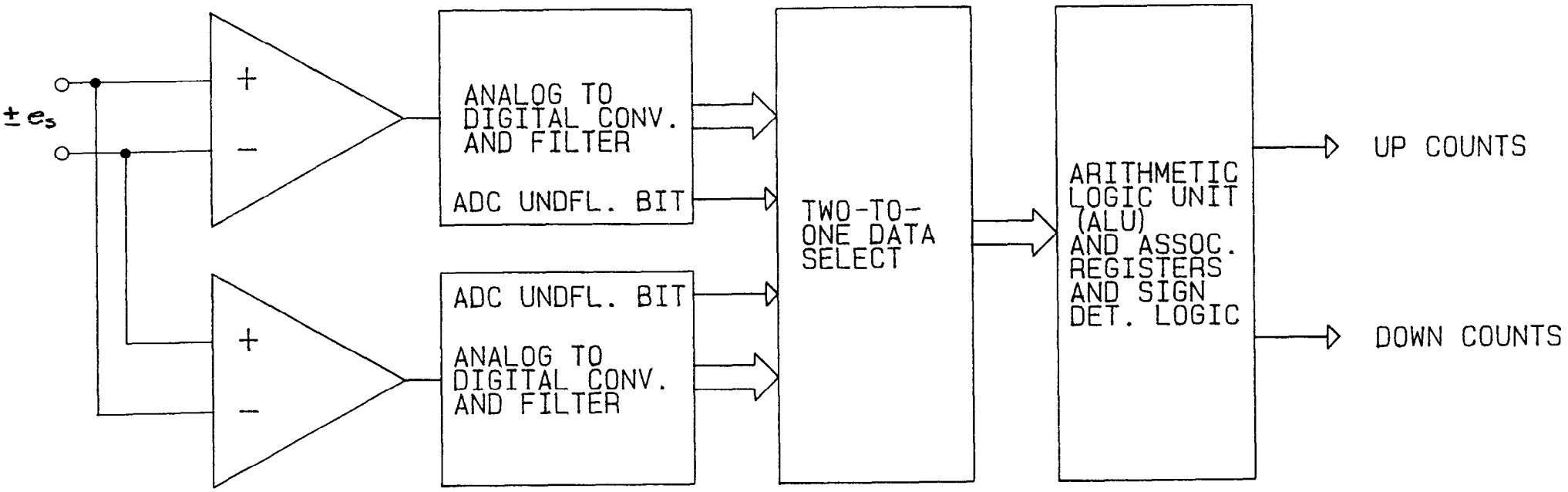


fig 3

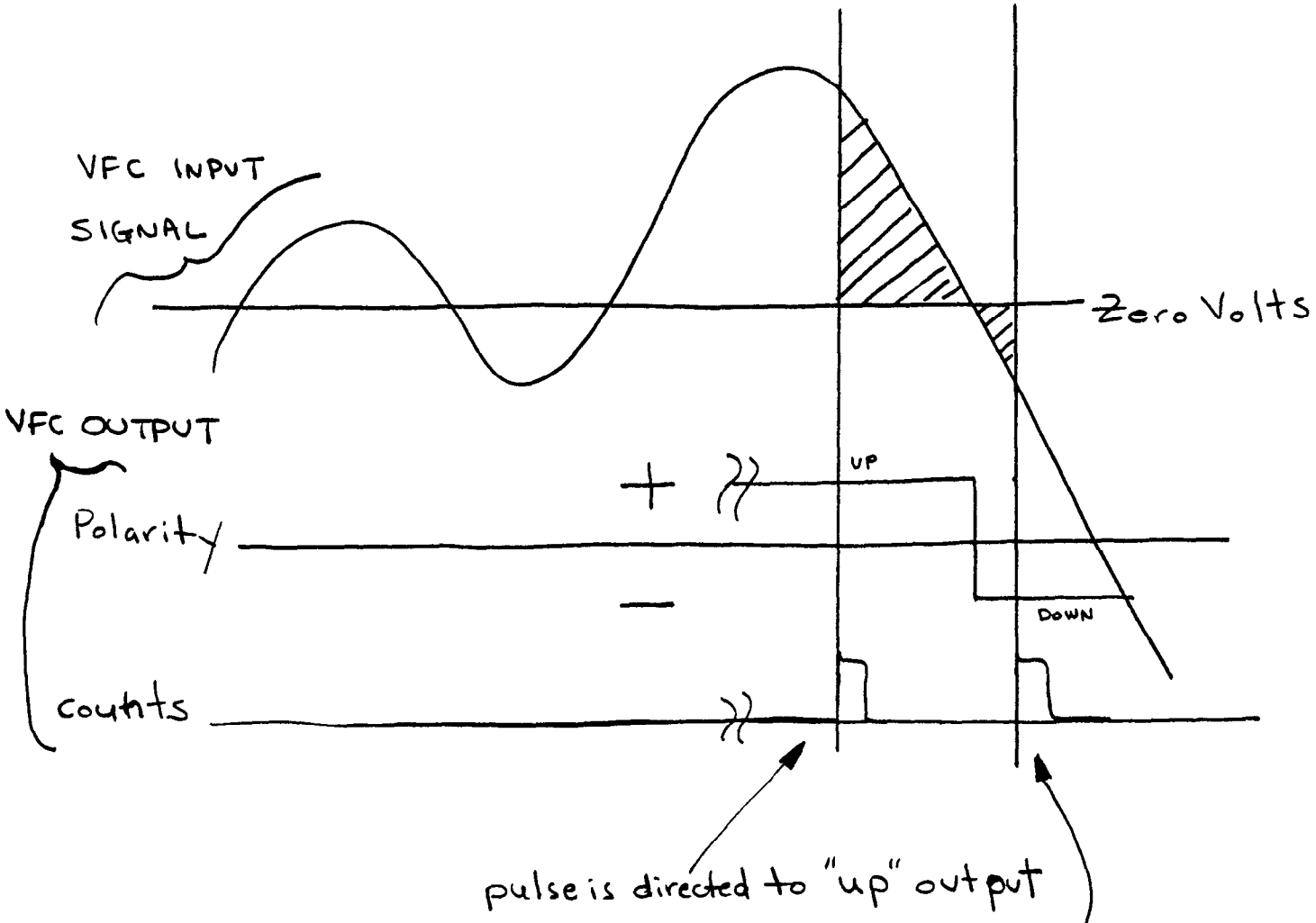


THE DIGITAL VOLTAGE TO FREQUENCY CONVERTER (DVFC)

FIG. 4

APPENDIX 1

AN ILLUSTRATION OF THE ERROR NEAR ZERO VOLTS IN THE BIPOLAR VFC CONSTRUCTED WITH AN ABSOLUTE VALUE AMPLIFIER (AS DESCRIBED BY R. THERN)



pulse is directed to "up" output

most of charge leading up to output pulse is from + signal, but since last bit of charge is during negative input, the output pulse is incorrectly directed out as a down count.