BNL-105211-2014-TECH

Booster Technical Note No. 167;BNL-105211-2014-IR

BOOSTER LRM SYSTEM HARDWARE SPECIFICATION

E. Beadle

June 1990

Collider Accelerator Department

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC)

DISCLAIMER

BOOSTER LRM SYSTEM HARDWARE SPECIFICATION

BOOSTER TECHNICAL NOTE
NO. 167

E. BEADLE and G. BENNETT

JUNE 7, 1990

ALTERNATING GRADIENT SYNCHROTRON DEPARTMENT
BROOKHAVEN NATIONAL LABORATORY
UPTON, NEW YORK 11973

BOOSTER LRM SYSTEM HARDWARE SPECIFICATION

E. Beadle
G. Bennett

Introduction

The Booster Low sensitivity beam loss Radiation Monitor system is described. This document presents details of the proposed system design, including a block diagram ,specifications of each of the component modules, a description of the detectors and their placement, and timing considerations. An appendix estimates the signal and noise amplitudes on which the choice of integrator capacitor and input resistor is based.

The system consists of 48 ring detectors, plus 8 in the LTB line, 8 in the BTA line, and 15 spare channels. An 80th channel will be used to digitize the Booster CBM signal. Electronics will be installed in the Upper Equipment Bay, building 930. A comprehensive system manual is being prepared, to contain all pertinent information, including distributed documentation engineering changes, test procedures and results, calibrations, etc.

Detectors / Siting

The Booster low sensitivity detectors will be coaxial cable ionization chambers similar to the AGS low sensitivity units now in use. The Booster chambers will be 15' long, mounted close by the median plane near the inside wall of the tunnel, approximately 30 inches radially inside the reference orbit and 1 inch below. There will be 48 chambers in the ring, one spanning each half cell, with the ends of the chambers overlapping at the middle of each dipole magnet reference location.

In addition there will be 16 more chambers, 8 each in the injection and extraction lines of the Booster. The 4 detectors in the upstream section of the LTB are 15' long, the 4 downstream of the shielding wall are each 12' long. The detectors in the BTA line are all 21' long, 3 on the Booster side of the shielding wall separating the AGS and Booster, 5 downstream. These 16 transfer line detectors will be positioned below the beam line at the side of the supports for the beam line components. This position results in potentially less sensitivity than on the beam plane, but experience with similar detectors on the tunnel wall in the HEBT line shows sensitivity is still adequate. The chambers will be arrayed contiguously, with overlap where necessary. Provisions for up to 15 expansion channels will be available, for a total of 79 detectors.

Hardware Description

The system architecture is shown in figure 1. Each detector is biased at 200 VDC using a floating supply. The detector output is integrated, sampled, and digitized. An analog mux

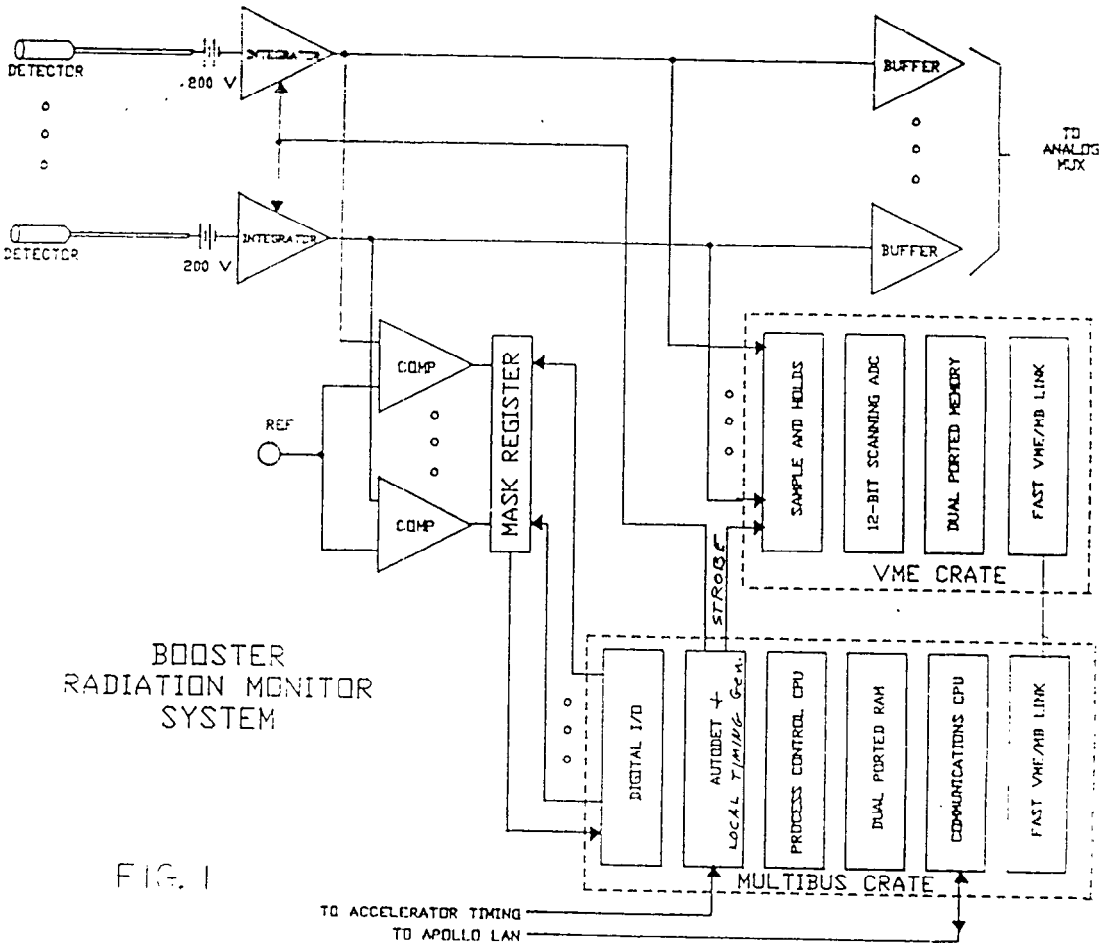

FIG. 1

system is used to provide any 4 of the 79 channels for observation in the Main Control Room. The instrument controller generates the strobes to the S/H modules. The ADC then automatically advances through the 80 channels, digitizing each detector channel, and the beam intensity signal, in turn. The integrators are reset after the ADC scan is initiated. The ADC output is stored in a dual ported memory that is shared with the instrument controller through a "Bit-3 interface".

Integrator outputs which exceed preset "trip levels" at each comparator input can be used to trigger the read/reset process, providing an expanded dynamic range for the system. Integrated detector signals from the Booster ring will be fed to discriminator modules which will have all trip levels set at the same value, about 80% of ADC full scale, 8 V.

The strobes from the instrument controller will be triggered by either the central timing system or the comparators. Timing system triggers are generated in response to user requirements. Note that LTB and BTA detector trips do not initiate ADC scans.

Additionally, comparator signals can generate a beam inhibit signal. The LTB and selected spare signals (16 channels maximum) can trigger the Linac Fast Beam Interrupt circuit via a Beam Interrupt module; comparator outputs are fed to the instrument controller for identification of tripped channels. Similarly, any BTA signal or selected spare (8 maximum) which trips a comparator will output to an external circuit forbidding further injection into the Booster. These comparator outputs also go to the instrument controller for tripped channel identification. The LTB, and BTA interrupt signals are automatically cleared at the start of the next Booster cycle. Therefore, the signal levels are only held by the BLRM system for the balance of the current cycle. For proper inhibition the external circuits must latch the signals, and provide the logic to recognize the desired fault status (e.g., 2 of 4 detectors tripped, or 2 trips per 3 cycles, etc.). An interrupt is indicated by a level <0.8V; normal operation (no interrupt) is signalled by 12 to 15V to the Linac, and by a TTL logic high to the Instrument Controller, referenced to the BLRM rack ground. Comparator trip levels for the "non-ring" detectors will be set based on operational requirements to be established.

It is required that the LTB comparator response be fast enough to protect equipment if the beam is mis-steered. To this end the integrator input resistor for these channels is to be 500Ω, giving a "rise time" (0-90%) of 16 μsec. Since the reset duration of the integrators is 10 μsec, during which time signal is lost, it is planned that a read/reset cycle be initiated programmatically immediately before injection. Otherwise, a read/reset cycle could occur fortuitously during injection, shrouding a signal large enough to trip the interrupt. The standard ring integrator input resistor, 1 kΩ, gives a rise time of 30 μsec, but experience with the present AGS system suggests such fast losses are not achievable. In the case of the BTA channels, the signal duration is but a fraction of 1 μsec. Such fast response is not practical, or necessary. The integrator resistor for these channels will be 5 kΩ, giving about 130 μsec rise time, which is adequate to inhibit the succeeding injection pulse, and provides buffering in the capacitance upstream of the integrators. A programmatic reset before extraction should be provided to prevent signal loss during reset.

A mask is used to prevent malfunctioning or uninteresting channels from generating read/reset strobes. The LTB comparator signals,and selected spare channels which also feed the FBI, will not be maskable, nor will the BTA comparator signals and selected spares which supply the BTA Interrupt. The mask can be read back through the Instrument Controller on a byte by byte basis.

Note that insertion of a harp is presumed to provide loss beyond operating trip levels for some detectors in the transfer lines. Unless the harps are fully retracted contact switches on each harp will activate circuitry to disable up to 4 front panel selected comparator signals going to the Beam Interrupt modules. MCR can override the beam interrupt disable circuitry via a bit in the instrument controller.

Module Descriptions

Integrators: Standard BNL Module, 8 channels, switchable capacitance (100 pF & 920 pF), Slew Rate 5 x 10^5 v/s, 1 kOhm input resistance (ring units, see text for LTB and BTA channels). (AGS/EPS tech note 129)

Analog Mux: Standard AGS control system mux and interface.

S/H, MUX: Datel p/n DVME-645, 16 ch/module, cascadable to 256 ch, Droop rate 1.2 uv/us, 6 us settling time to .01%, .05 % Accuracy.

A/D Conv: Datel p/n DVME-601, 12 bit ADC, 64 KB dual port RWM, 170K samples/s maximum.

Comparator: Standard BNL module, 16 ch, individual control over set points, external control or monitor of set point, open collector outputs on TTL lines.

Reset Mask: Custom module allowing any of 72 input signals to be gated off via Instrument Controller. Mask readback is provided.

Beam Interrupt: Custom module, 8 ch, active low output reset by SOQC or equivalent results from any input going high.

Analog Buffer: Standard BNL module, 32 channels, unity gain, approximately 3 MHz bandwidth.

Bias Supply: Standard BNL module, 8 ch, 200 V, 15 uA nominal, >100 uA max output. (AGS Div Tech note 146)

Data Processing

Note that a separate specification defines the software requirements. The present discussion is included for orientation to the hardware.

The present RLRM program allows access to digital and graphic data on a pulse by pulse basis, and logging data to a file. The main original operating mode allowed one time window per cycle, plus totals for the cycle. A second mode (no longer used) measured the outputs at regular intervals to determine peak response during an interval and the interval producing peak response. A third mode generated a real time display that showed the total radiation response vs time via a D/A.

The minimum time for a window is limited by the ADC scan rate to approximately 1 ms for this system (80 channels), and the maximum is limited by the acceleration cycle time. Temporal resolution is specified at 1 ms. However, the accuracy of the start/stop times may be

affected by conflicts between hardware and timing system sample commands. The local timing generator will arbitrate the conflict and delay the second sample command causing the contention. The worst case delay is determined by the ADC scan rate, but the data stream informs the user when the windows actually start and stop, within 1 msec.

To facilitate viewing the (integrated) analog signals it may be useful to reset the integrators at regular intervals, thus generating a pseudo-differentiated display more suggestive of the instantaneous ionization current. This can be accomplished via an oscillator/timer with user selectable period which will periodically initiate the A/D scan throughout the accelerator cycle. Note that like the comparator generated triggers, these timer generated triggers are transparent to the user window output. The primary user may suppress the timed resets during selected intervals or disable the feature completely.

A mask is provided to prevent selected channels from initiating the read cycle, either because of user operational requirements or because a channel is defective. Since a user may have the option of setting the mask, when two or more users are using the system a priority must be assigned and only the highest priority user can alter the mask. Additionally, only a system operator can alter a defective entry in the mask. To avoid confusion, the software should inform all lower priority users that they cannot alter the mask. The primary user should be able to update the mask interactively but no faster than once per cycle. A sample of a mask display is shown:

A1 A2 A3 A4 A5 A6 ... F2 F3 F4 F5 ...

D M M A A A A D M A

D = Defective M = Masked A = Active

To handle the 12 bit ADC output a 16 bit word size is recommended. If the data for each detector is accumulated in the dual ported WRM for each user set time window, then the ADC can read full-scale a minimum of 16 times without overflowing the data registers. The maximum number of full scale readings expected is 10 per cycle which indicates 100 % beam loss at full energy. It is desirable to read and process the data from the ADC dual port RWM as it becomes available. However, this may be impractical as this rate can approach 200 Kbytes/sec. Therefore a more reasonable requirement is to read and process all the data by the end of the current AGS cycle, or the next cycle. This reduces the worst case average data rate for a 3 s machine cycle to less than 10 KB/s.

Gas System

Argon gas at 10 PSIG will be distributed to the detectors in 4 loops: LTB, ring sectors A to C, sectors D to F, and BTA. Each loop will have all detectors in series, starting with a gas cylinder and regulator, ending with a pressure switch to close an alarm circuit when the

pressure drops below about 8 PSIG. Detector to detector connections will use plastic tubing to maintain electrical isolation, other gas lines will be copper tubing.

Calibration and Troubleshooting

1. A set of resistive loads to replace detectors will be available for system static testing.

2. A calibration source (Cs-137) is available for detector testing and calibration.

3. An estimate of induced activity and system performance may be available by reading detectors during invert.

4. The gas charging system status will be monitored via the computer.

Timing Requirements

The basic timing relationships between the required outputs from the timing board in the instrument controller are shown in figure 2. Timing considerations are expanded and further refined in a specification document devoted to the Instrument Controller interface. In response to an integrator exceeding the comparator set point (typically 80% of A/D full scale) the mask output becomes active. The mask strobe then activates the timing sequence which outputs a sample and hold strobe followed by ADC start and integrator reset.

The analog system response time is determined by the time constant of the input circuit ($C_{cable}R_{int}$), the amplifier slew rate (nominally 1 v/μsec), and the integrator discharge time constant ($C_{int}R_{FB}$). Typical cable capacitance is 6 nF (300'·20pF/ft), and the integrator resistance is 5kΩ, producing a time constant of 30 μsec. The slew rate suggests that the amplifier can go full scale (10 V) in not less than 10 μsec.

R_{FB} is 440 Ω. Nine time constants (4 μsec) are required to discharge the integrating cap to 0.1%. The standard reset duration is 10 μsec.

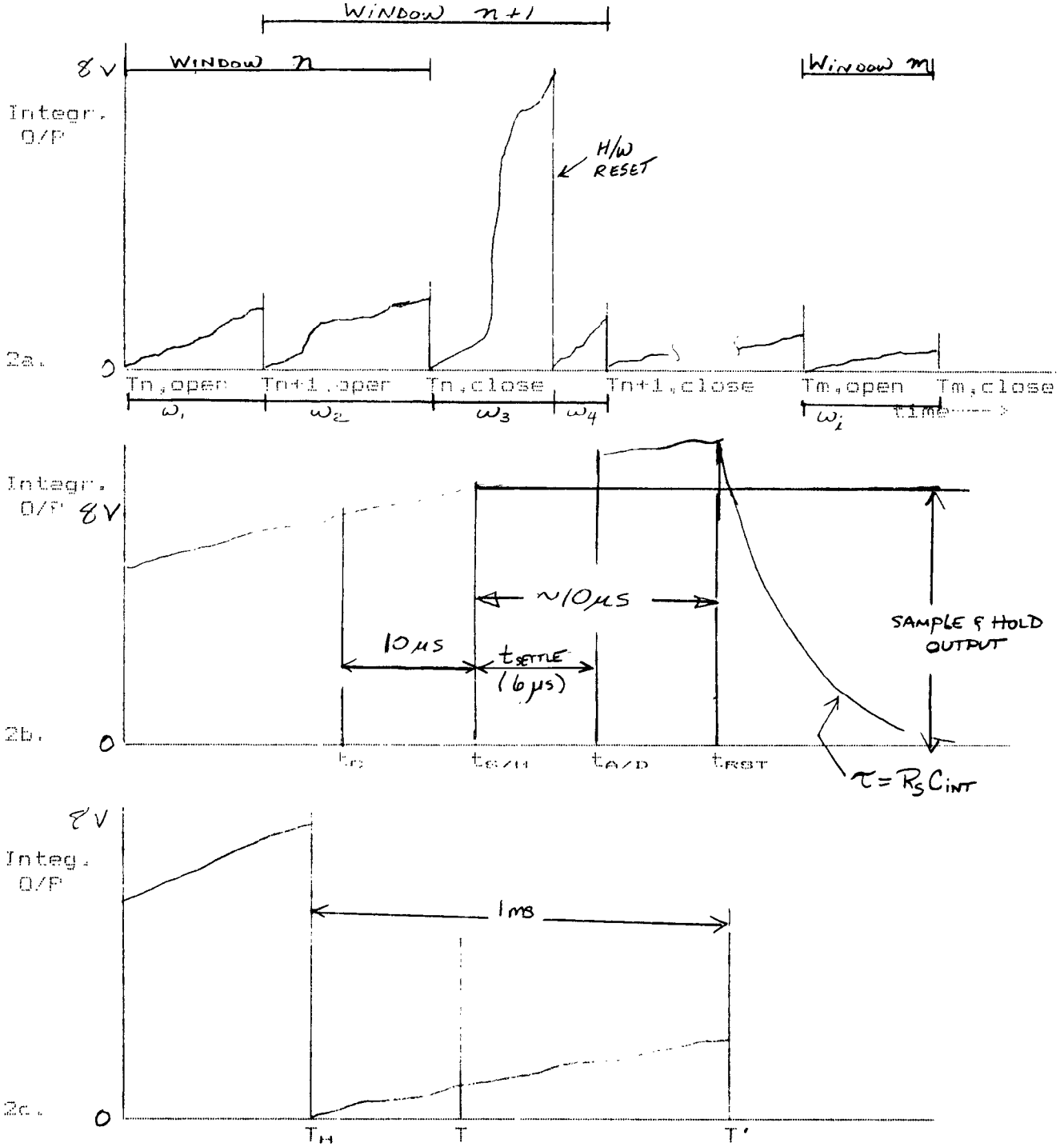

Fig 2a. Overlapping windows result in contiguous sub-windows. Hardware reset (w3) is noted in data but creates no conflict unless occurring less than 1 msec (80 ch sys) before user window trigger.

Fig 2b. Hardware reset trigger sequence, t_D=comparator generated trigger, $t_{S/H}$=sample, $t_{A/D}$=start conversion, t_{RST}=reset integrators.

Fig 2c. User window trigger (T) occurring within 1 msec after hardware trigger (T_H) will result in arbitrator generated delay to T'.

APPENDIX A

SIGNAL and NOISE ESTIMATES

The larger of the two integrating capacitances was calculated to give 10 V output with 10% beam loss at full energy; the smaller capacitance was to give less than 25% of full scale output with the anticipated input noise level. An estimate of the ion chamber signal to be expected from the Booster low sensitivity system may be obtained from data from the AGS standard detectors, which are almost identical to those proposed for the Booster, but are 30% longer. The AGS detectors are mounted below the girder, spanning two magnets. Figure I shows curves, each of which is the mean of two runs using the flip targets to produce beam loss. At the lowest energy (1 GeV) the data reflects the largest signal obtained from any detector (J12 when using the J5 target, and K4 when flipping J19), at higher energies the largest signals are from the detectors nearest the targets.

Figure I indicates .7-2.2 counts per $2x10^{10}$ protons lost at the full design energy of the Booster, 1.5 GeV. Assume, conservatively, that the Booster magnet structure and detector geometry are equivalent to the AGS case, and use the minimum value, .7cts per $2x10^{10}$. One count in the present RLRM system corresponds to a charge of 1.5×10^{-10}C (1 megohm feedback resistor, 10^5cts/15V·sec V/F conversion factor). The design intensity for the Booster is 1.5×10^{13}. Thus a 10% loss at full intensity and energy produces a charge

$$Q=(3.5 \times 10^{-11}\text{ct/proton})*(1.5 \times 10^{-10}\text{C/ct})*(1.5 \times 10^{12}\text{protons})$$

or 8×10^{-9} Coulombs. The integrator capacitor to produce full scale output (10 V) is

$$\text{Cap}=8 \times 10^{-9}\text{C}/10\text{V}=.8\text{ nFd}$$

Uncertainties in the estimate include influence of the AGS scraper (capturing up to 2/3 of the lost protons), differences in effective shielding in the magnet structures and in detector geometry, and the spatial (i.e. azimuthal) distributions of the prompt radiation in the two accelerators. The first is probably the largest and could reflect an increase in signal by a factor of three in the Booster without a scraper.

System noise measurements in the environment of the AGS with a 100 pF integrating capacitor and 5 kΩ input resistor showed 1.5 V peak-peak, predominantly 60Hz. With 500 Ω input resistance the noise amplitude increased to approximately 2 V peak-peak.

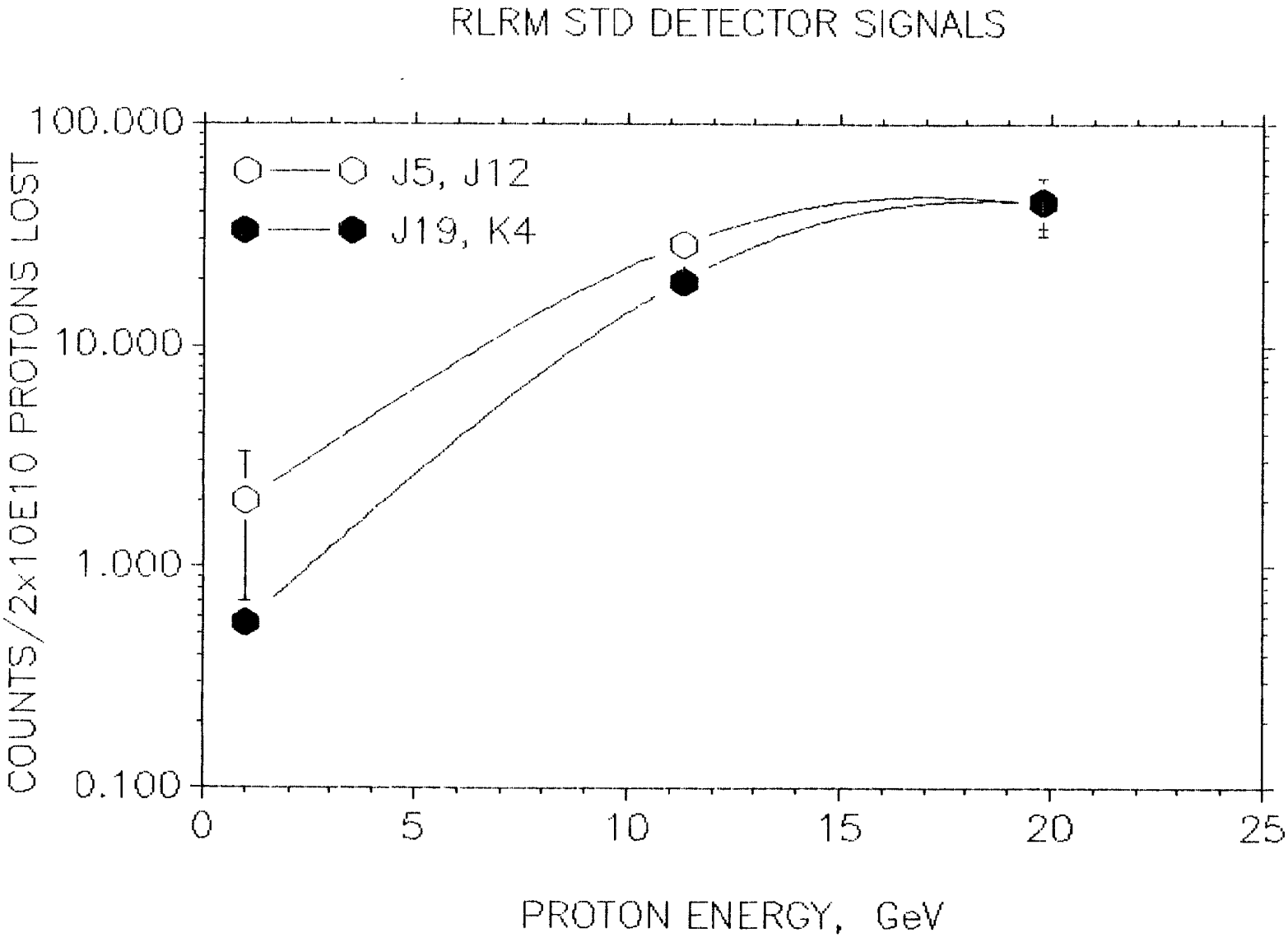
RLRM STD DETECTOR SIGNALS
100.000
10.000
1.000
0.100
COUNTS/2x10E10 PROTONS LOST
J5, J12
J19, K4
0
5
10
15
20
25
PROTON ENERGY, GeV

FIG. I