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AGS BOOSTER STANDARDIZED POWER SUPPLY CONTROL

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U.S. Department of Energy

USDOE Office of Science (SC)

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I. GENERAL

A. The AGS Booster Project is adding about 150 power supplies to the AGS complex. In order to simplify the control and interlock, as well as the computer interface objectives, standardized design tasks in the control of the power supplies will be followed. The initial goal is to make even ps's of diverse functions have identical control interfaces. An additional goal is to reduce manpower costs by decreasing labor requirements for the power supply controls and for the device controller software. This standardization will also result in a more uniform set of hardware and software tools. At the same time, flexibility is built-in to the scheme to enable implementations utilizing different technologies.

B. This note will define the standard power supply (ps) control scheme for units used in the AGS Booster. Standardization is accomplished by defining the ps control philosophy and typical sets of hardware for the computer interface, for the control panel layout (lights, pb's, mechanical considerations, etc.), and for the standard low-level analog controls. These standards will apply to all ps's whether developed in-house, or purchased. Hopefully, standard "off-the-shelf" designs of both control hardware and software packages will be available to be used by all ps design personnel, both now and in the future.

II. PS CONTROL: STANDARD PHILOSOPHY

A. The basic ps control states and their definitions are as follows:

1. AUXILIARY OFF (OFF): All external power (24Vdc, 115Vac, 460Vac, etc.) is connected to the ps input terminals, however, all ps functions are in a de-energized state.

2. STANDBY (SBY): This mode, when activated, applies control power (usually 24Vdc, 24Vac, or 115Vac but no greater), to all the ps control functions with the intent of preparing the unit towards a READY and a final dc ON state. This means that all ps functions (e.g. relay power, modular $\pm 15V$ & $+5V$ ps's, op-amps, cooling, filaments, heaters, etc.) are energized. Also, time delay in process (TDIP) relays are initiated.

3. RESET (RST): This command (which is not an independent state) is sent simultaneously with SBY and/or ON and resets any or all non-cleared, or tripped, ps faults. This is in preparation of attaining a READY status which enables the final dc ON state. It may have to be repeated, or sent

as many times as necessary until all interlocks are satisfied, especially with TDIP control relays.

4. HI V or HI I DC ON (ON): This state energizes the main ac and/or dc (if available) contactor(s) of the ps and energizes (i.e. opens) all dc shorting contactors or relays. This defines a state of power energization of the ps load (i.e. magnet, capacitor bank, kicker, etc.).

5. IDLE: This is a dc ON subset condition (i.e. load current or power is ON) in which the ps output current is driven to a minimum regulated or controlled value. This is an operational function (e.g. to save energy) usually accomplished by reducing the ps analog reference or adjusting a feedback loop value such as gain.

6. CONFIGURATION: This command changes ps operation from one setup to another and can be user defined. For example, it may be a polarity reversal, it may change an output magnet current pulse width, or alter a maximum voltage or current range, etc.

Further clarification of the above definitions is presented in figure 1, where a simplified ps state diagram is shown.

It can be seen from figure 1 that one can go from the OFF state to the SBY/RST state and vice-versa. Also from the SBY to the ON state (via RDY) and the reverse. It can also be seen that one cannot go from OFF to ON directly, but can go completely OFF from the ON state. The latter step bypasses the SBY state and turns all auxiliary systems off. This should be avoided in order to prevent any associated TD's when returning back to the SBY state (e.g. warmup or cooling to reach the steady state operating temperature ranges). After an interlock tripout, the ps goes to SBY/FLT mode and the SBY/RST command must be exersized to get the unit to the SBY/RDY mode.

Figure 2 shows a schematic diagram implementation of the ps control states described above. Also shown are the status and fault indications of the ps. This figure is discussed further in section B, below.

B. PS CONTROL IMPLEMENTATION

A schematic diagram showing a standard ps control implementation in relay hardware logic is given in figure 2. The circuit presents the basic control philosophy that must be adhered to. Figure 2 shows a remote/local selector switch. This selects between remote (i.e. remote control panel, computer) or local (ps location) operation. Further, we see in figure 2 that the SBY/RST pb's are ganged together. Other features that are preserved in this design and must be in all other design schemes are that:

1. all interlocks (faults) are latched,

2. if an interlock is either reset or self-clears, the ps unit does not automatically come ON, but that the ON command must be re-issued,

3. all interlock and control power is 115Vac or less. All other power, with the possible exception of security interlock power, does not enter the ps via any other means than the SBY mode,and

4. isolation is preserved between the control, the ps and the indication (via relay contacts and/or opto-couplers).

C. LOCAL CONTROL; LIGHTS; MECHANICAL CONSIDERATIONS

Although all ps's will be interfaced and operated remotely by the AGS control computers, they shall have a means of local control for testing purposes, or emergency operation. Local, in this case, refers to the ps location.

The local ps control panel in the normal control scheme consists of three push-buttons (dedicated to the control functions defined earlier), and four (five) indicator lights (corresponding to the ps states). Also, a remote/local switch shall be mounted. Additional fault status lights may be utilized as necessary. The three push-buttons shall be labelled OFF, SBY/RST, and ON. The four (five) lights shall be labelled as follows and shall be of the colors indicated:

Name	COLOR
OFF	green
SBY	amber
FLT	white
(RDY	blue)
ON	red

The additional panel lights shall be colored white when they define a fault. They shall also be labelled by the fault name. Other intermediate ps states or information, if any, shall be identified and shall use a different color than those previously selected above. (e.g. polarity-l.green, TDIP-yellow, WARNING-orange, etc...).

The local control panel shall have three connectors mounted on it. The first, which shall be a 37-pin sub-miniature D type, shall be wired to the ps. The second and third, which shall be sub-miniature D type, 25-pin and 9-pin, shall connect to the remote control panel. The analog dc reference in the local mode is supplied by a potentiometer mounted on the local panel; the ps output controlled variable (V,I,etc.) shall be wired to test points on the front panel for monitoring. In the remote mode, the reference and

readback voltages are supplied through the 9-pin D connector. A typical layout of this interface is shown in figure 3.

III. BOOSTER IMPLEMENTATION

The description given in the preceding sections outlines the basic control philosophy of standard AGS ps control. The schematic hardwired diagram is given in figure 2 and the local control panel mechanical layout in figure 3. In this section we outline a more modern, PREFERRED, implementation for the Booster ps's which utilizes programmable logic controllers (PLC's). The PLC field has matured to the point where it is the preferred scheme for industrial process controls. PLC's are readily available from a multitude of manufacturers ranging from simple plastic boxes, to large distributed, networked control systems. They have demonstrated reliability in noisy industrial environments. They are also very flexible. Since they are microprocessor based, functions can be programmed and hence modified easily. They can also be expanded via the use of analog modules such as DAC's, ADC's, signal conditioning modules, and PID type feedback control units.

In the following we describe the use of PLC's in the control of ps's. A PLC consists of a physical crate and a set of plug-in modules consisting of a master control (cpu) unit and the necessary input/output (I/O) modules. The choice of input and output voltages for the modules is quite varied, up to 125V. I/O isolation is provided. Most design options that can be made in PLC module choices relate mostly to modularity. For example, a choice that can be made in the design is whether to use a single PLC with its set of I/O modules to control a single ps, or whether to use a design in which a single PLC controls multiple ps's that share the cpu and I/O modules. This is because of the nature of some of our ps designs and layouts. Also economic factors play an important role.

A. HARDWARE

The basic implementation in the use of a PLC to control a ps is shown in figure 4. The schematic shows that the PLC is not only used as the interface tool (to the device controller), but is integrated in the design of the ps in terms of interface, control, interlocking, and indication. When using the PLC for interlocking purposes, some of the most crucial interlocks (such as ACOL, DCOL, DCOV, etc.) shall be hardwired to the main RDY relay or the main contactor to minimize delays in disconnecting the ps from the power line, or in performing a crowbaring functions, thus offering maximum protection. The other(more routine interlocks) are handled by the PLC. In both cases, the information is always fed to the PLC so that it may be indicated locally or remotely.

The PLC arrangement, both hardware and software, implements the ps operational functions identically as described in section II, above.

Other possibilities or configurations (to figure 4) exist depending on where some of the ps control functions take place. One example is whether the ps local control acts through the PLC or is wired directly within the ps. Other examples are dependent on which choice of control voltage and on the availability of approved PLC modules.

In all cases, the PLC shall be designed to operate in a fail-safe manner. In case of a power failure, the ps shall be turned OFF into a safe state. "Heart-beat" type circuits are standard in current designs and shall be used.

The PLC hardware (currently approved) that shall be used to control any ps is listed in Table 1, which is found at the end of this note. Other modules may be used, but they shall first be approved by the PS Group Leader or the Dept. Chief E.E. The PLC and ps basic approved control voltage is 24 Vdc.

A manual local control and indication panel is shown in figure 4. This is optional and may be replaced by a commercially available PLC plug-in control and indication module (via the PLC serial link). An available (approved) unit is also indicated in Table 1.

The types of ps's that we employ generally fall into two main categories:

1. custom: all controls and interlocks are specified as above, and

2. commercial type: which usually have a minimum amount of controls. These shall be selected, where possible, with a minimum of two relays (contactors) for SBY and ON; and an adequate number of interlock relays or contacts. If not available, these may have to be installed by the ps designer in an interface chassis acting in conjuction with the PLC.

Table 2 lists the names of approved ps commands and status. Figure 5 gives the connector pin identification for the ps to device controller interface.

B. SOFTWARE

Software used in this more modern type ps control scheme resides in two places, namely in the PLC and in the DC (device controller).

The software in the PLC is done in ladder-logic type programming. All the functions defined earlier (see table 2) for the standard AGS ps control are fulfilled. In addition, the various interlock and indication functions are implemented. The final programs usually reside in PROM. The AGS PS Group can provide listings of standard PLC programs.

The software in the DC is written in PL/M and runs under RMX version 4.0 Executive. For further information on the DC programming refer to any DC description or specification of the AGS Controls Group.

IV. ANALOG SIGNALS

The handling of analog signals, both input and output, involves two different schemes. These differ in where the DAC and ADC are physically located and where the signal isolation takes place.

A. DAC/ADC in DC

In this scheme the digital-to-analog and the analog-to-digital converters reside in the device controller and the isolation is at the analog signal level via differential or isolation amplifiers. This scheme has limited isolation and accuracy (< 12 bits). Figure 6 gives the (9 pin D) connector pin identification for the analog reference signal and analog readback signal (i.e. input and output).

B. DAC/ADC in PS

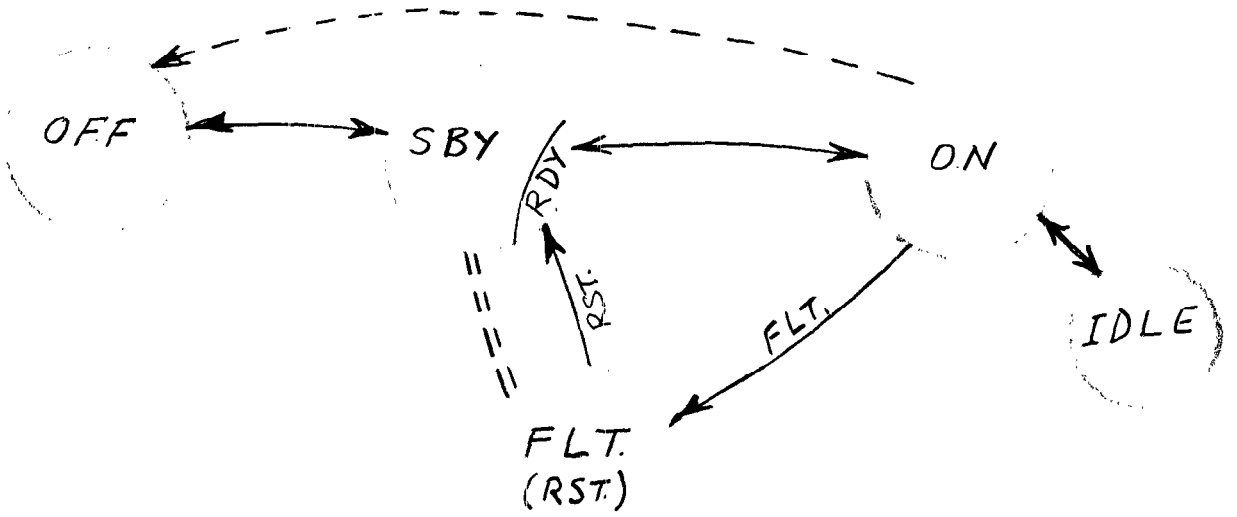
This scheme has the digital-to-analog and the analog-to-digital converters (with or without sample and holds) embedded in the ps. The converters are dedicated to the one ps function. Isolation in this case is done at the digital level via opto-coupler or fiber-optic technology, or at the digital communication level via pulse transformers (e.g. Dcn). In this scheme there is no inherent limitation (up to the current state- of-the-art) on the number of bits or accuracy that may be used.

V. ACKNOWLEDGEMENT

Work in this area was performed by many people in the AGS PS GROUP and in the AGS CONTROLS GROUP. This note is a report summarizing the culmination of many discussions and meetings within both GROUPS.

As changes occur and further items are defined, updates will be issued to this note.

FIGURE 1
AGS PS STATE DIAGRAM



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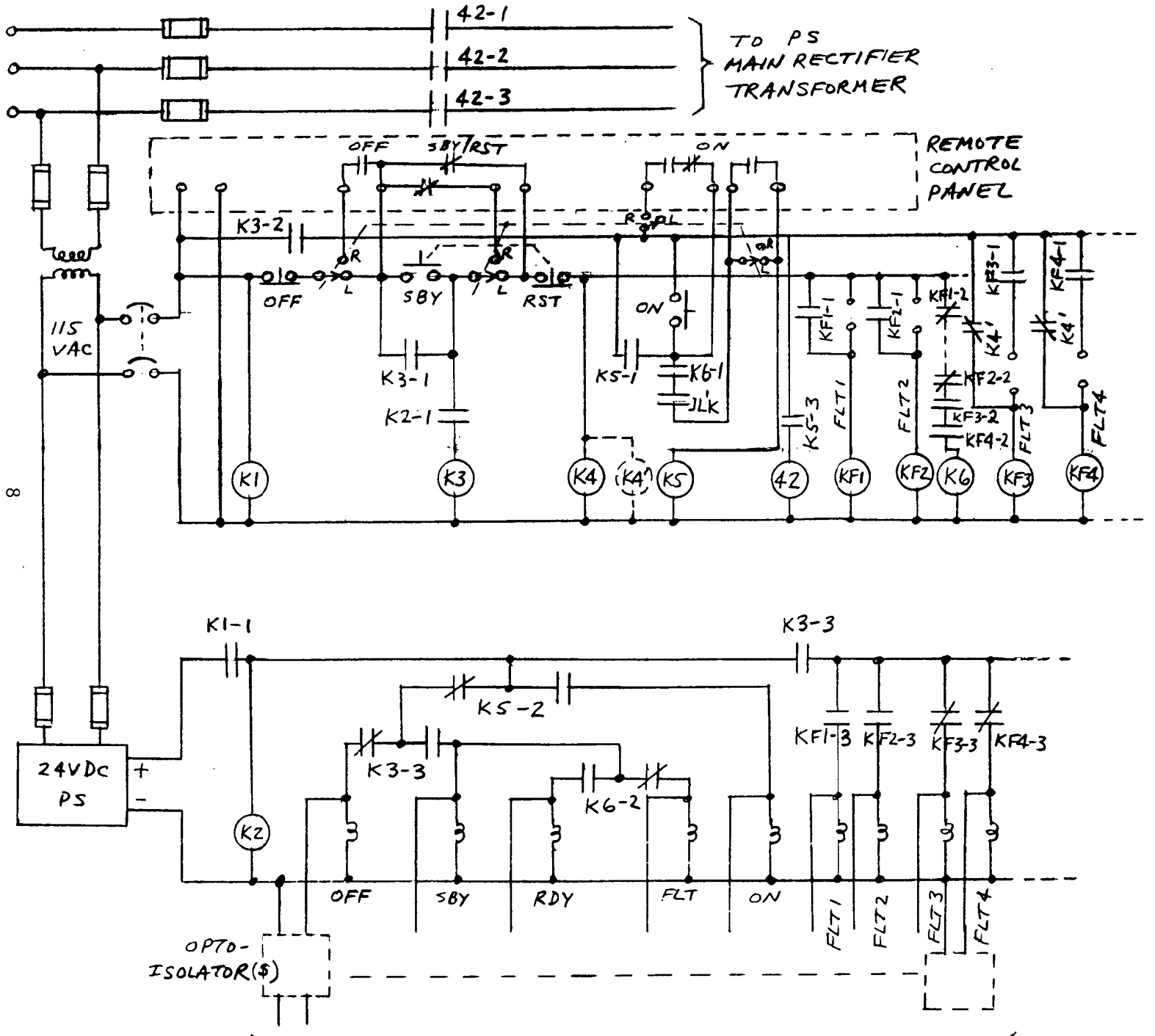
BY RS DATE 1-15-90 SUBJECT PS CONTROL SCHEMATIC SHEET NO. ..... OF .....

CHKD. BY ..... DATE ..... — FIGURE 2 — JOB NO. .....

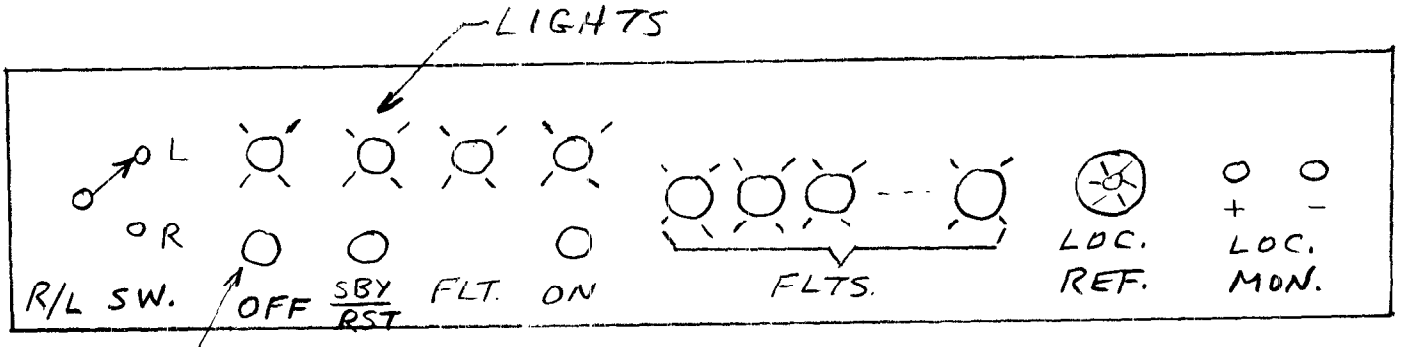
..... DEPT. OR PROJECT .....



SP 116379

FIGURE 3

MECH LAYOUT OF LOCAL CONTROL PANEL



A - TYP. FRONT PANEL LAYOUT

B - CHASSIS & REAR PANEL CONNECTIONS

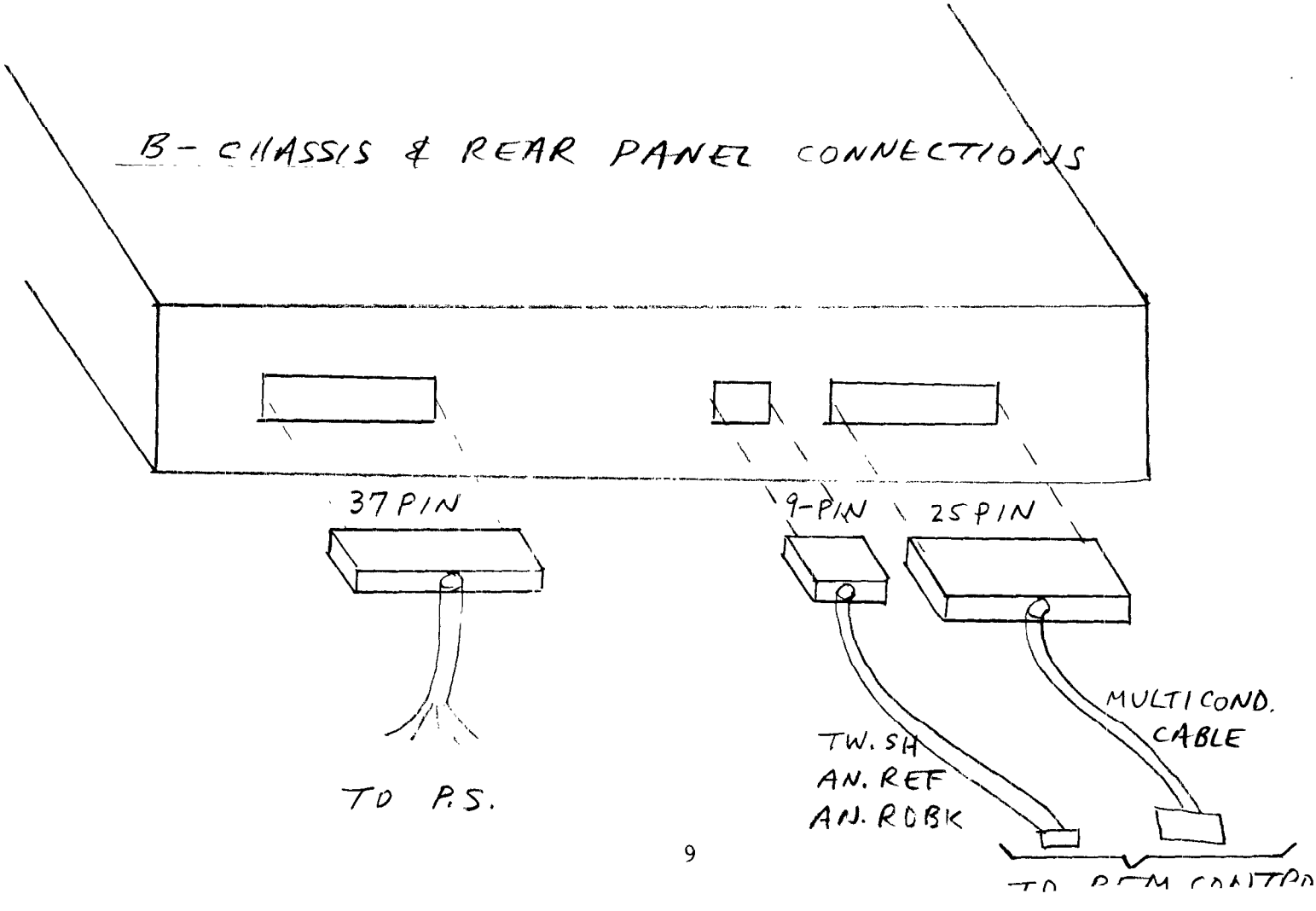
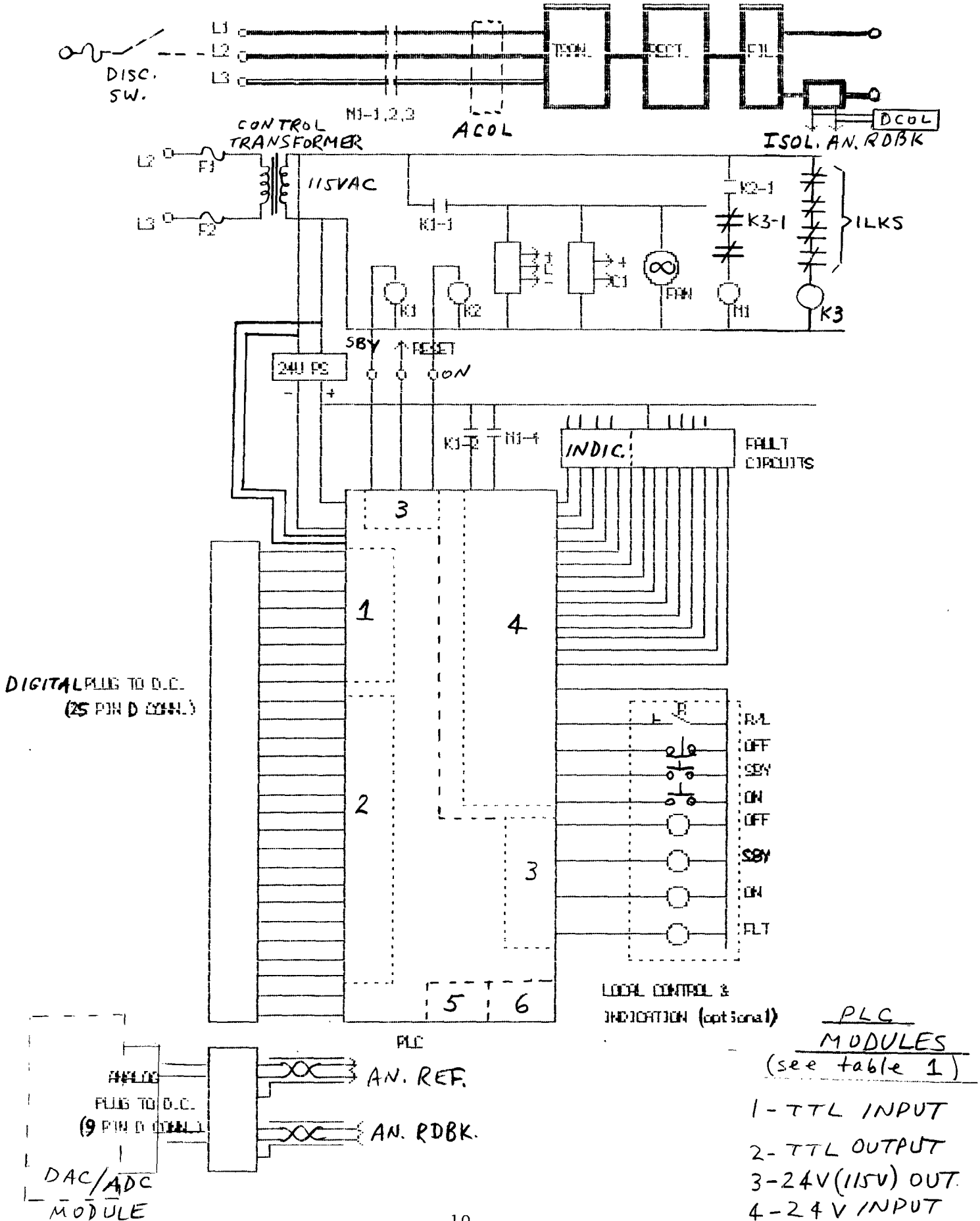


FIGURE 4

PS CONTROL - USE OF PLC



PLC MODULES (see table 1)

1 - TTL INPUT
2 - TTL OUTPUT
3 - 24V (115V) OUT
4 - 24V INPUT
5 - CPU
6 - MPP PS's

1-10-92

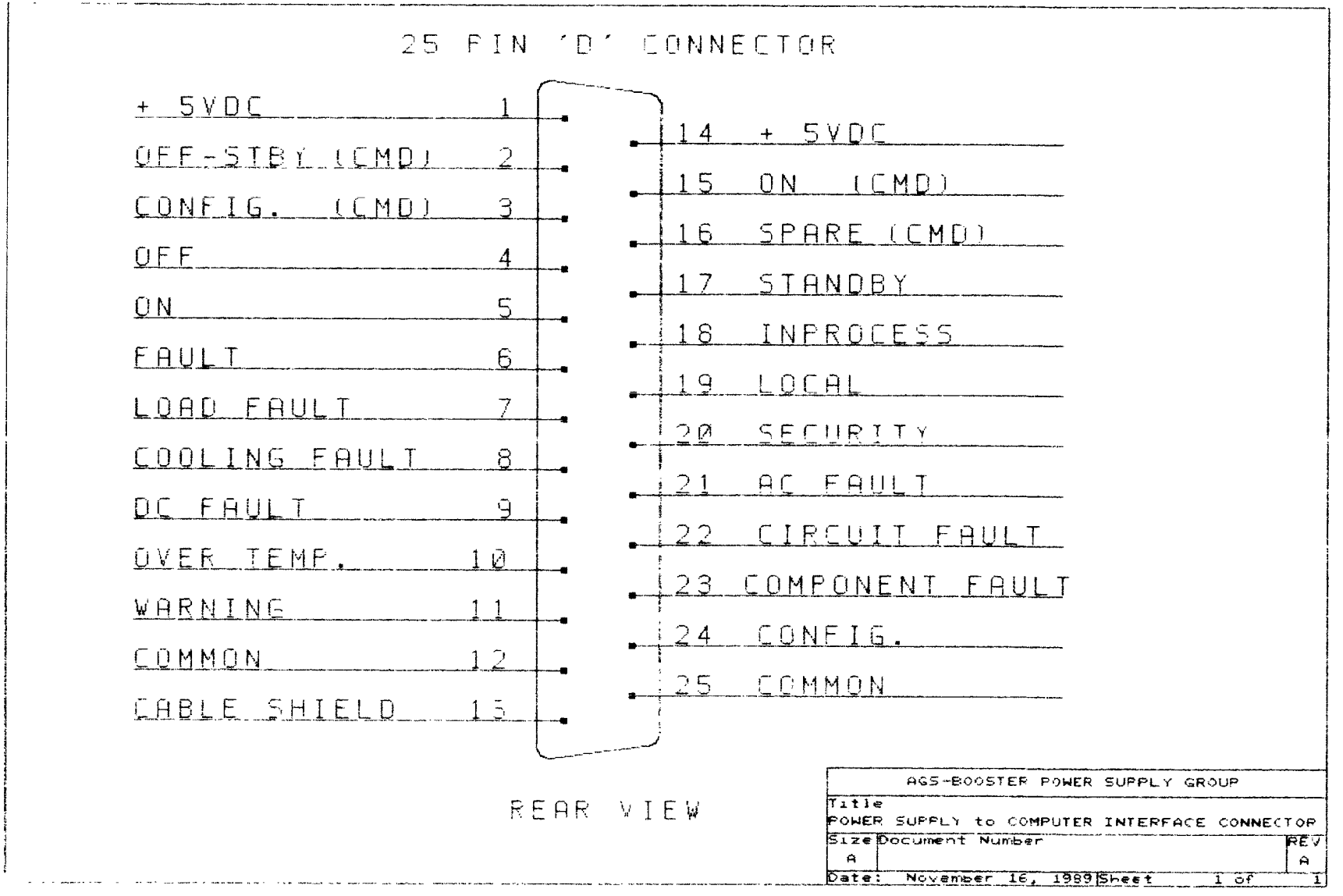


FIGURE 5

P.S. CONTROLS CONNECTION

PIN DEFINITION

FIGURE 6 - PIN IDENTIFICATION FOR ANALOG SIGNAL INTERCONNECTION

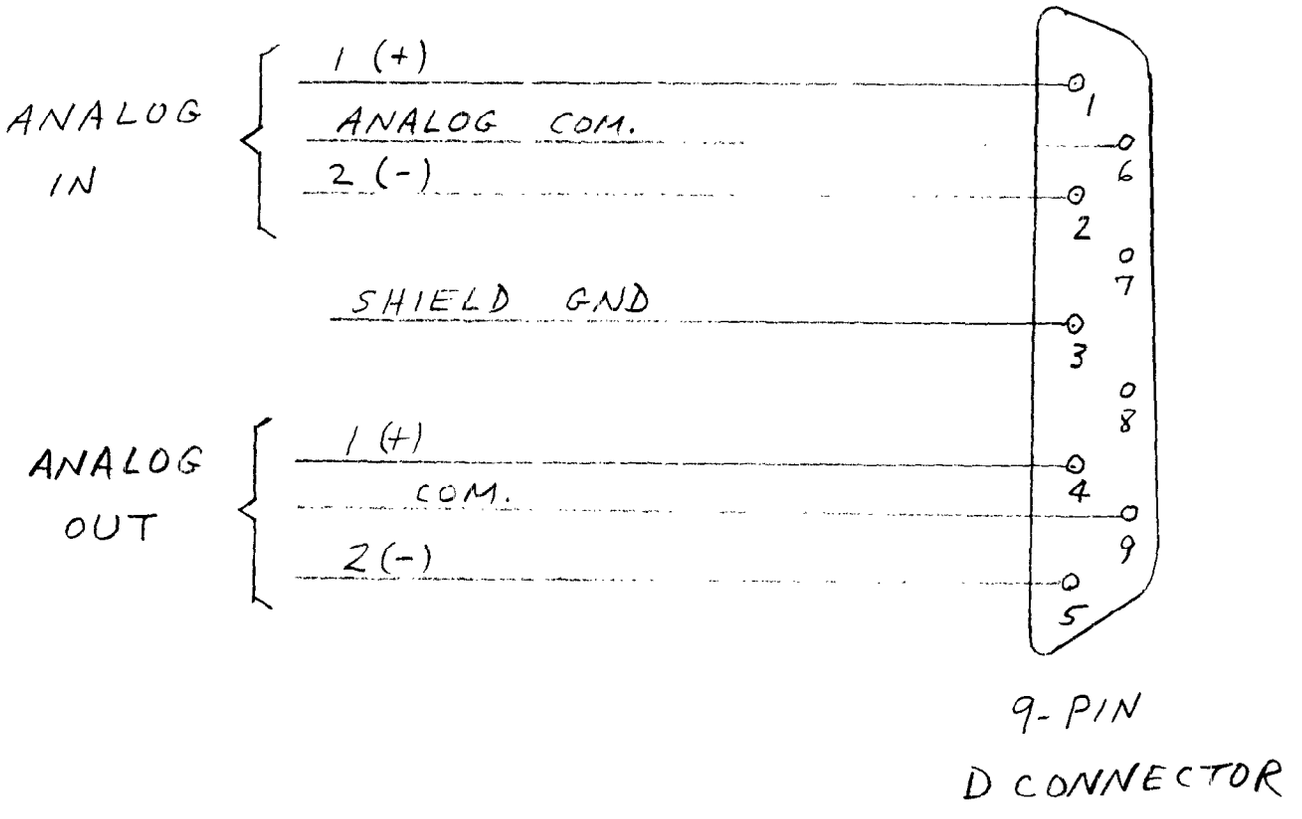


TABLE 1

Current PLC Modules In Use (Approved)

PLC Processor ...PLC2/16	1773-LXP	(5)
TTL 16-Input Module	1771-IGD	(1)
TTL 16-Output Module	1771-OGD	(2)
10-30V 32-Input Module	1771-IBN	(4)
10-30V 32-Output Module	1771-OBN	(3)
Crate, 12-Slot	1771-A3B	
120Vac 6-pt. Isol. Output	1771-ODC	(3)
10-30V 16-pt. Input Module	1771-IBD	(4)
Local Control Module	1784-T30G 1770-T11	

* Model nos. refer to units mfg. by the Allen-Bradley Co.

TABLE 2.

AGS BOOSTER POWER SUPPLY CONTROLS: DEC. 15, 1989

F. TOLDO

STANDARD COMPUTER to POWER SUPPLY INTERFACE CONTROL I/O. FILE:CONTSTAT.WRK

INPUT COMMANDS:	DEFINITION	LOGIC	PIN No.
1. OFF-STBY		OFF=00, STBY=01	2
2. ON		NOT ON=10, ON=11	15
3. CONFIGURATION	PPM, POLARITY		3
4.			16

OUTPUT STATUS:	DEFINITION	LOGIC	PIN No.	CODE	NAME
1. OFF		1= TRUE	4	4B	OFF
2. STANDBY		1= TRUE	17	53	STA
3. ON		1= TRUE	5	6F	ON
4. INPROCESS	TIME DELAYS	1= TRUE	18	70	INP
5. FAULT	NOT READY	1= TRUE	6	64	ITL
6. LOCAL	LOCAL/REMOTE CONTROL	1= TRUE	19	4C	LOC
7. LOAD FAULT	GROUND, OV-TEMP,WATER, VACUUM	1= TRUE	7	73	LOA
8. SECURITY		1= TRUE	20	21	SEC
9. COOLING FAULT	PS AIR, WATER	1= TRUE	8	*	COL
10. AC FAULT	OV-CURRENT,OV-VOLTAGE,FUSES	1= TRUE	21	*	ACF
11. DC FAULT	OV-CURRENT,OV-VOLTAGE, FUSES	1= TRUE	9	*	DCF
12. CIRCUIT FAULT	REGULATOR ERROR,LEVEL,PULSE WIDTH	1= TRUE	22	63	CIR
13. OVER TEMPERATURE	PS OV-TEMPERATURE	1= TRUE	10	68	OVT
14. COMPONENT FAULT	DOORS,TRANSISTORS,SCR,CAPS,TRIG.	1= TRUE	23	45	ELE
15. WARNING	PENDING TRIP,COUNTING CKT	1= TRUE	11	*	WAR
16. CONFIGURATION	PPM, POLARITY	1= TRUE	24	*	CFG

+5 VDC POWER	1
+5 VDC POWER	14
COMMON	12
COMMON	25
CABLE SHIELD	13

ALL OF THE ABOVE INPUT AND OUTPUT CONNECTIONS ARE TTL,
20 mA (MAX) SINK CURRENT AND 1mA (MAX) SOURCE CURRENT.
ALLEN-BRADLEY TTL MODULES: INPUT 1771-IG & IGD, OUTPUT 1771-OG & OGD.