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Gauss Clock Stabilization of the Main Magnet Power Supply

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October 1981

Collider Accelerator Department

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC)

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AGS Division Technical Note

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This note describes the operation and performance of the "new" Gauss clock for the stabilization of the main magnet power supply.

The function of the Gauss clock is to continuously monitor the field in the main ring magnets, and provide control signals to the main magnet power supply to regulate, from pulse-to-pulse, the extraction field in those magnets. The Gauss clock also provides markers, or Gauss clock pulses, approximately every 0.2 Gauss. This feature allows events to be timed directly to specific programmed energies. An example of this would be in the Polarized Proton Program where the pulsing of the correction dipoles will be timed to the energies where depolarizing imperfection resonances exist.

The magnet's electrical parameters over the acceleration cycle are illustrated in Figure 1. At t_0, a low voltage is applied to the magnets to slowly ramp them to injection field which occurs at t_1, about 60 msec later. After injection, the pulsed rectifier bank (P bank) is turned on to increase the voltage to 12,000 volts. This rapidly increases the magnet's field until slightly below the desired current, when at t_2 ($\approx t_0$ + 500 ms) the load is transferred to the flat-top rectifier bank (F bank). This does not occur abruptly, but is programmed down reaching zero in 20 ms. The F bank is variable from bout 500 volts to 1,800 volts. The current is reduced by the F bank until the precise final field is reached at t_4 ($\approx t_2$ + 30 ms). The F bank is then switched to 1,600 volts which matches the IR drop on the resistive portion of the magnet load, and maintains the current at a fixed level.

Figure 2 is the block diagram of the Gauss Clock. The signal input to the system is a search coil mounted in the gap of magnet 242. This magnet is located in the basement of the motor generator building, but is electrically in

series with the main magnets in the ring. The search coil generates approximately 40 volts at the maximum dB/dt. The output leads are hard wired to the voltage-to-frequency converter using twisted-pair shielded wire. All connectors were eliminated to reduce the thermal emf's that are generated by such devices.

The selection of the voltage-to-frequency converter (VFC) was done with much care since the VFC is the primary accuracy determining element. The steps to insure highest accuracy were:

1. A unipolar VFC was chosen. The methods required to accommodate both polarities of input increase the VFC's complexity and add sources of error. Most of the input signal is one polarity and the portion that is not will be handled by an analog integrator.
2. The best available VFC was chosen, and then was modified. The unit chosen is a Dynamic Measurements Corporation Model 7215. This unit is a modified version of their standard Model 8116. The first modification was to eliminate the input buffer amp. This amp which is similar to an LM201 is normally supplied as an interface aid to designers, but taking it out removed all the amplifier's error sources and did not complicate the design.

   The heart of a VFC is an analog integrator. The second modification was to make the output of that integrator externally accessible. The maximum full-scale frequency obtainable in a high precision VFC is 100 KHz, which is the maximum for the 7215. In this application, the peak field is at about 50,000 counts. If the initial starting point of the integrator is random, there will be a one part in 50,000 or 20 ppm peak-to-peak error. This error is eliminated by closing a feedback loop around the integrator. This is referred to as phasing the VFC.

The VFC output pulses are buffered, and they become the Gauss clocks. They are also integrated by two counters. These counters are preset with a number from Datacon. The VFC pulses cause them to count down until zero is reached. At that point, the counters output a pulse. Counter 1, as shown in Figure 2, is loaded with a number representing the B field where the magnets will be transferred from the P bank to the F bank. This transfer is programmed to occur as a quarter cosine wave lasting 20 ms. Just prior to the $\dot{B}$ going negative, Counter 2 switches on the analog integrator. As mentioned previously, the VFC can only handle on input polarity, so the analog integrator is

required to handle this small bipolar portion of the signal. These timing relations are shown in Figure 3.

The energy at t_3 (as determined by Counter 2) is the final energy since t_4 is generated by comparing the analog integrator output to a d.c. reference (set to zero in normal operation) which makes region 1 = region 2 as shown in Figure 3b.

Care was also taken in the design of the analog integrator. Its major features are:

1. The amplifier is chopper stabilized.
2. The integrating capacitor uses a teflon dielectric. The capacitor is thermally biased by a nichrome wire heater to the capacitor's most thermally stable region (> 25°C).
3. The switching is done with D-MOS enhancement FET's. They have low leakage and low gate-to-source capacitance. Even with low capacitance, they are used in a complimentary configuration so that as one gate-to-source capacitor charges, the capacitor on the other discharges.

The output of the integrator plus the $\dot{B}$ signal is summed with an offset voltage and the result servo's the F bank to its proper value. The reason for this servo action is shown in Figure 4. This is an exaggerated view of the magnet current in the time between t_3 and t_4. At t_4 the F bank is programmed to the voltage that just matches the IR drop of the magnets. That change cannot happen any faster than one power supply commutation. Since t_4 is asynchronous to the line, there will be a random amplitude error. This error is a function of the commutation period and the slope. With the single value of F bank control previously used, the error generated is E_1. By having a wide range of F bank controls, the error is approximately as with the two-value case shown.

The worst case accuracy was predicted by using manufacturers' data. Other things to know about this error analysis is:

1. Data for the VFC (7215) was taken from the unmodified version (8116). These were usable for worst case calculations as the 7215 will always perform better in our application than the 8116 would.
2. Scale factor errors must be sorted from offset errors and weighted before adding in with the other errors.
3. Errors will be presented on the basis of a one-hour run. The parameters of change over this run are:
   a) $\Delta t_{amb} = 3°C$
   b) power supply variation = 1%

The predicted results were:

1. VFC

		Offset	Gain
a)	Temp. Coeff.	10.6 ppm	12.8 ppm
b)	Drift	1.2 ppm	1.7 ppm
c)	P.S. Sensitivity	---	1.7 ppm

RMS total for VFC = 16.8 ppm

2. Analog Integrator

a)	Op. Amp.	11.5 ppm
b)	Resistor & Cap.	33.6 ppm
c)	FET Switches	37.7 ppm

3. Weighting

The contribution to the total system error by the analog and digital portions must be weighted by the portion of the total B field that they measure. The integrated poortions were measured as:

K_V = 17.465 volt-sec (VFC)

K_A = 0.035 volt-sec (Analog, Up and Down)

This gives weighting factors:

$$P_V = \frac{17.465}{0.07 + 17.465} = 0.996$$

$$P_A = 1 - 0.996 = 0.004$$

The weighted system RMS error is:

$$E_s = 0.996(16.8) + 0.004(51.8) = 16.94 \text{ ppm}$$

4. Commutation Error

The power supply is a 24-phase system at 60 Hz. This gives a worst-case time ambiguity of:

$$t_{ce} = \frac{1}{60 \times 24} = 0.7 \text{ ms}$$

With the main ring magnets modelled as 0.75 Hy in series with 0.25 Ω, and using 100 volts as the minimum voltage difference to the IR drop, the current change during t_{ce} is:

$$\Delta I = \frac{100V}{0.75H} (0.7 \times 10^{-3}) = 0.093 \text{ amps}$$

ΔI is the variation in current out of a total of about 5,400 amps for a peak-to-peak commutation error of:

$$E_{s\ p-p} = \frac{0.093}{5400} \times 10^6 = 17.3 \text{ ppm}$$

The RMS error is:

$$E_s = \frac{E_{s\ p-p}}{\sqrt{12}} = 5.0 \text{ ppm}$$

The errors were measured on July 6, 1981, using the equipment shown in Figure 5. A direct current-current transformer (DCCT) measured the current in magnet 242. This was compared to a precision d.c. reference by a differential input scope at the time of the start rf off pulse. The gains of the devices were set so that one centimeter of variation on the scope face corresponded to 50 ppm of current change. Figure 6 is the table of data for that measurement. The numbers represent the number of centimeters the trace was from the screen midpoint. This data has been reduced in Figure 7, and shows the RMS errors to be 13.5 ppm.

There are two more points to be noted about this test:

1. The measurement of current using the DCCT does not account for residual fields in the magnet. The Gauss clock also does not, so both devices were measuring the same quantity.
2. Measuring the current at t_4 did not measure commutation errors.

There are still things to be done with the Gauss clock. Some of these are:

1. Using the analog integrator to measure current drift after t_4.
2. Controlling the current in the magnets during "flat-top" (after t_4).
3. Increasing the flexibility of its functions to permit more modes of operation, such as approaching the final current from a lower point, instead of overshooting the final current and settling downward.

But, the analysis has shown and the testing has verified that as a measuring and controlling device, the "new" Gauss clock has the stability to meet the requirements of all the AGS and ISABELLE programs planned.

Distribution: AGS Div. Physicists, AGS Div. E.E.'s, D.A. Davis, J.W Glenn, H. Halama, Y.Y. Lee, E. Raka

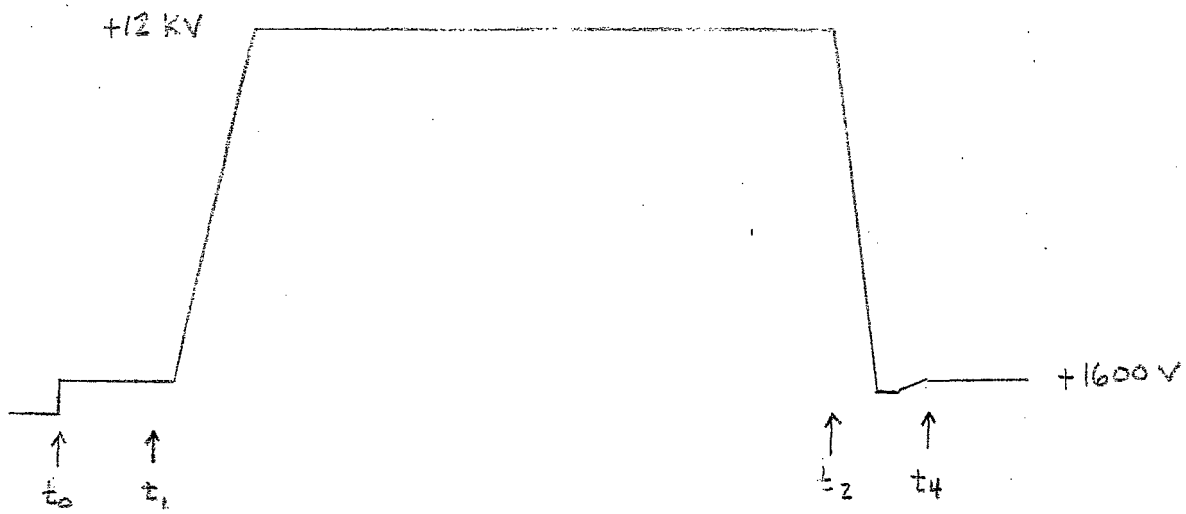


Figure 1a Magnet Voltage

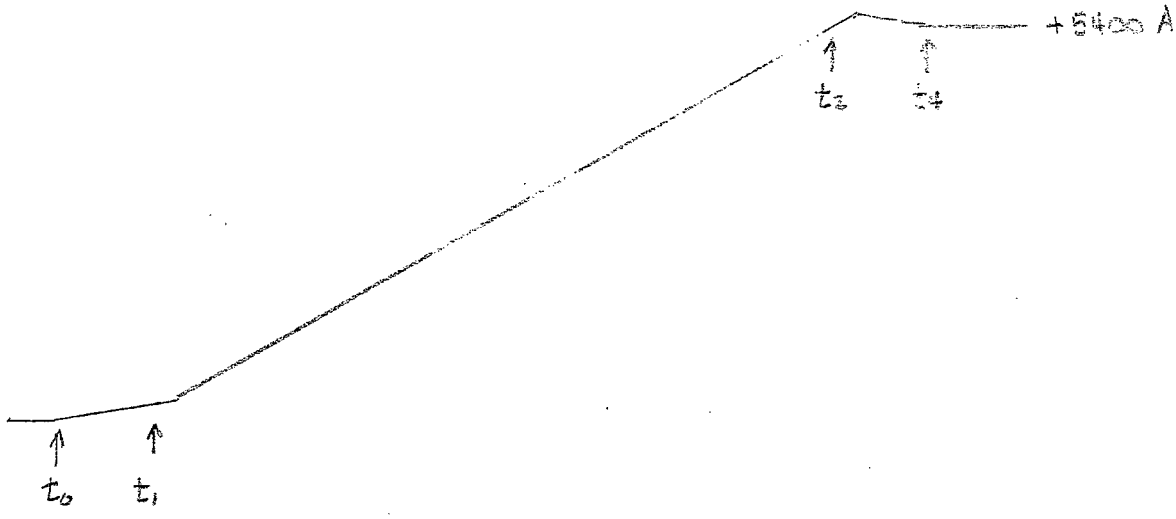


Figure 1b Magnet Current

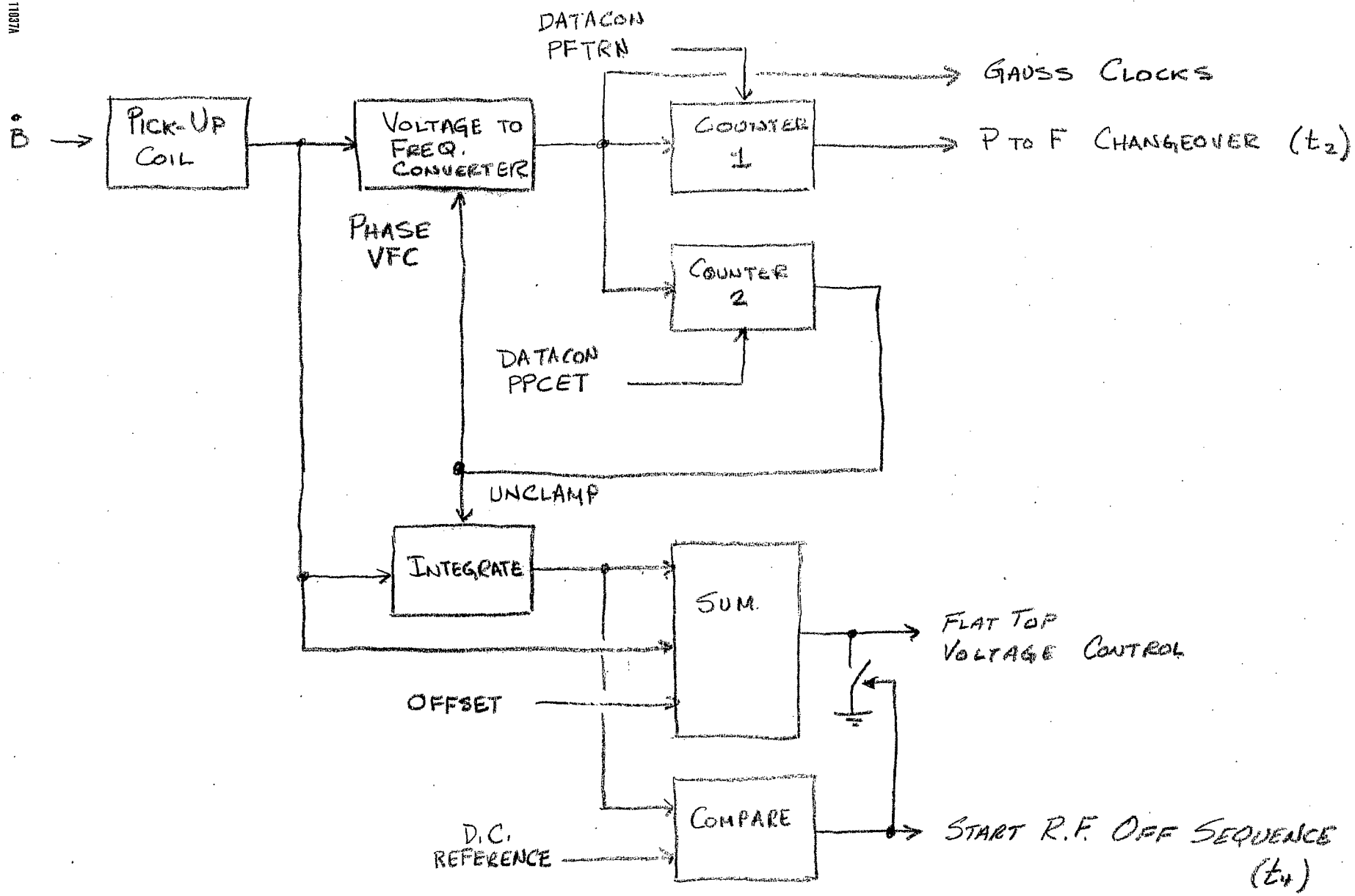
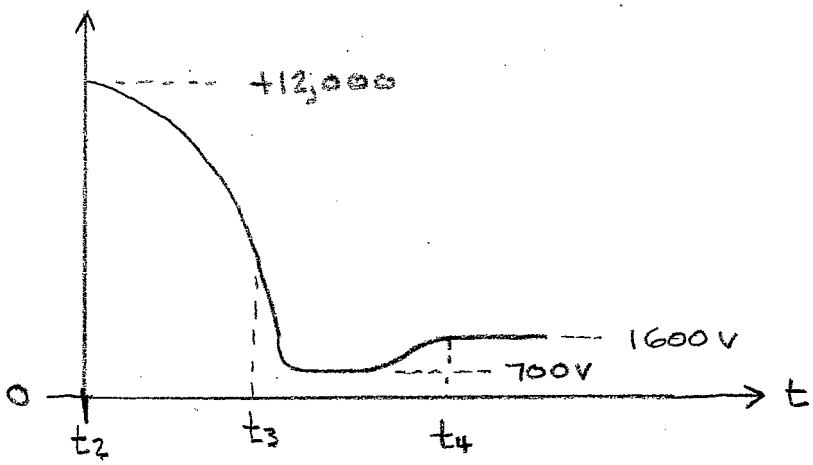
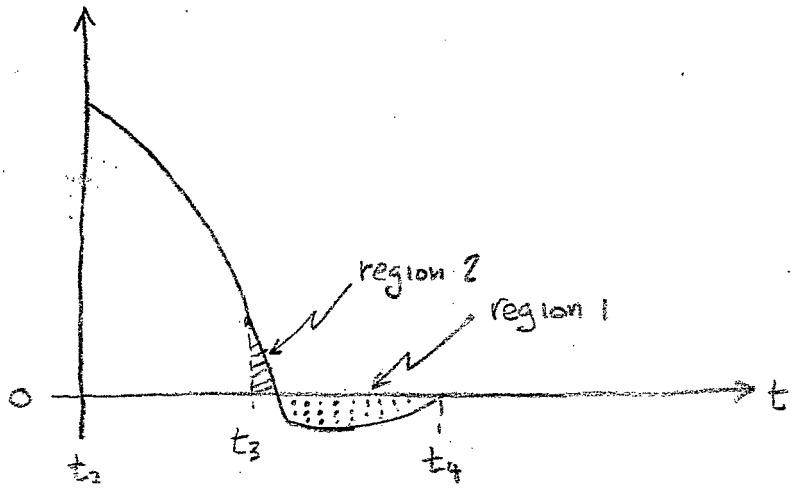


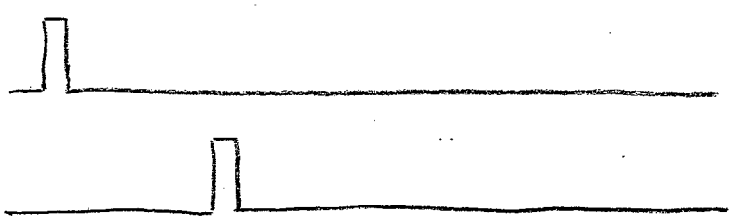
FIGURE 2. GAUSS CLOCK BLOCK DIAGRAM.



3a - Magnet Voltage (not to scale)

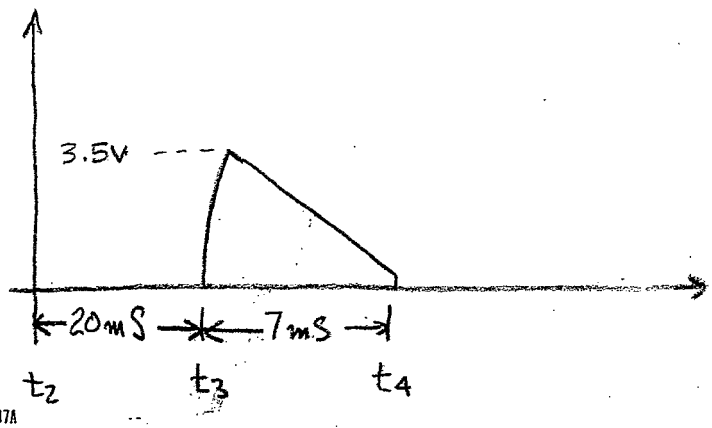


3b - $\dot{B}$ (not to scale)



3c. - Counter 1 Output

3d - Counter 2 Output



3e. - Analog Integrator (not to scale)

SP 11037A

FIGURE 3. TRANSFER TIMING

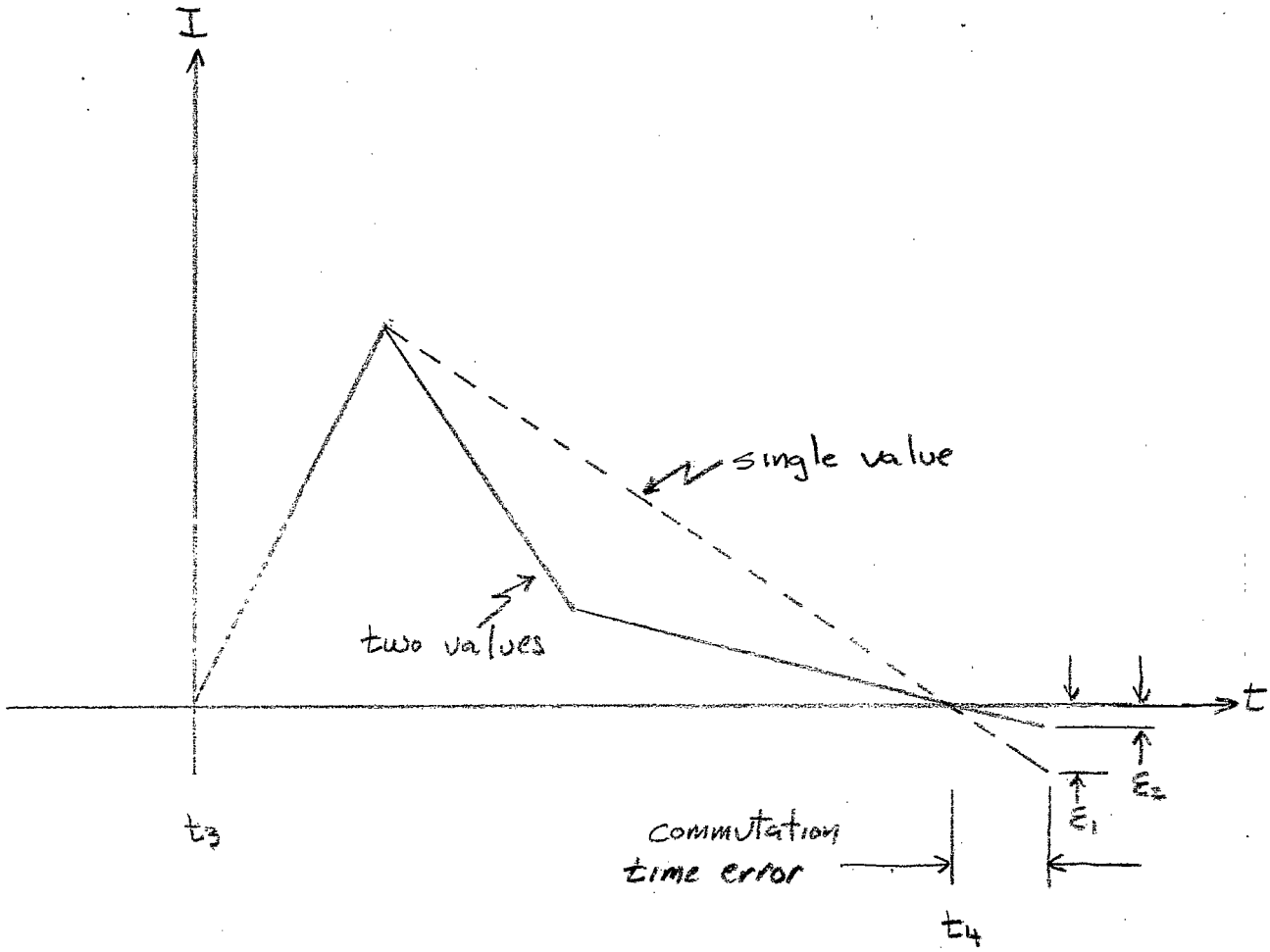


FIGURE 4. COMMUTATION ERRORS

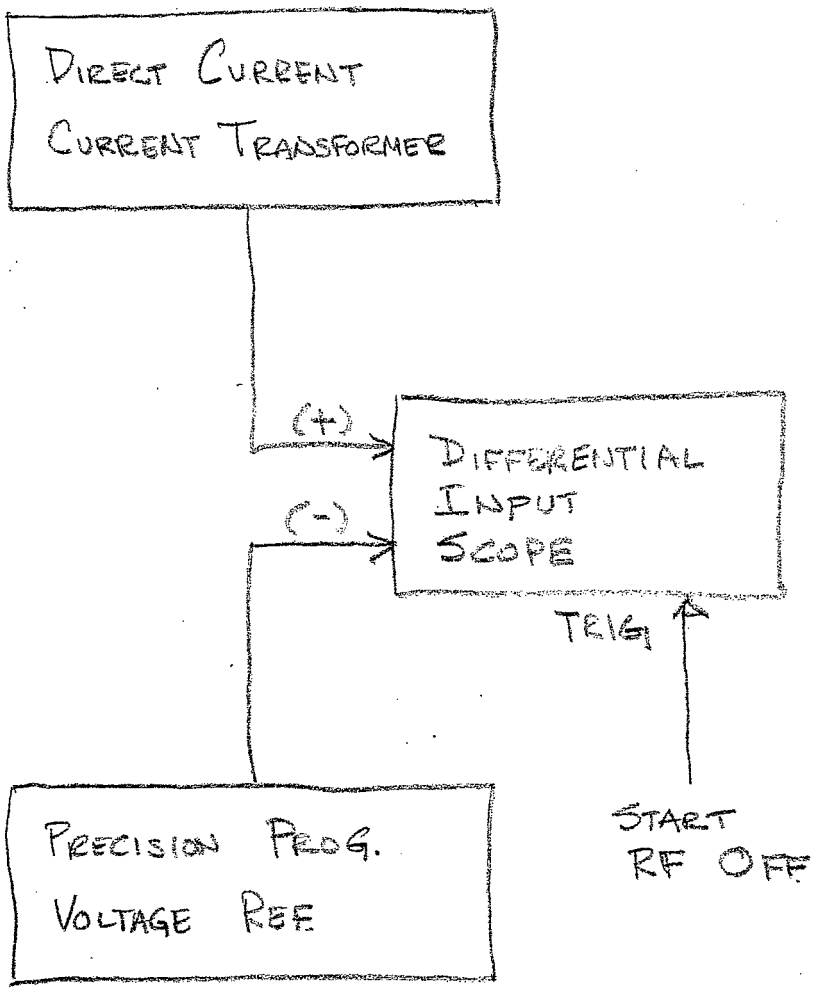


FIGURE 5 - TEST CONFIGURATION

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FIGURE 6. TEST DATA

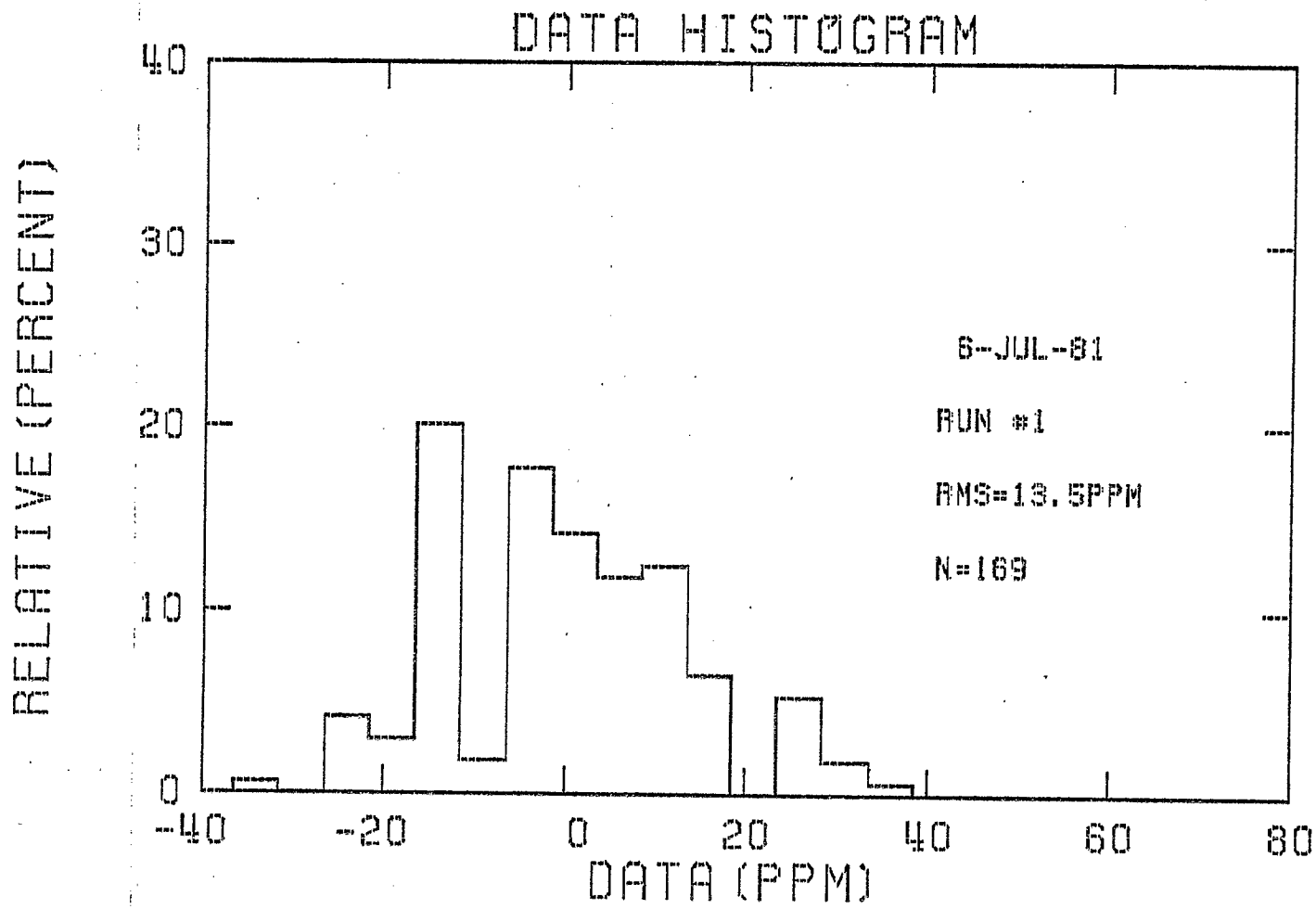

FIGURE 7. REDUCED DATA.