BNL-229756-2026-TECH

Testing the Common Platform LLRF with a 197 MHz NCRF Cavity

S. Mai

May 2026

Electron-Ion Collider

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC), Nuclear Physics (NP)

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S. Mai[1], R. Bachimanchi[2], K. Fahey[1], J. Latshaw[2], K. Mernick[1], M. McCooey[1], G. Narayan[1], T. Plawski[2], J. Settle[2], F. Severino[1], and A. Singh[1]

[1]Brookhaven National Laboratory, New York
[2]Thomas Jefferson National Accelerator Facility, Virginia

Abstract

The Common Platform is the hardware that will support the new LLRF platform to be used for the Electron-Ion Collider. The Common Platform features a carrier board that is used to interface with a variety of daughter for different applications. This paper details the testing that was done using the Common Platform and an RF Digitizer Daugther Board. Firstly, the firmware and software development is discussed followed by a description of the controls algorithms used in the testing. Then, testing and verification of the platform with a 197 MHz NCRF cavity is discussed. The paper concludes with results from the testing and the path forward.

1 Introduction

The Electron-Ion Collider (EIC) is the next generation particle accelerator being built at BNL. It is going to use an existing RHIC tunnel for the hadron storage ring and repurpose the second ring for the electron storage ring. The accelerator complex at RHIC contains many integrated systems including Low-level RF Controls, Controls, Cryo, Vacuum, etc. All of these systems will be upgraded to meet the mission statement of EIC. The EIC LLRF system has been designed and is in its prototyping and testing phase. It uses the Common Platform as the main cavity field controller. The Common Platform is a FPGA-based carrier with 2 slots for pluggable daughtercards. The standardized daughtercards designs include Digital IO, Baseband ADC, RF Digitizer, and SFP boards. The RF Digitizer specifically will be used to digitize cavity signals, and drive the high-power amplifiers and cavities. With RHIC operations concluding in April 2026, 2 weeks of dedicated testing of the Common Platform LLRF was performed on a RHIC 197 MHz cavity. The test provides a valuable opportunity to validate LLRF designs on a real cavity before RHIC shutdown.

2 Firmware Development

DESY Firmware Framework (FWFWK) and GitHub were used to support RF Digitizer firmware development. DESY FWFWK helps keep the firmware project organized, compact, and modular by using Make and TCL scripts to recreate projects. The TCL scripts are used to add sources to the project, recreate block diagrams, and generate/configure Xilinx IPs. GitHub is used to provide version control and easy collaboration between multiple contributors. Git submodules also allow for code reuse

between multiple projects.

Fig. 1 shows the top level firmware block diagram of the carrier and RF Digitizer. An AXI Chip2Chip interface is instantiated on both the carrier and daughtercard. This interface is the primary communication path between the carrier and daughter. It includes an AXI4 bus for transferring blocks of data, and a slower AXI-Lite bus for daughtercard register access.

There are 2 MicroBlazes instantiated in the block design. The first MicroBlaze is dedicated to housekeeping, initializations, and debugging. SPI is used to optimize timing on the ADC and DAC chips. I2C is used to periodically monitor voltage, current, and temperature. UART provides some debugging functionality in the software. The second MicroBlaze is dedicated for the tuning loop. It reads back the cavity and forward phases to calculate detuning and update the tuner position. Since the Digitizer board is not able control the tuner directly, it sends a command through the Update Link to a RHIC Motor Controller daughtercard to update the tuner position.

The RHIC Update Link (UL) is a 2 Gbps fiber link that provides timing events and data packets to all downstream receivers. The UL receiver was ported over to the RF Digitizer to allow synchronization of frequency tuning words with the RHIC system. The RF Digitizer is able to transmit a 16-bit address and 16-bit data word to the Update Link Master, which then redistributes that information to all downstream receivers. This transmission of tuning loop commands allows the RF Digitizer to indirectly control the tuner via a RHIC Motor Control daughtercard.

Fig. 2 shows the field controller module. It includes the ADC and DAC interface, ADC processing blocks, and control algorithms. The ADC interface deserializes the digitized ADC data, and applies fine and coarse timing adjustments of the ADC data stream. Next, the raw ADC data gets IQ demodulated to get IQ data. The IQ data is low-passed to filter out the upper sideband. A CORDIC block is used to calculate the magnitude and phase of the signal.

The IQ data is subtracted from the reference to get the error term for the control algorithms. The resulting feedback correction is added to a feedforward term for seamless opening and closing of feedback loops without introducing large transients. The data gets scaled, IQ modulated, then finally serialized to the DAC.

3 Software Development

3.1 EPICS and PscDrv

The RF Digitizer daughtercard is controlled by data written to its memory by the Common Platform Carrier. The carrier responds to packets sent to it by a remote EPICS IOC, which specifies the address and data of the register. These packets are formatted using the Portable Streaming Controller (PscDrv) specification, which is a lightweight TCP packet specification [1]. This allows for minimal overhead on the carrier, as well as straightforward IOC updates.

3.2 DesyRDL

The registers that the PscDrv packets control are defined by DesyRDL, a register mapping package provided in FWFWK [2]. With DesyRDL, registers can be defined, and an address is defined that persists across workflows. A set of EPICS PVs can be created from this set of addresses, and so a PscDrv packet can be used to instruct the Common Platform Carrier to write to and read from the proper registers in the daughtercard, without needing to know what board was installed with which firmware version.

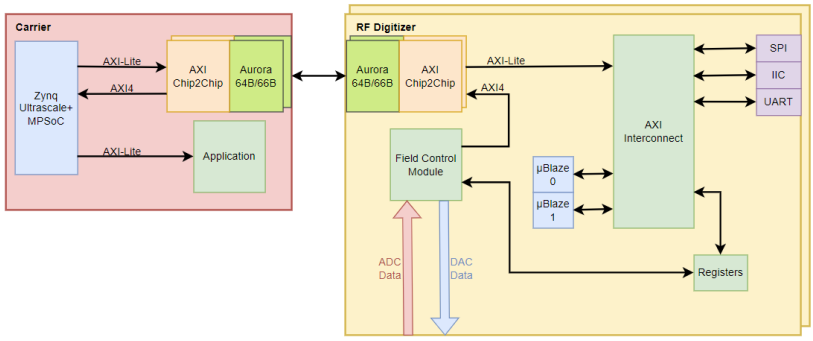

Figure 1: Diagram shows the top level firmware diagram between the carrier and RF Digitizer Daughtercard

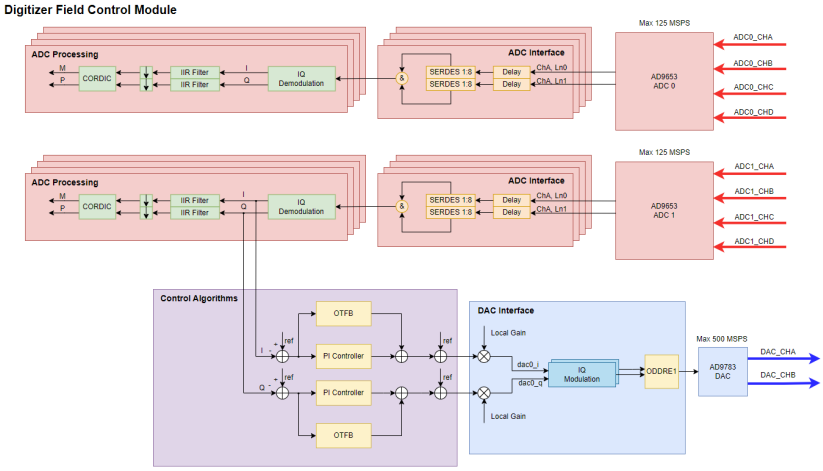

Figure 2: Figure shows the Field Control Module for the RF Digitizer.

3.3 Phoebus

A user interface was created in CS-Studio Phoebus to control the digitizer, mapping register states to buttons and text input boxes. Logging was also set up, where configuration parameters and readbacks were visible through Phoebus's Data Browser tool. The EPICS parameters were monitored and logged for the entirety of the time testing was done in the RHIC tunnel.

4 Algorithms

4.1 Field Control Loop

The cavity field control is done through IQ feedback using a proportional-integral (PI) controller. A derivative term was not needed for this testing but it can be added in the future. The magnitude and phase reference is set on the EPICS GUI and gets converted to I/Q reference values. Before the feedback loop can be turned on, the residual errors must be set to 0 by adjusting the ADC scaling and NCO phase. The firmware also features a rotation matrix at the end of the processing chain which can be adjusted to apply any phase corrections. There

Figure 3: Figure shows Phoebus UI for the RF Digitizer, while testing was underway

is an option to add the reference at the output of the field controller block, this prevents any large transients when the loop is closed.

4.2 Tuning Loop

The tuning loop is a software algorithm implemented on a Microblaze, it is responsible for maintaining proper detuning of the cavity. The implementation is based on the tuning loop algorithm used for RHIC. The tuning loop operates in 2 modes, position mode and phase mode.

Position mode is used primarily to ensure a cavity is at the correct frequency prior to applying voltage. For example, in RHIC, the 28 MHz cavities are used to capture and accelerate the beam while the 197 MHz cavities are only used during store. The position mode algorithm would ensure the 197 MHz cavities are at the correct frequency to ensure optimal detuning is achieved once voltage is applied to them. On the other hand, phase mode is used once there is voltage on the cavity. The phase mode algorithm compares the phase between the forward and cavity probe signals and adjusts the tuner to maintain the setpoint. Of course, there is additional logic to ensure proper checks and constraints on the tuning loop. For example, the loop should not try and move the tuner beyond some specified bounds. The code also uses a polynomial function to convert the tuner position read back to a frequency, the coefficients are determined empirically.

5 Testing and Verification

The EIC Common Platform LLRF system was tested on a RHIC 197 MHz cavity. The test includes verifying the Common Platform carrier, RF digitizer boards, analog front end, and EPICS functionality. The Digitizer board has 2 DACs: one for LO reference and one for generating the up-converter IF. The LO reference is used by the LO Generator chassis to generate 2x, 3x, and 4x harmonics of the reference. The analog front end also filters and mixes the IF and RF signals.

For the initial test, the RHIC LLRF platform was used to regulate the cavity field while the RF Digitizer read copies of the cavity, forward and reflected power. This verified the ADC in-

terface, processing, and read-back registers. It also verified that the Digitizer is able to receive the frequency tuning word from the Update Link. This test was also used to calibrate the ADC scaling on the Common Platform setup.

Next, the RF Digitizer was used to drive the cavity with the IQ loop closed. The DAC drives the LO generator and upconverter to create the 197 MHz cavity drive. When the cavity pickup signal comes back to the LLRF system, it gets downconverted and digitized by the board. The Digitizer field control module processes the ADC data for the control algorithms and regulates the cavity field.

Finally, the tuning loop was tested to provide resonance control of the cavity. The Digitizer calculates and transmits the tuner position command to the Update Link, where it redistributes it to a RHIC Motor Control board that sets the tuner position.

6 Results

Cavity testing took place over 2 weeks in March 2026 at various operating conditions. The cavity voltage was brought up to 500 kV. The digital IQ and tuning loop ran uninterrupted for over 48 hours before testing concluded. Phase noise and field stability of the cavity pickup were also measured.

6.1 Noise Results

Phase noise measurements were taken at various voltage levels on the cavity. Figure 4 shows a phase noise measurement of the cavity pickup at 100 kV compared to previous measurements of the same cavity controlled by older hardware. As can be seen, the integrated jitter from 1 Hz to 10 kHz was reduced from ~ 309 fs to ~ 118 fs. One thing worth noting is the phase noise above 100 kHz. The dip in the orange trace is due to the cutoff frequency of the direct analog feedback which has a bandwidth of around 200 kHz. This cutoff is not seen in the blue trace but this is due to the noise floor of the measurement. The signals monitored by the common platform setup were -20 dB copies that were later amplified. Thus the noise floor of the measurement prevents the cutoff (of the direct analog feedback) from being seen.

6.2 Field Stability

RMS phase and amplitude stability for the new LLRF system was calculated using logged data pulled from legacy controls systems. These numbers were compared to previous cavity stability numbers of the same cavity being controlled by legacy RHIC LLRF systems. Table 1 shows the RMS voltage and phase stability comparison between the legacy RHIC hardware and new LLRF system. The bandwidth of these measurements is determined by the bandwidth of the monitoring port, which is the same for both measurements. As is shown in Table 1, amplitude stability is slightly worse using the new system, while phase stability is better.

Table 1: RMS Voltage and Phase Comparison

Stability	**RHIC LLRF**	**New LLRF**
Voltage (%)	0.0034	0.0048
Phase (°)	0.0118	0.0073

7 Path Forward and Conclusion

Testing with a RHIC 197 MHz cavity was essential for validating core LLRF capabilities with the EIC Common Platform setup. With this testing, we were able to demonstrate functional hardware, software, firmware, and algorithms. While the exact implementation details for each of these components may change going forward, this testing demonstrates that critical pieces of the LLRF platform are integrated correctly.

References

1. Davidsaver M. The PSC Driver. `https://mdavidsaver.github.io/pscdrv/`. 2021.
2. Büchler M and Butkowski L. DesyRDL. `https://fpgafw.pages.desy.de/docs-pub/desyrdl/main/index.html`. 2026.

Appendix A: Cavity Phase Noise Measurements

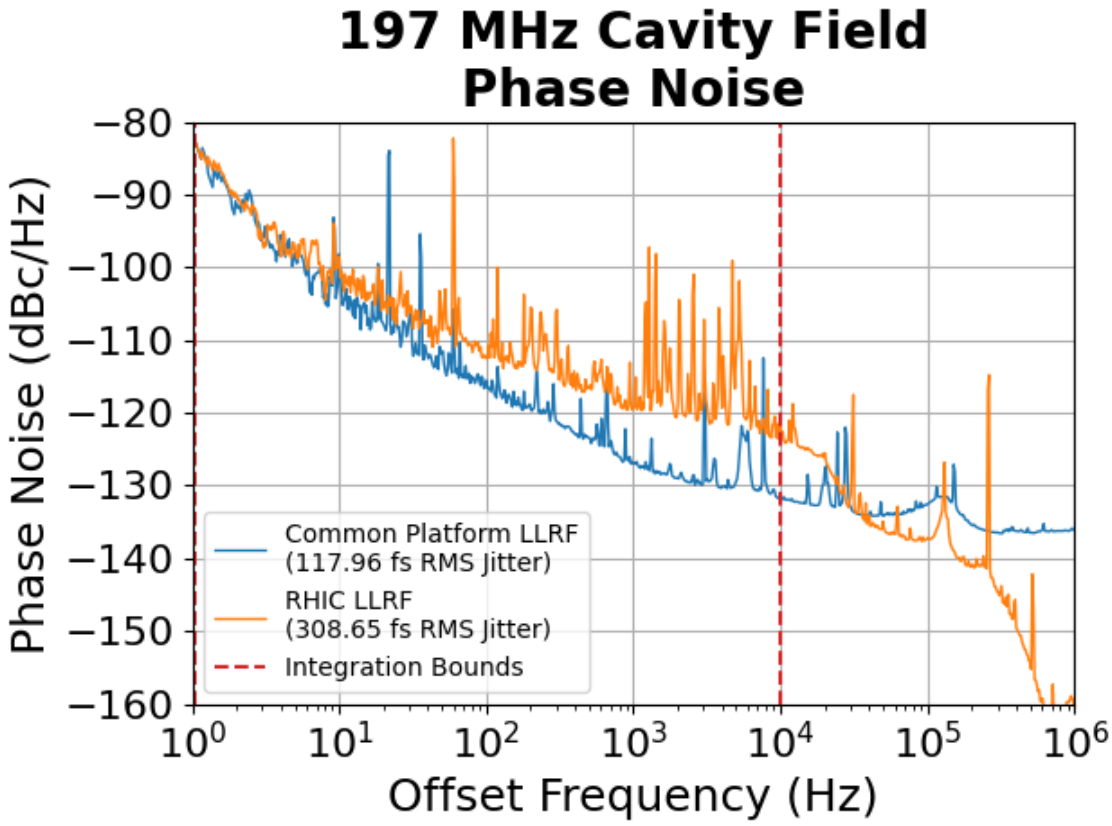

Figure 4: Cavity Pickup Phase Noise; Common Platform Controller (Blue) vs. Legacy Cavity Controller (Orange)