BNL-229755-2026-TECH

RF DIGITIZER FOR EIC LLRF

S. Mai

May 2026

Electron-Ion Collider

Brookhaven National Laboratory

U.S. Department of Energy

USDOE Office of Science (SC), Nuclear Physics (NP)

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RF DIGITIZER FOR EIC LLRF*

Samson Mai[1†], Ramakrishna Bachimanchi[2], Kyle A. Fahey[1], Kevin Mernick[1], Arshdeep Singh[1]
[1]Brookhaven National Laboratory, Upton, NY, USA
[2]Thomas Jefferson National Accelerator Facility, Newport News, VA, USA

Abstract

With the shutdown of Relativisitc Heavy Ion Collider (RHIC) in FY26, the former RHIC facility will be upgraded to the new Electron-Ion Collider (EIC). An RF Digitizer for the EIC LLRF system has been developed and tested on a RHIC 197 MHz cavity in Q2 2026 for a baseline performance. Firmware and software has been developed and validated during the 197 MHz cavity test. Preliminary data from the cavity test shows phase noise performance significantly better than the RHIC LLRF system.

INTRODUCTION

With the RHIC shutdown in 2026, RHIC will be removed and repurposed for EIC. The existing LLRF systems at BNL will be mostly replaced by the Common Platform. The Common Platform is a modular 2U chassis with a carrier and 2 pluggable daughtercards. The RF Digitizer daughtercard was designed and developed to be integrated with the Common Platform carrier. Three prototype boards were procured to allow for parallel testing at JLAB and BNL.

HARDWARE

The RF Digitizer board shown in Fig. 1 has been developed at JLAB in collaboration with BNL. Its design is based on existing designs at LCLS-II [1], JLAB [2], and BNL [3]. The Digitizer board has 8 ADC channels and 2 DAC channels. Layout for the revision of a 4 ADC channel, 4 DAC channel board is done. The new board also includes minor revisions to allow for more debugging flexibility.

The Digitizer board contains an Artix UltraScale+ FPGA, on-board oscillator, LMK04808B PLL, and ethernet for stand-alone testing. It has 2 edge connectors to interface with the Common Platform carrier. The edge connectors allow for up to 7 transceiver lanes for communication with the carrier. It also receives power, PLL clocks, and other miscellaneous signals from the carrier. The carrier provides a 400 MHz clock for the DAC and a 100 MHz clock for the ADCs.

The Digitizer board has 3 main tasks: digitizing the IF signal from the downconverter, generating IF signal for the upconverter, and generating signal for the local oscillator (LO) reference. Initial tests were performed to test these functionalities, along with measuring isolation, noise floor and phase noise.

* This work was supported by the EIC Project and the U.S. Department of Energy, Contract DE-SC0012704.
† smai@bnl.gov

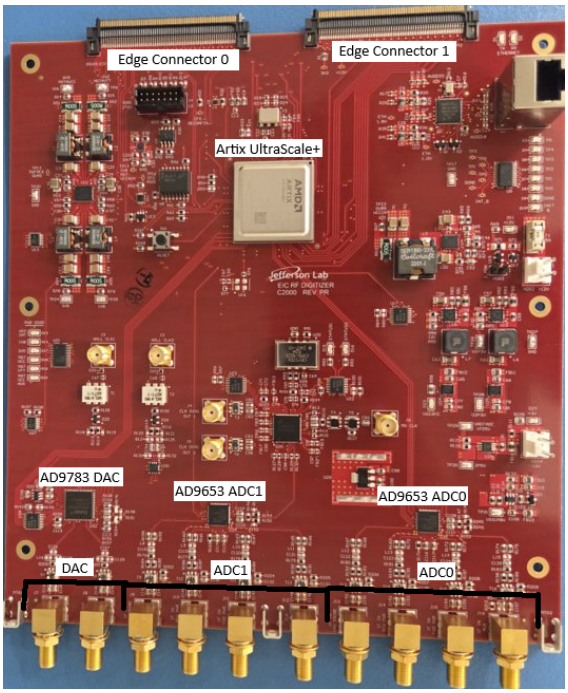

Figure 1: Picture of the RF Digitizer prototype board. It includes 2 edge connectors to the carrier, a Xilinx Artix UltraScale+ FPGA, 1 AD9783 DAC chip, and 2 AD9653 ADC chips.

FIRMWARE ARCHITECTURE

The top-level firmware architecture of the RF Digitizer is shown in Fig. 2. The Chip2Chip interface between the carrier and daughtercard uses an Aurora 64B/66B and AXI Chip2Chip block. The Aurora 64B/66B acts as the physical layer that instantiates a 10 Gbps transceiver lane on the edge connector. The AXI Chip2Chip block creates an AXI4 and AXI-Lite interface between the carrier and daughtercard. The AXI-Lite bus allows the EPICS GUI to read and write registers on the RF Digitizer. The AXI4 bus allows for a high throughput bus protocol from the Digitizer to carrier DDR4 memory. Registers are auto-generated in VHDL using DESYRDL [4]. The test application includes ADC/DAC interfaces, data acquisition, and field controller blocks.

EPICS Communication

Experimental Physics and Industrial Control System (EPICS) is an open-source software used for control systems. It will be used for EIC, replacing the proprietary Accelerator Device Object (ADO)-based RHIC control system. The carrier software uses a Portable Streaming Controller (PSC) driver to encode and interpret Ethernet packets [5]. The

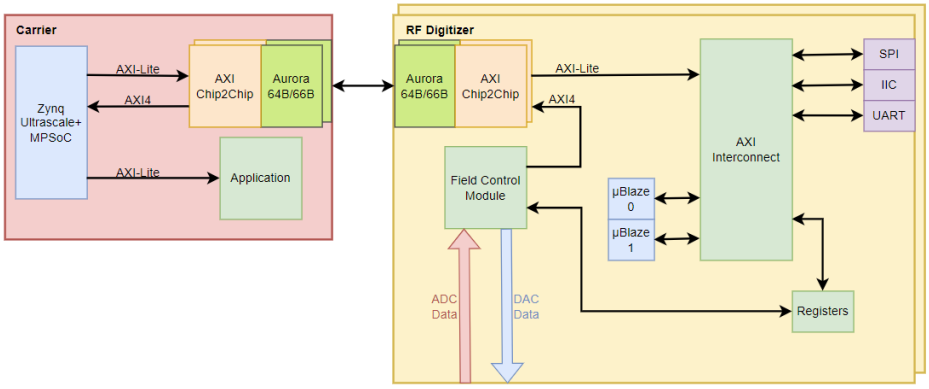

Figure 2: Diagram shows the top level firmware diagram between the carrier and RF Digitizer Daughtercard

packets can initiate AXI-Lite read and writes to the daughtercard registers through the AXI Chip2Chip link. On the daughter side, AXI Burst writes can be initiated using an AXI DataMover Xilinx IP. The streaming data gets mapped to DDR4 memory on the carrier, which will get read by the IOC.

Test Application block

The field control module shown in Fig. 3 contains primarily the ADC/DAC interfaces, ADC processing and field controller blocks. The 2 Gbps RHIC Update Link [6] was also ported over to the RF Digitizer specifically for the 197 MHz cavity test. The Update Link Receiver is necessary to synchronize to the RHIC system's resets and frequency tuning words. The Digitizer can also transmit to the Update Link through a dedicated transceiver lane to the carrier SFP TX. The Digitizer transmits tuning commands to a RHIC Motor Controller daughtercard, allowing the cavity to stay on resonance.

ADC Interface Each AD9653 ADC channel provides 2 serial data lanes to the FPGA, each at 800 Mbps. The ADC also provides a 400 MHz data clock, allowing us to deserialize the data stream with DDR mode. We use a Xilinx Input delay block to perform fine timing shifts of the data. This deskewing helps us sample in the center of the data window. Temperature drifts are compensated for using the Xilinx IDELAYCTRL block.

ADC Processing After the Analog signal is digitized, IQ demodulation converts the raw ADC signal to in-phase and quadrature components. The IQ signals are passed through a low-pass filter to filter out the upper side-bands. Next, a CORDIC block is used to convert IQ to magnitude and phase.

Field Controller The field controller block is used to regulate field stability. Before turning on control loops, the ADC data should be calibrated for gain and phase. The IQ error terms are calculated and fed into the Proportional-Integrator (PI) and One-Turn Feed Back (OTFB) control loops. These control loops have been tested in previous RHIC experiments with beam [7]. The field controller has the option to have the feedforward drive term on, in combination with the error feedback term. This allows for seamless closing and opening of the loop without introducing huge transients that can trip the cavity. The field controller block also includes an IQ window comparator that shuts down RF if the feedback error term grows too large for a certain amount of time.

DAC Interface Lastly, we have a DAC interface for the AD9783. The final output is multiplied with a local gain, IQ modulated, and gated by faults. IQ modulation turns IQ data back into a real signal and sent out in parallel to the DAC. Since the AD9783 DAC samples at DDR, a Xilinx ODDRE1 primitive is needed to combine the two DAC channels for double data rate sampling. Finally, faults gate the DAC output to shut off power to high power and prevent damage to personnel or equipment. Faults include fast fault, IQ window comparator fault, and high-level fault.

SOFTWARE

The Digitizer contains 2 MicroBlazes, each providing dedicated functionalities. The first MicroBlaze provides housekeeping, initializations, and serial communication access. The second MicroBlaze is dedicated to the tuning loop.

Serial Communication Drivers

The first MicroBlaze is used to access the SPI, I2C, and UART communication protocols. SPI is used to initialize both the AD9653 ADCs and AD9783 DAC. The ADC chip is programmed to output a test pattern for initial timing calibrations. Similarly, the DAC has its own timing optimization procedure accessible through its SPI registers. I2C is used to monitor voltage, current, and temperature on the LTC2991 chip. Finally, UART is used for general debugging purposes.

Tuning Loop

The second MicroBlaze is used for calculating the tuner position using the cavity and forward phase. The tuner com-

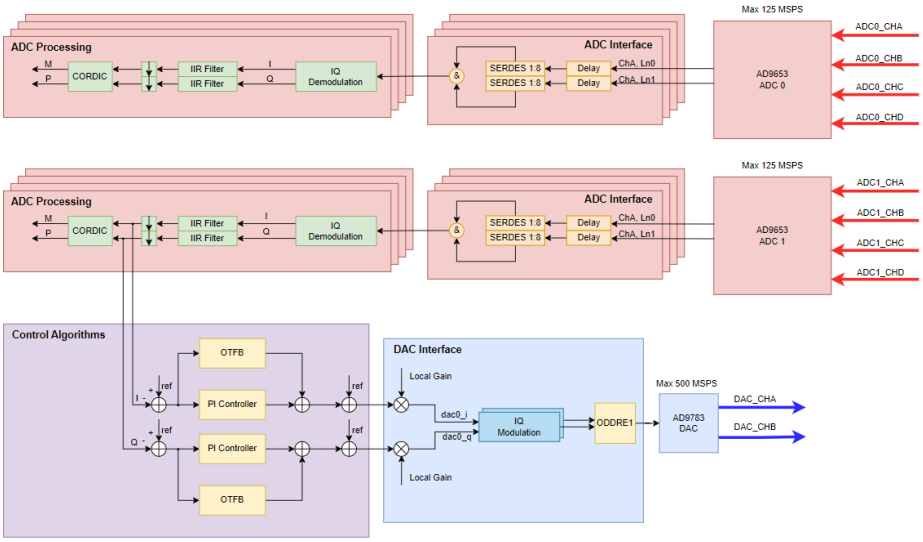

Figure 3: Figure shows the Field Control Module for the RF Digitizer.

mand is sent through the carrier, to the Update Link, where the RHIC Motor Controller board decodes the Update Link command and sets the tuner position.

TESTING

Initial hardware tests occurred in the RF lab to test isolation of ADCs and DACs, phase noise, and noise floor. Next, the Digitizer board was tested on a RHIC 197 MHz cavity at Bldg. 1004. The Digitizer board provides IF and LO reference to the 197 MHz upconverter. Similarly, the cavity voltage, forward and reflected power are downconverted to IF for digitizing. The Update Link master provides a fiber to the Common Platform carrier. Testing was done in several stages to allow us to adequately test each aspect of what we wanted to test, and it makes debugging easier.

Hardware Adjacent DAC and ADC channels were measured for isolation. With one DAC channel at full-scale output, the adjacent channel was measured on the spectrum analyzer to calculate the isolation. For the ADC isolation, a -1 dBFS signal was connected to the ADC while adjacent channels were measured for isolation. The processing was done in Python to calculate the logarithmic ratio between the adjacent channels and the driven channel.

Phase noise was measured on both the DAC and upconverter output. The noise floor was measured by recording ADC data on a terminated channel, and the power spectral density was calculated using Welch's method.

Monitoring The first test involves driving the cavity with the existing LLRF system, and monitoring the cavity signals on the Digitizer board. We tested the new EPICS snapshot waveform, and verified the ADC readbacks on the EPICS GUI. This test also allowed us to calibrate the cavity voltage readings using the existing system.

Driving the cavity Next, the cavity was driven in open and closed PI loop from the new LLRF system. The cavity voltage's phase and gain were calibrated to the RF drive reference before closing the loop. Phase noise measurements were taken of the cavity pickup. Phase and magnitude data were logged. The cavity ran for over 48 hours without tripping.

Tuning Loop The tuning loop was tested in closed loop mode with the PI controller. No major differences were observed in the cavity readings compared to the old tuning loop.

RESULTS

DAC crosstalk as a function of frequency is shown in Fig. 4. ADC isolation was calculated to be better than 80 dB for each ADC channel. ADC noise floor was measured to be better than -150 dBFS/Hz. Table 1 shows the RMS voltage and phase comparison between the RHIC and new LLRF system. Fig. 5 shows the cavity pickup phase noise plot. RMS jitter is better on the new Common Platform (117.96 fs) compared to the RHIC LLRF system (308.65 fs).

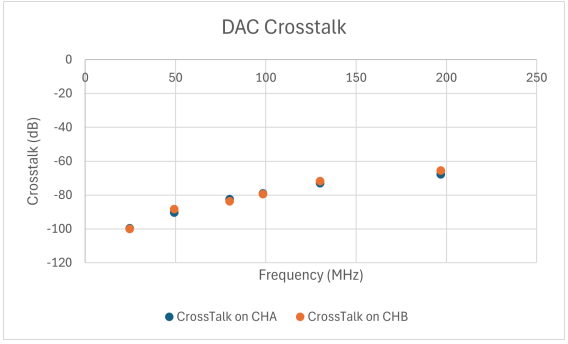

Figure 4: Plot shows DAC crosstalk on Channels A and B. Frequency was swept from 24.6 MHz to 197 MHz.

Table 1: RMS Voltage and Phase Comparison

Stability	RHIC LLRF System	New LLRF System
Voltage (%)	0.0034	0.0048
Phase (°)	0.0118	0.0073

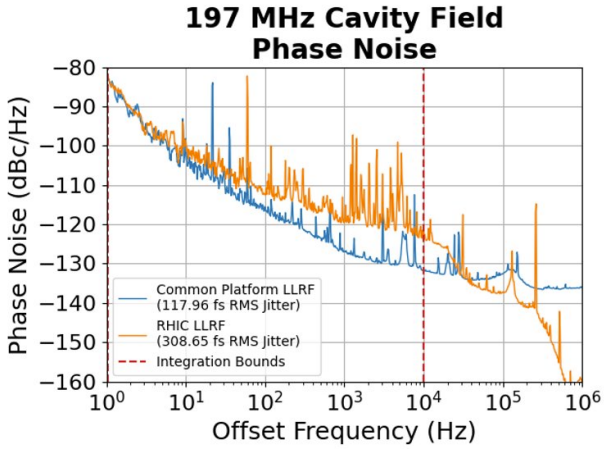

Figure 5: Plot shows phase noise measurements of RHIC LLRF system vs Common Platform LLRF system. RMS jitter calculations integrate from 1 Hz to 10 kHz.

CONCLUSION

Significant work has been done on the Digitizer hardware, firmware, and software. The Digitizer has been tested on a RHIC operational cavity. Preliminary results show similar or better performance when compared to the existing RHIC LLRF system.

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