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ELECTRON STORAGE RING POWER SUPPLY SYSTEM DESIGN REPORT

Z. Zapata

April 2026

Electron-Ion Collider Project

Brookhaven National Laboratory

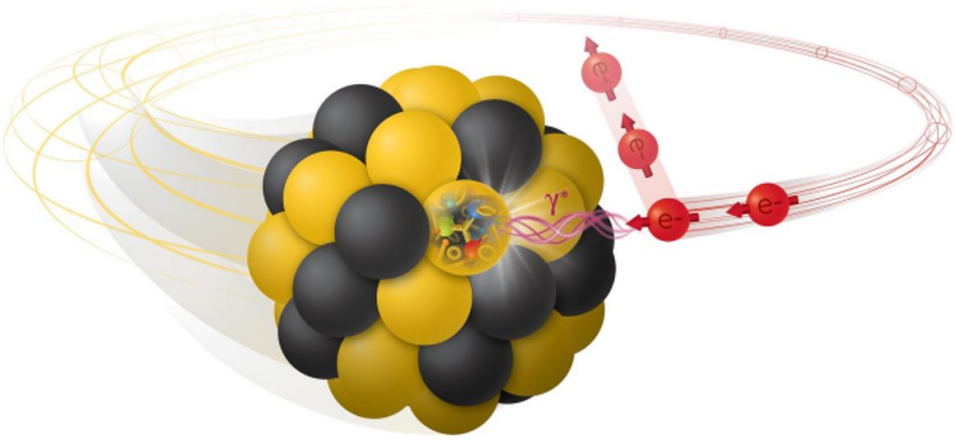
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1 Introduction

In January 2020, U.S. Secretary of Energy Dan Brouillette announced the decision to build an Electron Ion Collider (EIC) at Brookhaven National Laboratory (BNL). While advancing the state of the art of particle colliders, the EIC will enable the U.S. nuclear physics community, with world-wide participation, to take a giant step forward in the centuries-old quest to understand the nature of matter at its most fundamental level, providing the clearest picture yet of how the elemental quarks and gluons interact to form the basic structure of atoms and nuclei. The EIC at Brookhaven National Laboratory will be the first particle accelerator capable of colliding polarized ions with polarized electrons.

The EIC will require advanced design of a magnet power supply system to achieve the established science requirements. The Electron Storage Ring (ESR) is part of the EIC and has a unique power supply system. This document is one of several prepared to define the technical basis of the full ESR power supply system and meet EIC project requirements.

1.1 EIC Overview

The EIC is an advanced machine that will require two different storage rings – one for electrons and another for hadrons, to facilitate the collision of the particles. In total, the EIC will consist of four major systems.

- Hadron Storage Ring (HSR)
- Electron Storage Ring (ESR)
- Electron Injection System (EIN)
- Interaction Region 6 (IR 6)

The EIN will feature a Rapid Cycling Synchrotron (RCS), which will be a fast-ramped machine designed to bring the electrons up to energy for injection into the ESR. The HSR and ESR will reuse infrastructure from the Relativistic Heavy Ion Collider (RHIC). The injection system for the hadrons will also make use of the existing infrastructure present at BNL and will consist of a polarized ion source, booster ring, and Alternating Gradient Synchrotron (AGS). IR 6, also known as ePIC, will be designed for collision detection and research.

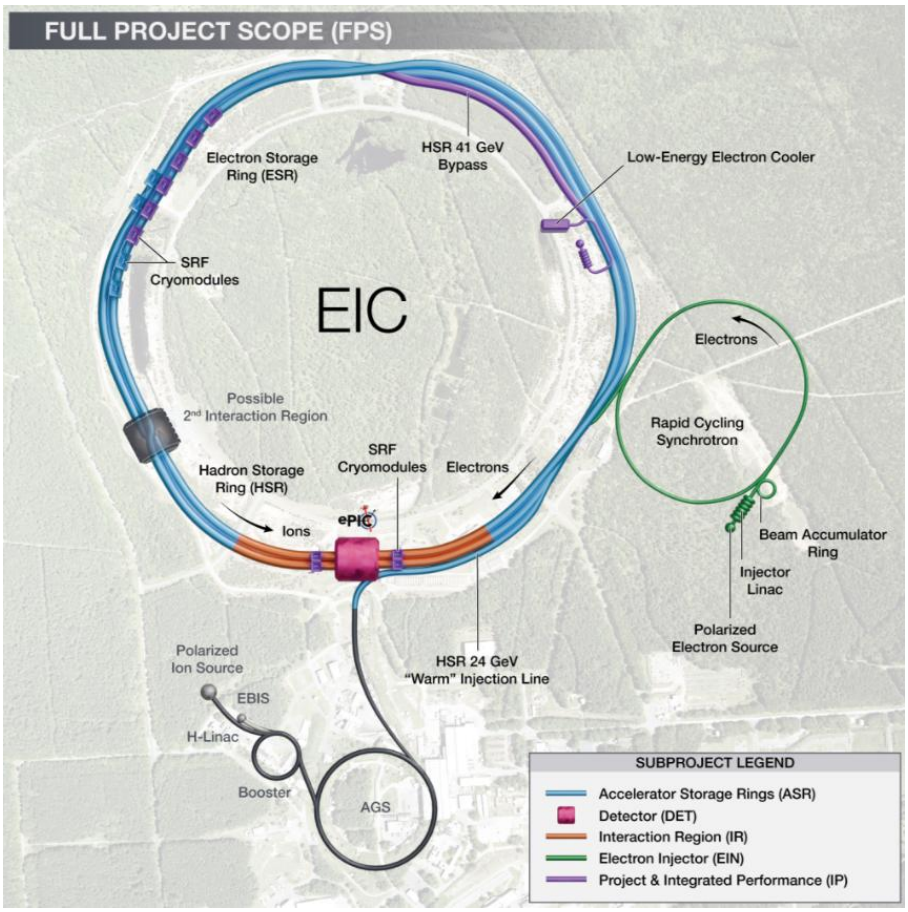


Figure 1. EIC Full Project Scope

1.2 ESR Power Supply System

The ESR power supply system will feature one main dipole magnet series string. The dipole magnet designs have built-in trim coils, which are grouped into separate series strings. Also, there will be both individually powered and series string quadrupole and sextupole magnets. Lastly, there will be individually powered corrector magnets throughout the ring for both horizontal and vertical plane corrections. The corrector magnet designs are consistent throughout the ring, except for in IR6, which will feature unique large aperture corrector magnets.

Due to the high-power requirement of the main dipole circuit, three custom-built power supplies will be used to power the entire string. Additionally, in cases where the voltage and/or current requirement is higher than available Commercial-Off-The-Shelf (COTS) units, the COTS supplies are connected in series and/or parallel circuits to achieve the higher voltage and/or current, respectively. The main dipole, dipole trim, quadrupole, and sextupole power supplies will operate in single quadrant and therefore will be purchased/built as unipolar supplies. The correctors must operate in four quadrants and therefore require a bipolar solution. Since some of the dipole trim magnets are required to operate at very low currents, they will also require a bipolar solution to achieve the required precision. The bipolar solutions are designed in-house as Build-to-Print (BTP) solutions.

Table 1. ESR Power Supply System Summary (Includes IR 6)

Magnet Type	Number of Magnets	Number of Powered Circuits	Number of Power Supplies
Horizontal Corrector	221	221	111 2CH BTP
Vertical Corrector	222	222	111 2CH BTP
Quadrupole	464	291	574 COTS
Sextupole	309	81	121 COTS
Trim Dipole	747	34	24 COTS & 6 4CH BTP
Main Dipole	747	1	3 CUSTOM
Total	**2710**	**850**	**719 COTS** **228 BTP** **3 CUSTOM**

The EIC power supply group's deliverables include the power supplies, racks, associated auxiliary equipment, and cables. Power supplies can be categorized as custom (the main dipole), COTS (all quadrupoles, all sextupoles, and most dipole trims), and Bipolar BTP (all correctors and some dipole trims)

1.3 ESR Main Dipole Power Supply Overview

Detailed descriptions of the main dipole power supply design, control strategies, and performance validation are provided in Section 4.1.

1.4 ESR COTS Power Supply Overview

For the ESR magnets, all the quadrupoles and sextupoles, and most of the dipole trims, will be powered by COTS unipolar power converters. These power supplies can interface with BTP designs for controls and interface hardware and have undergone testing to meet the ESR performance requirements.

The COTS power supplies are selected based on their availability, reliability, and high-power density. The required precision current regulation is achieved through interfacing with COTS Direct-Current-Current-Transducers (DCCTs) the BTP Power Supply Controller (PSC). The COTS supplies are operated in voltage mode, and the highly accurate current feedback from the DCCT is passed on to the current loop within the PSC. In cases where individual COTS units cannot meet the required voltage or current, multiple power supplies are combined in series and/or parallel configurations to achieve the desired operating range. When series/parallel configurations are used, a Multi-Channel Power Converter Interface Card (MCPCIC)—a BTP solution—is used for setpoint distribution and current sharing. AC power is distributed to all equipment in the rack with both COTS and BTP Power Distribution Units (PDUs).

The COTS-based approach also supports a wide range of ESR operating conditions, including varying magnet configurations and energy modes, without requiring custom hardware for each

application. This reduces system complexity and facilitates maintenance, spare management, and future upgrades.

Detailed descriptions of the COTS power supply configurations, control strategies, and performance validation are provided in Section 4.2.

1.5 ESR Bipolar Power Converter Overview

The ESR corrector magnets require a bipolar power converter (BPC), so the magnets can provide field corrections in a positive and negative direction in their respective planes. The BPC solution will operate as a four-quadrant power converter and provide both positive and negative voltage and current to the corrector magnets.

The National Synchrotron Light Source II (NSLS-II) electrical engineering group has designed BTP solutions for the Advanced Light Source Upgrade (ALS-U) project. These converters are tried and tested designs and are in use at both NSLS-II and ALS-U projects. The EIC power supply group has leveraged off the proven designs from the NSLS-II team and made modifications to existing designs to meet EIC needs. Additionally, the EIC power supply group will upgrade the existing convert designs based on lessons learned from production testing.

The ESR physics team is requiring very low operating currents (<300mA) for some of the dipole trim coils. To meet the required precision at these low currents, another BTP solution is designed. This unit will be a small 4-channel device located in each new service building. Therefore, each building will have enough available channels for trim coils permanently running at these low currents, as well as spare channels to cover cases where higher current trim coils switch to low current operation at different energy levels.

Detailed descriptions of the bipolar power supply designs, control strategies, and performance validation are provided in Section 4.3.

2 ESR Power Supply Requirements

The ESR will store electrons at three different energy levels defined in Giga-Electron Volts (GeV). The energy levels are 5 GeV, 10 GeV, and 18 GeV. The EIC project has defined physics requirements into early science and full science. Early science refers to operations at 5 and 10 GeV, while full science refers to operations at 18 GeV. To ensure longevity of the ESR power supplies, requirements at full science are considered, so future upgrades or redesigns will not be needed. The requirements for all ESR power supplies are documented in an official record of decision (ROD), EIC-ROD-044.

2.1 Ripple and Stability

To understand the ripple and stability requirements provided by physics, the terms need to be precisely defined.

- **Stability** – Very slow movement over time and/or movement in response to environmental conditions such as temperature or humidity (comparable to noise at a very low frequency)
- **Ripple** – unwanted periodic AC fluctuations superimposed on DC output (typically an expected frequency, from switching components or an artifact of device configuration)
- **Resolution** – precision; how small of a change is detectable and representable as a distinct digital value

The ripple requirements must be met by the power supplies and measured under test conditions that reflect full science operation. Stability can be achieved by interfacing with the PSC. The BTP PSC—also a tried and tested design from NSLS-II—can interface directly with all ESR power supply types.

2.1.1 Science Requirements

The science requirements for the ESR power supplies are defined in the following table for both early and full science. The maximum allowable values are defined as parts per million (ppm) of the root-mean-square (RMS) current in relation to the power supplies maximum operating current.

Table 2. ESR Power Supply Science Requirements

Full Science Requirements					
Magnet	Ripple up to 1kHz (ppm rms)	Ripple >1kHz (ppm rms)	Ripple 1kHz-8kHz (ppm rms)	Ripple 8kHz-40kHz (ppm rms)	Long Term Drift (1s – 10 hours) (ppm peak)
Sextupole	40	1000	-	-	100
Quadrupole	15	500	-	-	10
Corrector	100	10000		-	100
Dipole (Main Coil)	10		1000	See Plot	10
Dipole (Trim Coil)	10		1000	See Plot	50
Early Science Requirements					
Magnet	Ripple up to 1kHz (ppm rms)	Ripple >1kHz (ppm rms)	Ripple 1kHz-8kHz (ppm rms)	Ripple 8kHz-40kHz (ppm rms)	Long Term Drift (1s – 10 hours) (ppm peak)
Sextupole	100	2500	-	-	180
Quadrupole	30	1000	-	-	10
Corrector	100	10000	-	-	100
Dipole (Main Coil)	10	1000	-	-	10
Dipole (Trim Coil)	20	2000	-	-	50

Figure 2 assumes a single ripple line with FWHM of ≤800 Hz, or multipole such lines, separated by at least 800 Hz. The vendor shall provide the option for the peak (fundamental switching) frequency adjustment of +/-500Hz OR stay below the Ripple plot over the entire [8-40] kHz range. If a frequency adjustment is provided and there are no other, unrelated ripple peaks in the [8-40]

kHz range, then the ripple limit, integrated in the [8-40] kHz range, shall be 100ppm rms of the maximum operating PS current.

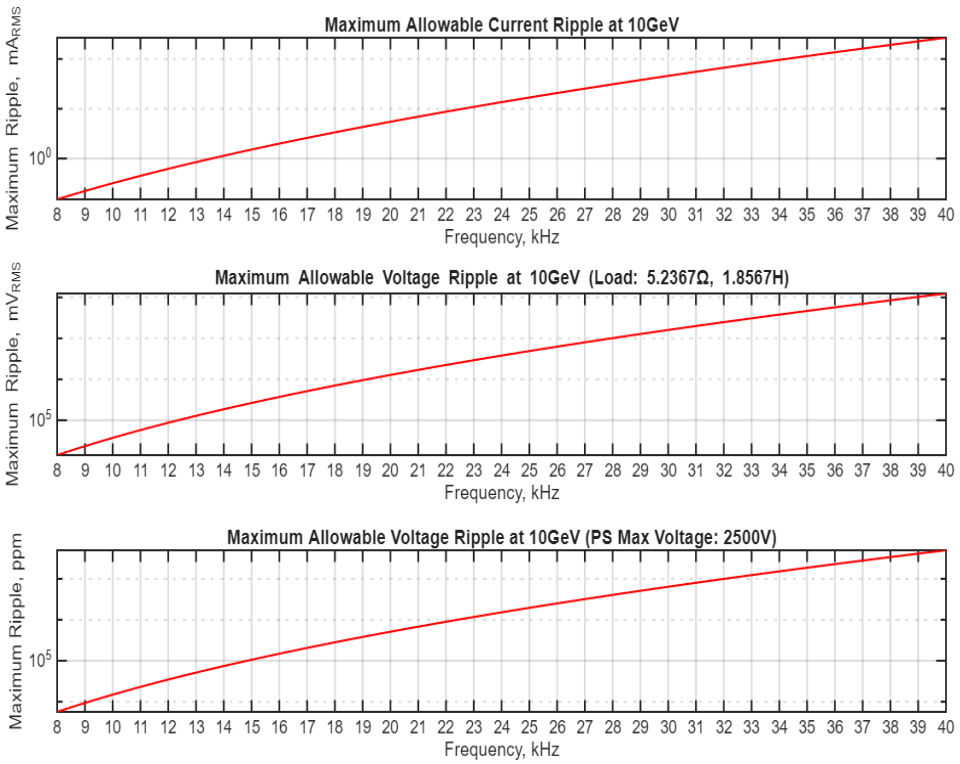


Figure 2. Maximum Allowable Ripple for ESR Main Dipole Power Supplies from 8kHz-40kHz. 10GeV operating conditions produce the tightest specification and are therefore used to generate the plots.

The plots in Figure 3 are generated based on the power spectral density specification used for the ESR Main Dipole. The power spectral density limit is relaxed by a factor of 100 to account for the different amp-turn ratio between main coil and trim coil. 10.4A is used as the operating current for the conversion. The ppm plot is based on a power supply with a maximum current of 300mA. This plot is valid for all trim coils.

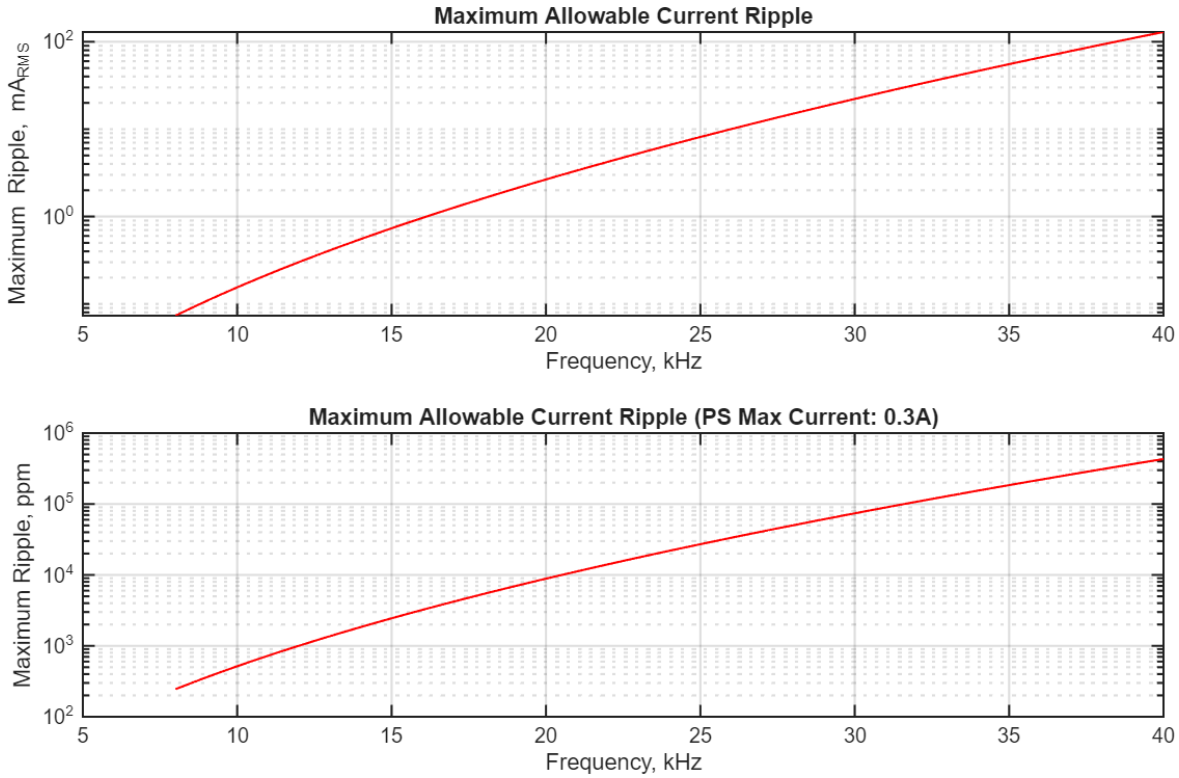


Figure 3. Maximum allowable ripple for ESR Dipole Trim coils

2.1.2 Determining Ripple Requirements for ESR Dipole 8–40kHz

The ripple specifications for the ESR Dipole magnets from 8kHz-40kHz are provided by physics as power spectral density plots. Therefore, the EIC power supply group translated the specifications into voltage and current. This mathematical process is described in detail in the tech note *Maximum Allowable Voltage Ripple for ESR Main Dipole Power Supply.*

The report converts the power spectral density (PSD) ripple specification (given in ppm²/kHz) into current and voltage ripple limits through a sequence of unit transformations grounded in physical relationships. First, the PSD is scaled to absolute current-squared spectral density (A²/kHz) by relating ppm to the maximum operating current and squaring the result. This is then interpreted as power spectral density by assuming a 1 Ω load (so $P = I^2R$), yielding W/kHz. Because the original specification is distributed over frequency with a Gaussian profile (±400 Hz), the method normalizes the spectral density by the peak of the Gaussian (derived from its FWHM) to recover total allowable power at each frequency. Taking the square root of this power gives RMS current ripple, and finally, frequency-dependent impedance $Z = \sqrt{R^2 + (2\pi fL)^2}$ is used to convert current ripple to voltage ripple via $V = IZ$. This stepwise approach systematically maps a frequency-domain PSD constraint into practical current and voltage ripple specifications.

2.2 Standards, Electrical Safety, and QA

The ESR power supply systems are designed with a strong emphasis on safety, regulatory compliance, and quality throughout their lifecycle. A structured framework governs design, procurement, manufacturing, and testing to ensure reliable, compliant, and safe operation.

2.2.1 ESH Safety Considerations

The ESR Power Supply Systems shall be designed, manufactured, and installed in accordance with the EIC Code of Record [EIC-ORG-RSI-026] to meet applicable safety and regulatory requirements. Compliance is ensured with the following standards and regulations:

Federal Regulations and Laws

- 10 CFR 851, 2023, Worker Safety and Health Program
- 29 CFR 1910, 2020, Occupational Safety and Health Standards

National Fire Protection Association

- NFPA 70, 2023, National Electric Code (design/purchase)
- NFPA 70E, 2021, Electrical Safety in the Workplace
- NFPA 111, 2022, Stored Electrical Energy Emergency and Standby Power Systems

U.S. Department of Energy

- DOE Order 414.1D, Chg. 2, 2011, Quality Assurance
- DOE Order 420.1C, Chg. 3, 2019, Facility Safety
- DOE-STD-1066, 2023, Fire Protection

Power supplies operate across a wide range of voltages and currents, presenting electrical shock and arc flash hazards. The design incorporates the following control measures:

- There will be no exposed AC power in power supply racks. All cords and plugs are standard IEC and NEMA configurations. All AC input terminals shall be sufficiently enclosed to prevent accidental contact.
- Priority is being made to procure and use Nationally Recognized Testing Laboratory (NRTL) certified equipment.
- Use of PDU for decreasing the level of Lockout-Tagout (LOTO) Personal Protective Equipment (PPE) requirement. The manufacturing of BTP PDUs will be handled by an assembly house capable of building and certifying UL508A.
- BNL established Work Planning and Control and LOTO procedures are followed during testing, installation, commissioning, operations and troubleshooting.
- Isolation and tagging mechanisms are implemented for maintenance access.
- Identification and mitigation of energized components in exposed or serviceable areas.

Heavy Equipment Handling (Weight and Lifting Considerations): Power supplies can be heavy, requiring safe mechanical handling. Improper rigging and lifting may present significant risks. The design incorporates the following control measures:

- Assess weight limits per rack.
- Incorporate lifting points and mechanical fixtures designed into chassis as applicable.
- Use of carts, hoists, or lift tables for transport and installation.

Non-NRTL Electrical Components: Power Supplies and its subsystems that are not certified by NRTL may not meet safety standards. NRTL certified electrical equipment and components will be purchased whenever commercially available as required by BNL Standards, provided they meet design requirements. The design incorporates the following control measures for non-NRTL components:

- Equipment with minimal hazards will be inspected and approved by BNL approved Electrical Equipment Inspectors (EEI Program).
- Equipment that is deemed too complex for the scope of a BNL EEI and equipment valued at greater than $50k must be field evaluated by an NRTL.

2.2.2 Quality Assurance for EIC ESR Power Supplies

The Quality Assurance (QA) approach for the EIC ESR power supply system establishes a structured framework integrated across design, procurement, manufacturing, and installation phases. A formal project-level QA plan [EIC-QAG-PLN-002] provides the foundation for developing system-specific Quality Control (QC) plans aligned with BNL and EIC standards. These QC plans ensure that quality requirements are defined early and consistently implemented throughout the project lifecycle. They include key documentation such as configuration controlled individual Quality Control documents, specifications, Statements of Work (SOW), Acceptance Criteria Lists (ACLs), and test procedures, ensuring that requirements are clear, measurable, and verifiable across all subsystem categories, including COTS, build-to-print, and custom systems.

Verification and validation are performed through a combination of vendor testing, BNL inspections, and system-level testing to ensure compliance with technical and performance requirements. Pre-production (first article) units are used to validate design and manufacturing processes prior to full production, while production units undergo defined acceptance testing and inspection. Full traceability is maintained through EIC-standard electronic travelers (e-travelers), which document all inspection and test activities. At the system level, integrated testing includes no-load, short-circuit, and full-load conditions which will be used to confirm operational readiness. This comprehensive QA approach ensures consistency, reduces risk, and supports reliable system performance meeting project’s requirements.

3 ESR Power Supply System Architecture

The final design builds upon the Preliminary Design Report (PDR) baseline, which was based on ESR Lattice v6.3 and extends it into a fully traceable and uniquely identifiable system based on Lattice v6.4.2. A higher level of detail has been implemented in the ESR PS Architecture Design Spreadsheet, along with a seamless data transfer from lattice data to the design environment.

With this increased level of design control, the architecture can be clearly summarized in building and rack rows tables. The position of each rack within a building, along with associated AC disconnects, cable trays, generated heat and how much is dissipated on each cooling system, are fully accounted for and organized to support efficient data export.

The ESR PS Architecture Design v2.3 includes 2710 magnets and 850 powered circuits (magnet strings), distributed across twelve buildings based on cable length optimization. The six new EIC buildings can accommodate any string type, while the existing RHIC buildings are limited to correctors and single-powered quadrupoles.

3.1 Physics Export to Power Supply Group

The transfer of data from physics/magnet to power supplies is an iterative process.

The process typically begins with a physics-driven lattice change, which is evaluated to determine whether it impacts specific accelerator lattices (ESR, HSR, or EIN). If applicable, the corresponding lattice working versions are updated, version-controlled, and ultimately published as frozen, traceable baselines. These updates are managed through formal revision control systems, ensuring that each iteration is documented and accessible. The updated lattice data is then propagated downstream to the magnet design process, where magnet string configurations are drafted, reviewed, and refined based on the new lattice parameters. If the changes affect magnet design, associated product requirement documents (PRDs) and technical specifications are updated accordingly.

Following magnet validation, the refined data is passed to the power supply team, where the system architecture is reviewed and updated to reflect the new requirements. The power supply design is iteratively verified against the updated magnet data, with checks to determine whether design changes are necessary and acceptable. If required, specifications are revised in coordination with physics/magnet team, and the system architecture is finalized. Throughout this workflow, structured checkpoints, version-controlled documentation, and feedback loops ensure traceability, cross-discipline alignment, and controlled iteration. The process continues until all changes are validated and approved, resulting in a finalized, published configuration that serves as the authoritative design baseline.

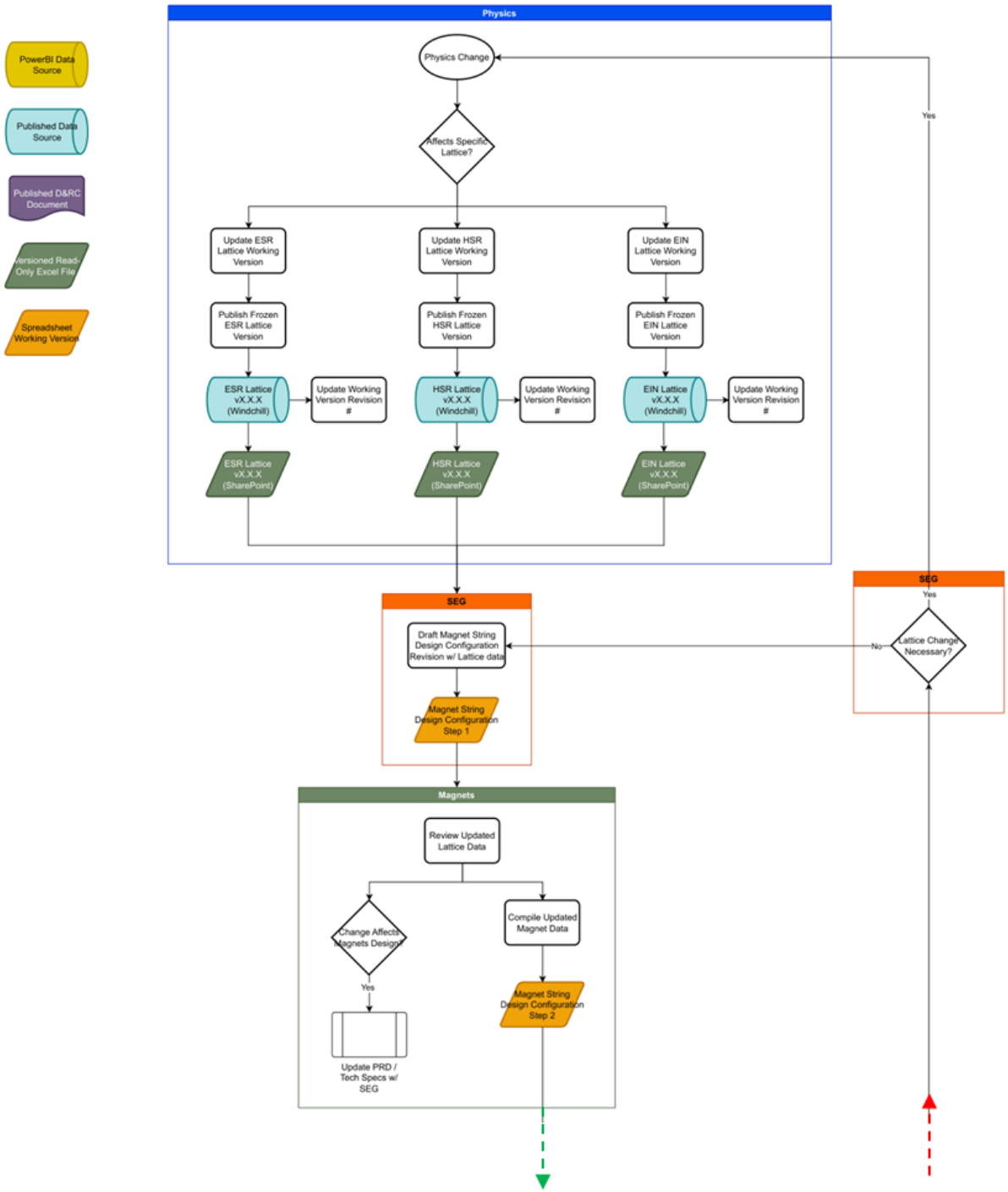


Figure 4. Physics Group to Power Supply Data Flow Diagram Pt.1

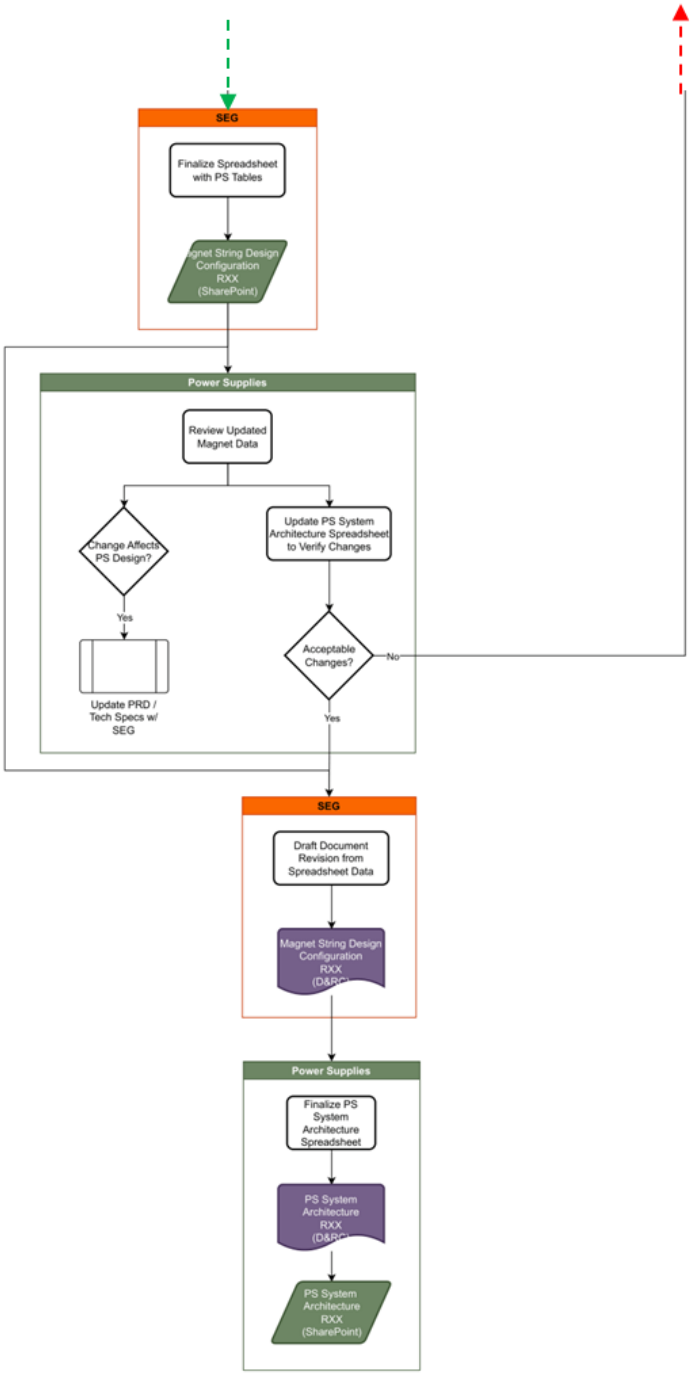


Figure 5. Physics Group to Power Supply Data Flow Diagram Pt. 2

3.2 Cable Length Calculation and Building Selection

The exported data from physics and magnet teams is published as an official string configuration document. This data is used to select buildings for power supplies and calculate round trip cable lengths. This critical data is exported to ESR PS Architecture Design v2.3 and used for the power supply selected process.

Cable lengths are important for determining the additional load the circuit will see. The first step in calculating the maximum cable resistance is determining the worst-case cable length. Next, the cable gauge is selected based on the maximum allowable currents provided by the National Electric Code (NEC). The ambient temperature is assumed to be 45℃, to account for thermal fluctuations in the cable from temperature rise in the ring. Then, a cable appropriately rated for radiation is selected. Lastly, the cable jacket temperature rating and the resistance per foot are used to realize the resistance.

3.2.1 Cable Length Calculation

There are 12 total service buildings that will be used for ESR. Figure 6 shows the locations of existing and new construction service buildings with respect to the ring. Most of the power supplies will be housed in the new construction service buildings, but to limit cable density in the ring, individually powered quadrupoles and correctors will be housed in both existing and new construction service buildings. The ESR is defined by 12 sectors, and the service buildings exist at the transition point between two arc sectors. The distribution is uniform, and a sector is 320.5 meters long, traversing the circumference of the ring. There are 6 arcs and 6 interaction regions. New construction service buildings will be located at the mid-point of each arc, while existing service buildings are located at the mid-point of the interaction regions.

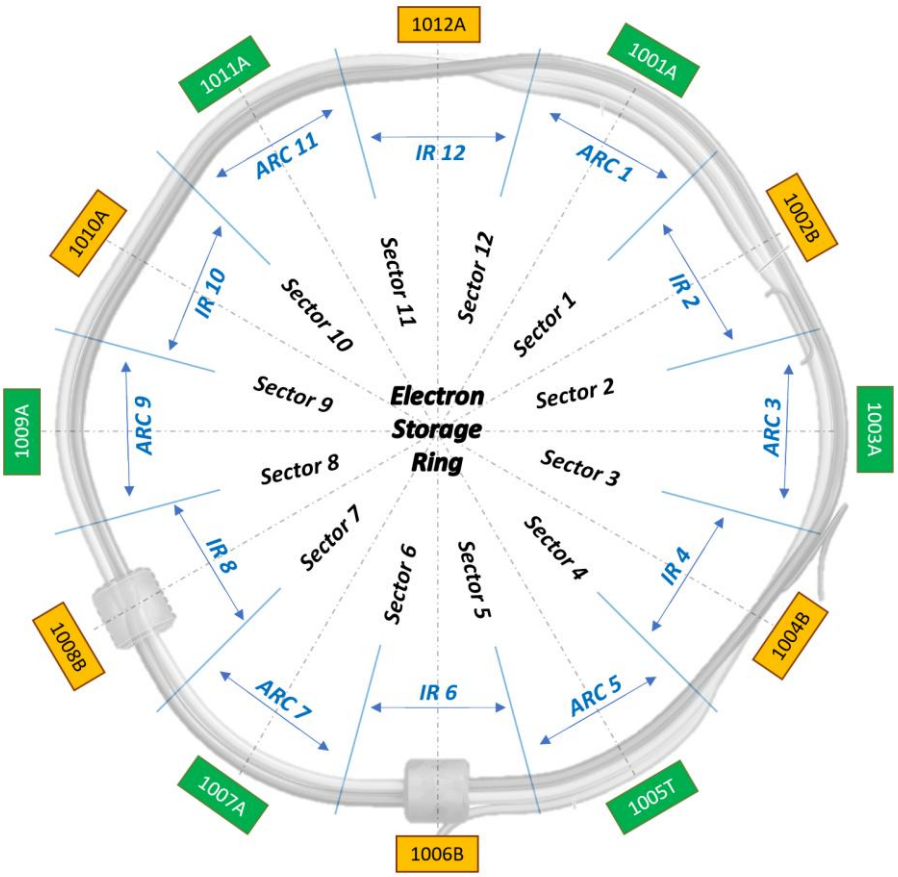


Figure 6. ESR Sectors with Existing (Yellow) and New Construction (Green) Service Buildings

Buildings are selected to house the power supplies based on the closest proximity to the magnet or string of magnets under power. The powering conductor must travel to the first magnet, connect all magnets in series, and travel back to the power supply. The distance from the service building to the ring entry point must also be accounted for as well as the service loop. The service loop is defined as the distance traveled from the cable tray, down to the magnet, and back to the cable tray. Margin is added as slack for the string and insertion distance. Therefore, the round-trip cable length is realized by the following equation.

$$L_{circuit} = \left[\left(2l_{string} + 2l_{insertion}\right) * \gamma_{slack}\right] + N_{mag} * l_{service}$$

- $L_{circuit}$ *round trip distance from the power supply to all magnets and back to the supply*
- l_{string} *distance between the ends of a magnet string*
- $l_{insertion}$ *distance from the supply to the ring entry point then to the start of a magnet string*
- $l_{service}$ *service loop length from cable tray, to magnet, and back to cable tray*
- γ_{slack} *20% increase to provide margin*
- N_{mag} *number of magnets in the string*

The service loop length is defined as 3.05 meters and the distance from the supply to the ring entry point is defined as 100 meters for all service buildings. This process is defined and documented in EIC-ROD-058.

3.2.2 Sextupole Family Configurations

The design establishes a structured approach for powering ESR sextupole magnets by organizing them into physics-defined families and connecting them through configurable link boxes. Across the arc sectors, 288 sextupole magnets are grouped into focusing and defocusing families that repeat consistently around the ring. These comprise of both short (repurposed) and long (new design) models. The families are wired such that magnets sharing the same function are electrically connected and routed to specific link box terminals. The link boxes act as configurable distribution points, enabling the system to switch between operating modes corresponding to different beam energies while maintaining consistent family-based powering.

The power supply configuration is designed to support operational flexibility by using different groupings depending on machine energy: two power supplies for the 90-degree (18 GeV) configuration and three for the 60-degree (5 and 10 GeV) configuration. The link box wiring enables these reconfigurations without physically rewiring the system, allowing efficient transitions between operating modes. Additional considerations include provisions for insertion region sextupoles, which are installed but initially unpowered, and the ability to "zero" selected magnets by locally shorting them in the tunnel to accommodate evolving lattice requirements. Together, this approach provides a modular, scalable, and adaptable powering scheme that aligns magnet configurations with physics needs while maintaining practical implementation and operational flexibility. This process is described in detail through EIC-ROD-042.

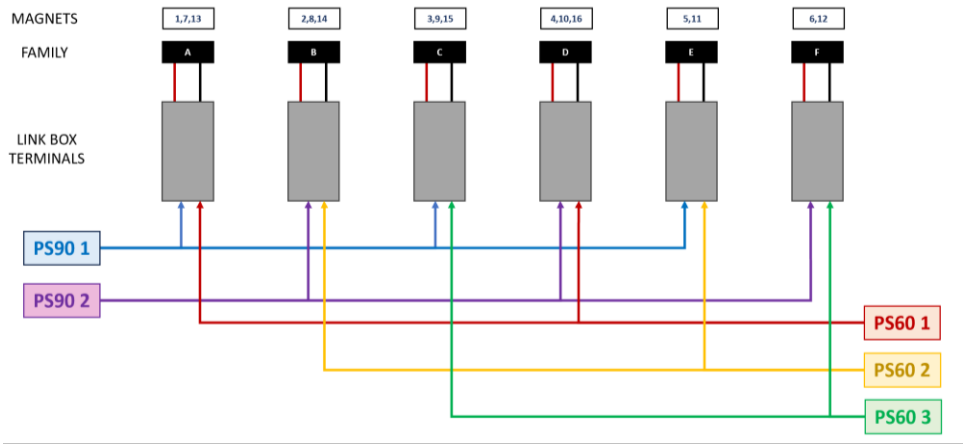


Figure 7. General layout for sextupole families (symmetrical across all arcs)

3.2.3 NEC Requirements for Cable Selection and Load Calculation

The maximum current the power supply can provide and circuit path length are used to determine magnet string cable size. For cables smaller than 1/0 AWG, two conductor multi-conductor tray rated cable will be used, as required by the NEC for use in cable trays. For cables 1/0 AWG or larger, single conductor tray rated DLO cable will be used. More detailed cable parameters and routing practices can be found in section 4.9.1 of this report. Allowable cable ampacities are calculated according to the NEC with all applicable deratings applied. This process is documented in EIC-ROD-043. The tables in EIC-ROD-043 show the delta between the allowable NEC ampacity and allowable ampacity from the manufacturer to ensure current limits are not being exceeded. After a size is selected, a specific cable part number will be assigned from a list of cables that have been accepted by the systems engineering group and BNL Authority Having Jurisdiction (AHJ). The total cable resistance is calculated based on cable length and a maximum ambient temperature in the tunnel of 45℃, to account for thermal effects on the resistance of copper.

3.3 Power Supply Selection and Rack Configuration

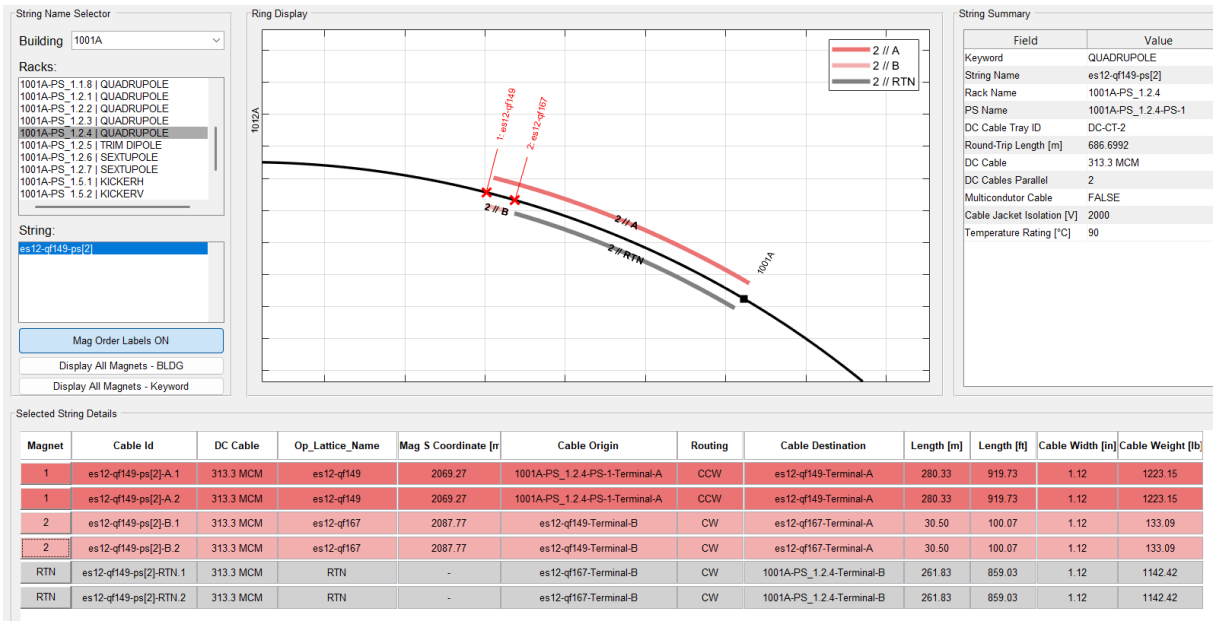
ESR PS Architecture Design v2.3 consists of 26 tabs, some containing more than 3,000 rows. Throughout its development, usability and clarity were prioritized to ensure the design remains accessible and easy to interpret. To support this, several visualization tools and auxiliary features were developed to aid in the design and in understanding the data and its relationships.

3.3.1 Spreadsheet Structure and Supporting Tabs

This section provides an overview of the supporting tabs, while the most critical ones are described in detail in the following sections.

- **COVER PAGE – DESIGN QUANTITIES:** consolidates summary and analytics tables that support the overall design. It includes information on magnet design status, magnet types, device quantities, power calculations, utility requirements, total cable length, cable tray usage, rack layout quantities, and other key metrics used to guide and evaluate the design.

- **COVER PAGE – DC CABLES:** each row represents a magnet in the lattice with its corresponding S-coordinate. This tab defines the magnet powering order within each string, identifying the sequence of magnets in the circuit. Using the coordinates of both magnets and buildings, cable segment lengths are calculated for each portion of the string. Each cable is assigned a label including its ID, origin, and destination, enabling clear tracking and simplified analysis. The Lattice Viewer application sources its data directly from this table to provide a visual representation of each string, aiming to help with the interpretation of the data.



Magnet	Cable Id	DC Cable	Op_Lattice_Name	Mag S Coordinate [m	Cable Origin	Routing	Cable Destination	Length [m]	Length [ft]	Cable Width [in]	Cable Weight [lb]
1	es12-qf149-ps[2]-A.1	313.3 MCM	es12-qf149	2069.27	1001A-PS_1.2.4-PS-1-Terminal-A	CCW	es12-qf149-Terminal-A	280.33	919.73	1.12	1223.15
1	es12-qf149-ps[2]-A.2	313.3 MCM	es12-qf149	2069.27	1001A-PS_1.2.4-PS-1-Terminal-A	CCW	es12-qf149-Terminal-A	280.33	919.73	1.12	1223.15
2	es12-qf149-ps[2]-B.1	313.3 MCM	es12-qf167	2087.77	es12-qf149-Terminal-B	CW	es12-qf167-Terminal-A	30.50	100.07	1.12	133.09
2	es12-qf149-ps[2]-B.2	313.3 MCM	es12-qf167	2087.77	es12-qf149-Terminal-B	CW	es12-qf167-Terminal-A	30.50	100.07	1.12	133.09
RTN	es12-qf149-ps[2]-RTN.1	313.3 MCM	RTN	-	es12-qf167-Terminal-B	CW	1001A-PS_1.2.4-Terminal-B	261.83	859.03	1.12	1142.42
RTN	es12-qf149-ps[2]-RTN.2	313.3 MCM	RTN	-	es12-qf167-Terminal-B	CW	1001A-PS_1.2.4-Terminal-B	261.83	859.03	1.12	1142.42

Figure 8. Example of Lattice Viewer

- **DESIGN PARAMETERS:** consolidates all key constants and reference values used throughout the design, including building coordinates, cooling system specifications, rack dimensions, and other global parameters.

- **COST ESTIMATE:** provides a simplified cost estimate based on the official cost analysis, supporting comparisons between different architecture designs. Labor and installation costs are not included.

- **POWER SUPPLIES MODELS:** this table gathers information about many COTS available in the market and the possible arrangements we can make with them. This tab starts with every PS model from 0.75 to 15 kW as stand alone. Then the spreadsheet groups each model into different arrangements and lists the new possibilities.

- **CONDUCTOR SIZE DATA:** gathers data about each cable considered for use in the final design. The data is acquired directly from datasheets for cables confirmed for use in accelerator applications.

Table 3. Conductor specifications after NEC derating

Cable Family	Wire Size	Part Number	Cable Voltage [V]	Temperature Rating [°C]	Conductors / Cable	Derated Ampacity (A)	Conductor Diameter (in)	Weight (lbs/ft)	Tray Space (in)	Resistance (Ω/ft)
Belden	22 AWG	B82723-1000	300	80	4	**2.3**	0.153	0.017	0.168	0.014700
Okonite Okoseal	14 AWG	203-70-3501	600	90	2	**15.0**	0.064	0.072	0.352	0.002742
Okonite Okoseal	12 AWG	203-70-3601	600	90	2	**20.0**	0.081	0.094	0.396	0.001724
Okonite Okoseal	10 AWG	203-70-3701	600	90	2	**27.8**	0.102	0.138	0.473	0.001085
Okonite Okoseal	8 AWG	116-70-3103	600	90	2	**38.3**	0.128	0.278	0.649	0.000682
Okonite Okoseal	6 AWG	116-70-3123	600	90	2	**52.2**	0.162	0.396	0.737	0.000429
Okonite Okoseal	4 AWG	116-70-3301	600	90	2	**66.1**	0.204	0.604	0.891	0.000270
Okonite Okoseal	2 AWG	116-70-3313	600	90	2	**90.5**	0.258	0.926	1.078	0.000170
TF Kable 2000V DLO Cable	1/0 AWG	DLO1/0	2000	90	1	**147.0**	0.325	0.515	0.738	0.000107
TF Kable 2000V DLO Cable	2/0 AWG	DLO2/0	2000	90	1	**169.7**	0.365	0.600	0.782	0.000085
TF Kable 2000V DLO Cable	3/0 AWG	DLO3/0	2000	90	1	**197.9**	0.410	0.792	0.866	0.000067
TF Kable 2000V DLO Cable	4/0 AWG	DLO4/0	2000	90	1	**229.0**	0.460	0.975	0.972	0.000053
TF Kable 2000V DLO Cable	262.6 MCM	DLO262	2000	90	1	**263.5**	0.512	1.135	1.045	0.000043
TF Kable 2000V DLO Cable	313.3 MCM	DLO313	2000	90	1	**293.3**	0.560	1.330	1.117	0.000036
TF Kable 2000V DLO Cable	373.7 MCM	DLO373	2000	90	1	**334.2**	0.611	1.564	1.195	0.000030
TF Kable 2000V DLO Cable	444.4 MCM	DLO444	2000	90	1	**369.1**	0.667	1.817	1.286	0.000025
Uniblend MV 5/8kV	500 MCM	17001.13651	5000	90	1	**558.0**	0.732	2.297	1.397	0.000021
TF Kable 2000V DLO Cable	535.3 MCM	DLO535	2000	90	1	**434.2**	0.732	2.162	1.342	0.000021

- **BUILDINGS LAYOUTS:** gathers tab pulls data from the Racks Layout tab to provide a clear and organized view of the building configuration. An example of the first few racks in Building 1001A is shown below, and the same structure is applied to all rows, positions, and buildings.

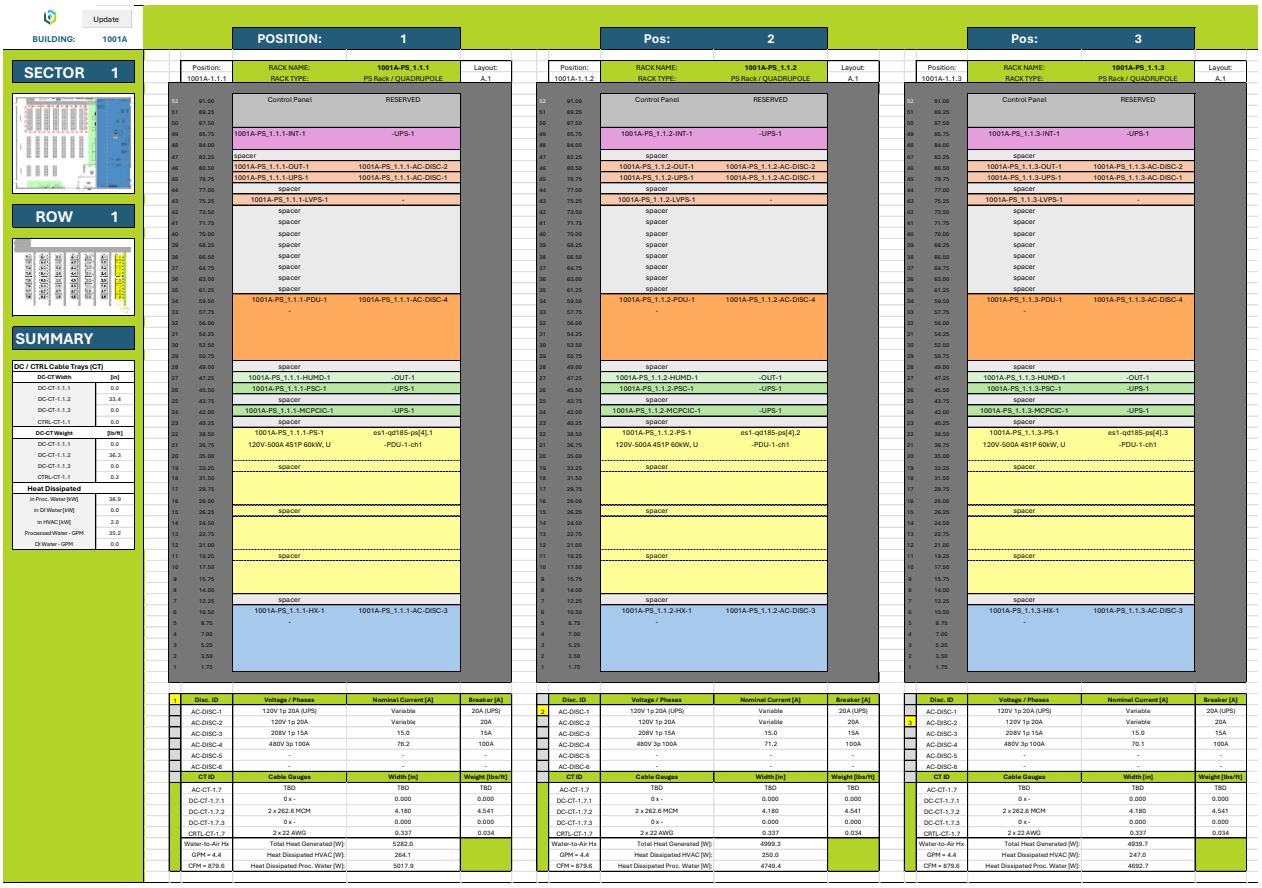


Figure 9. Rack Layout Example in Building 1001A (only first three racks shown)

3.3.2 Magnet Design Parameters

The spreadsheet tab "Magnet Designs" gathers all relevant information for each magnet model. This table serves as source of information for the algorithm to determine the different loads each PS will have. The information is transferred via systems engineering grouped with their respective Requirements from Technical Document EIC-SEG-RSI-110.

Information about the Design Status, Magnets and Powered Circuits quantity, Magnet Maximum Current, Magnet Inductance and Resistance, stability and ripple requirements, Maximum Voltage to Ground during Operation and during Faults, minimum Bits Setpoint for the PSC and some more requirements are available in the table and can be easily updated.

Table 4. Portion of the Magnet Design Table for ESR Quadrupole Magnets

Keyword	Mag Alias	Design Status	Magnets Quantity	Circuits Quantity	Mag Maximum Current [A]	Mag Nominal Resistance [Ω]	Magnet Inductance [H]	Magnet Cooling Method	Mag Temperature Rise [°C]	Magnet Polarity	Voltage-to-Ground during Operation [V]	Long-Term Stability [ppm]	Setpoint Resolution [Bit]
QUADRUPOLE	Q_LA	Assumption	10	10	650.0	0.045	0.041	Water	15	Unipolar	300	10	20
QUADRUPOLE	Q_SKEW	Assumption	13	13	412.0	0.015	0.009	Water	15	Unipolar	300	10	20
QUADRUPOLE	Q120	Assumption	22	22	412.0	0.066	0.041	Water	15	Unipolar	300	10	20
QUADRUPOLE	QLS3	Assumption	4	4	590.0	0.024	0.000	Water	15	Unipolar	300	10	20
QUADRUPOLE	QS1	Assumption	2	2	590.0	0.024	0.000	Water	15	Unipolar	300	10	20
QUADRUPOLE	QS2	Assumption	4	4	590.0	0.024	0.000	Water	10	Unipolar	300	10	20
QUADRUPOLE	QS3	Assumption	8	8	590.0	0.024	0.000	Water	15	Unipolar	300	10	20
QUADRUPOLE	QS4	Assumption	2	2	590.0	0.024	0.000	Water	15	Unipolar	300	10	20
QUADRUPOLE	QS5	Assumption	4	4	590.0	0.024	0.000	Water	15	Unipolar	300	10	20
QUADRUPOLE	Q50	FDR	214	66	412.0	0.030	0.017	Water	15	Unipolar	300	10	20
QUADRUPOLE	Q60	FDR	71	60	412.0	0.035	0.020	Water	15	Unipolar	300	10	20
QUADRUPOLE	Q80	FDR	72	72	412.0	0.044	0.027	Water	15	Unipolar	300	10	20
QUADRUPOLE	QN	FDR	38	24	410.0	0.048	0.009	Water	15	Unipolar	300	10	20

It is important to notice that every time a string does not have a current defined for any Energy Level, the Design defaults to the value in column Mag Maximum Current [A]. This represents the maximum current the magnet coils can handle, and the PS selection in these cases guarantees that the full range of operation is covered.

3.3.3 Cable Size and Power Supply Selection Algorithm

The cable sizing and power supply selection process is implemented through a structured workflow in the *Power Supplies Cables* tab, where each string is listed along with all relevant parameters required for the analysis.

The process begins by assigning the minimum cable gauge available (14 AWG) to all strings. Cable properties are retrieved from the *Conductor Size Data* tab, which contains NEC-derated parameters for each conductor type, including maximum current per conductor and heat dissipation per unit length. These values are automatically adjusted based on the number of cables in parallel.

The next step of the algorithm compares the highest operating current of each string against the allowable current of the selected cable. In parallel, thermal limits are verified through nominal and maximum heat dissipation. Visual indicators highlight any violations, allowing quick identification of insufficient cable selections. Based on these checks, the minimum required cable gauge and number of parallel conductors are determined for each string, being increased step by step from the minimum gauge until all indicators show the cable can safely handle the current.

Once the minimum cable capable of supporting the nominal current is identified, the corresponding voltage drop is calculated. This establishes the minimum voltage and power requirements for the PS. A suitable PS model is then selected from the database, prioritizing the lowest-rated unit that satisfies all current, voltage, and power constraints. Selecting the lowest acceptable current rating helps minimize cable size and overall system footprint.

After the PS is selected, the cable sizing is updated to account for the PS maximum output current. The cable must now support the full PS rating, not only the operating current. The smallest cable gauge that satisfies this condition is selected.

In the final step, the updated cable configuration is used to recalculate the voltage drop. If this results in reduced voltage requirements, the PS selection is revisited to determine whether a smaller unit can be used. In several cases, this iterative step allowed further optimization by selecting lower-rated PS models.

3.3.4 Power Requirements

The AC and DC power requirements associated with each building are determined and summarized in the table below. These values consider only the power supplies demands. Supporting equipment is accounted for separately.

Table 5. AC and DC Power Requirements per Building (Power Supplies only)

Building	AC Power [kVA]	DC Power [kW]
1001A	638.2	490.5
1002B	183.3	138.0
1003A	1,586.5	1,233.3
1004B	343.5	254.9
1005T	745.6	573.6
1006B	797.3	610.3
1007A	644.9	495.8
1008B	338.0	251.9
1009A	2,602.6	2,031.0
1010B	622.9	454.9
1011A	581.8	445.1
1012B	291.9	219.3
TOTAL	**9,376.5**	**7,198.6**

Buildings 1003A and 1009A have the highest power demands due to the Main Dipole supplies being present there. The overall efficiency of the power system is estimated to be around 77%.

3.3.5 Supporting Equipment Assignments

The power supplies will require supporting equipment for full operation inside the racks. The full power supply system for any circuit consists of the supply itself, a PSC, DCCT, PDU, and MCPCIC (if needed for series/parallel configurations).

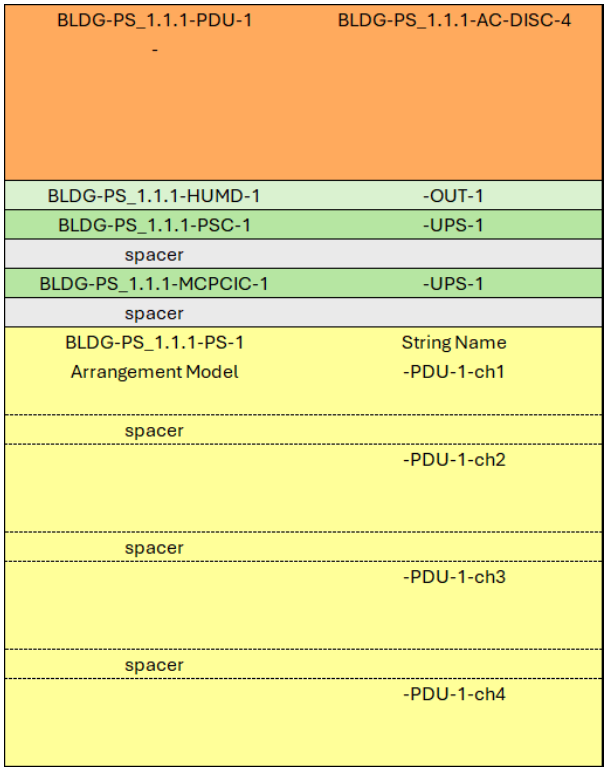


Figure 10. Example of a 4COTS Arrangement, 2CH PSC, 4CH MCPCIC, and 4CH PDU

After a rack is defined and the power supplies are assigned, the required supporting equipment can be determined to ensure proper operation.

PSC: the algorithm determines the number of required channels and their resolution (18-bit or 20-bit) based on the number of power supply arrangements in the rack. Each arrangement requires one channel, regardless of the number of COTS units. Racks with one or two arrangements use a 2-channel PSC, while racks with three or four arrangements use a 4-channel PSC. The required resolution for each string is defined in the *Magnet Parameters* table.

MCPCIC: an MCPCIC is required whenever an arrangement includes two or more COTS power supplies. The number of channels corresponds to the number of COTS units, with one channel per unit. If the COTS units are only connected in series, no parallel board is required. If parallel operation is present, the MCPCIC model with a current-sharing board is selected.

PDU: the algorithm evaluates the AC input requirements of each power supply to determine the appropriate PDU model. For 480V three-phase systems, available options include two 4-channel models with 70 A or 100 A input breakers, and one 2-channel model with a 45 A input breaker. For 208V three-phase systems, a 4-channel model with a 70 A breaker and a 2-channel model with a 40 A breaker are available. Correctors and some low-power sextupoles require 208V single-phase, for which a COTS PDU is selected.

DCCT: the algorithm selects a DCCT for each circuit based on the nominal current of the string. All COTS models use packaged DCCTs. The BTP units are designed to interface with a BTP DCCT chassis, which uses unpackaged DCCTs.

3.3.6 Rack Assignment Algorithm

The rack assignment algorithm defines all devices within each rack and performs the calculations required to determine rack-level parameters. It also assigns a unique identifier to every device, ensuring full traceability across the design in the following format:

$$BLDG - TYPE - POSITION - DEVICE - \#$$

An example of the second PSC in Building 1005T, rack in position 1.5.1 would result in the following label: 1005T-PS_1.5.1-PSC-2.

This is the most complex and computationally intensive tab in the spreadsheet, with 3,657 rows and 105 columns, most of which contain formulas. The generation of all racks across the buildings can take several hours, reflecting the level of detail and integration in the design.

The process begins by organizing the power supplies within each building based on power level and magnet type. Rack assignment is performed manually, with the spreadsheet supporting the process by providing immediate feedback on rack constraints and performance. To reduce the load on PDUs, higher-power power supplies are paired with lower-power units of the same magnet type whenever possible, while maintaining the base rack layouts.

The table is color coded to improve readability. White cells represent individual devices within a rack, green represents PS racks, orange represents auxiliary racks, purple represents Link Boxes, and blue represents Main Dipole systems.

Once power supplies are assigned to racks, the algorithms determine the required supporting equipment and configurations. This includes selecting the PSC type and number of channels, assigning PDUs and their channels, defining the heat exchanger type based on heat load and stability requirements, and adding temperature controllers and humidity sensors when required. Each rack is also assigned strip PDUs, an LVPS chassis, reserved space for control interfaces, an interlock panel, and a DCCT PDU when necessary. The number of power supply arrangements defines the type of MCPCIC required.

The sheet also manages device placement within each rack. Device positions follow standard rack layouts, and warnings are generated if overlapping positions are detected.

Some of the parameters calculated in this table are:

- Total CFM required by the PSs in the rack
- AC disconnects and their characteristics
- Heat generated inside the rack and how it is dissipated, including heat exchanger assignment
- Connections between PSs, PDUs, and PSCs, uniquely identified and traceable
- DC cable routing, including origin, destination, size, and weight
- Cable tray requirements

- Control cable routing inside the building
- Requirement for DCCT PDU within the rack
- Input data for building layout generation

Table 6. Example of Rack 1006B_1.3.4 that illustrates the Rack and Devices rows in the Design

Building	Rack Name	Device Name	Device Type	Device Height [U]	Device Position [U]	CFM	Heat Generated [W]	AC Input [V]	AC Input Phases	Panel Disconnect Identifier	Disconnect
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4	Standard Rack	28	K.2	393	2,359.1	120, 208	1, 3	-	-
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-PS-1	Power Supply	1	17	36	170.6	208	3	-	-PDU-1-ch1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-PS-2	Power Supply	2	9	119	324.0	208	3	-	-PDU-1-ch2
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-PS-3	Power Supply	2	12	119	365.8	208	3	-	-PDU-1-ch3
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-PS-4	Power Supply	2	15	119	498.6	208	3	-	-PDU-1-ch4
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-PSC-1	4Ch. 20Bits PSC	1	41	0	0.0	120	1	-	-UPS-1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-PDU-1	4Ch. 208V PDU	4	22	0	0.0	208	3	1006B-PS_1.3.4-AC-DISC-4	208V 3p 70A
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-INT-1	Interlock Panel	2	49	0	0.0	120	1	-	-UPS-1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-TEMP-1	Temperature Controller	0	33	0	0.0	120	1	-	-OUT-1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-HUMD-1	Humidity Sensor	1	33	0	0.0	120	1	-	-OUT-1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-LVPS-1	LVPS	1	44	0	0.0	120	1	-	-OUT-1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-DCCT-PDU-1	DCCT Low Power	1	43	0	0.0	120	1	-	-OUT-1
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-UPS-1	18Ch. 1p UPS	1	45	0	0.0	120	1	1006B-PS_1.3.4-AC-DISC-1	120V 1p 20A (UPS)
1006B	1006B-PS_1.3.4	1006B-PS_1.3.4-OUT-1	18Ch. 1p PDU	1	46	0	0.0	120	1	1006B-PS_1.3.4-AC-DISC-2	120V 1p 20A

3.4 Power Supply Export to Infrastructure

The data export process was developed to provide only the information required by other groups, while keeping the data clear and consistent. Several iterations have been performed to simplify the output and remove unnecessary details.

The spreadsheet generates summary tables with key infrastructure parameters, such as input power, processed water flow (GPM), total heat generation, cable tray width and weight, AC disconnects requirements, and other relevant quantities. These outputs are organized to support coordination with infrastructure and systems engineering. With the new functionality of placing a rack in an exact position in the building, summaries for each rack row are also available.

Because the spreadsheet contains many formulas, the main file is relatively large (~40 MB). To improve usability, a TEXT version is provided with each release. This version contains the same values but no formulas, making it faster to open and easier to navigate.

To further simplify data sharing, building-specific TEXT files are also generated. Each file includes only the relevant tabs for a single building and removes tabs that are required for the next steps. Tabs DC Cables, Power Supplies, Racks Layout, and Building Layout keep the information about the specific building and remove unnecessary columns, making it easier for infrastructure teams to navigate the design.

3.4.1 Building Layouts

Each building is represented by a dedicated Building Layout tab, where all rack positions are mapped according to their physical location. Visual references are included to aid interpretation of the layout within the building.

For racks that are required by the ESR power supply system, all devices are displayed based on their defined position within the rack as specified in the Racks Layout tab under column Device Position [U]. Unassigned racks are shown as blank racks so other groups can select empty spaces for their racks.

Sextupole Link-Boxes and Main Dipole systems are also included in the layout, with their physical footprint accounted for. Link-Boxes occupy the equivalent space of four racks, while Main Dipole systems occupy sixteen rack positions. The layout is color-coded by device type to improve readability and navigation.

Each rack has its own associated utilities table. A summary with the name and types of disconnects, the associated cables (AC, DC and control cables) and cooling system requirements. The cable data includes the total width and weight sorted by cable tray type. The cooling system features the heat exchanger (Hx) type (Air-to-Air, Water-to-Air, or Row Coolers), heat dissipated, ratings for both air and water flow to the rack.

An example of a PS rack and its associated utilities requirement table is shown below.

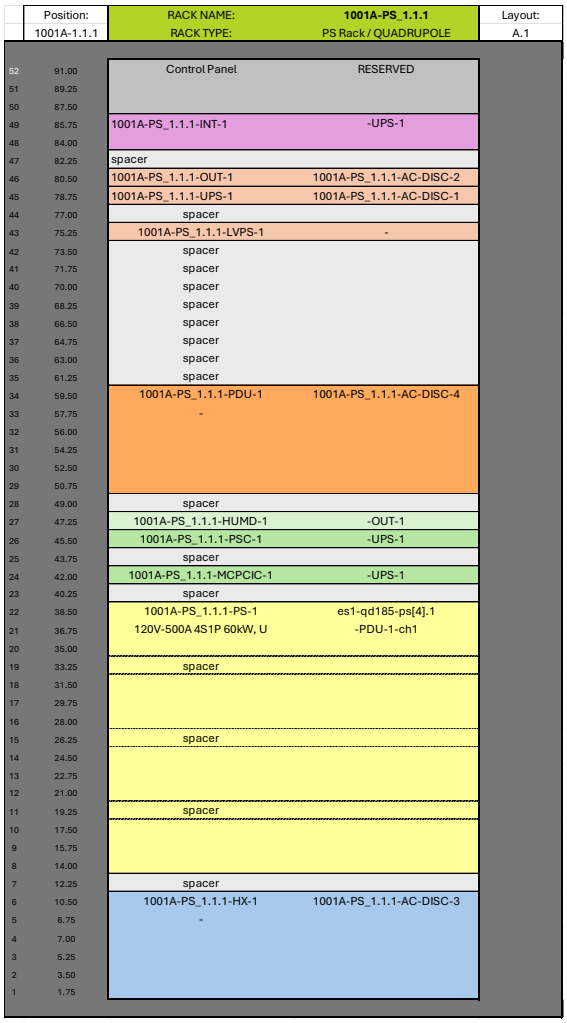


Figure 11. Individual Rack Layout

Table 7. Utilities Table Associated with Rack in Figure 11

1	Disc. ID	Voltage / Phases	Nominal Current [A]	Breaker [A]
	AC-DISC-1	120V 1p 20A (UPS)	Variable	20A (UPS)
	AC-DISC-2	120V 1p 20A	Variable	20A
	AC-DISC-3	208V 1p 15A	15.0	15A
	AC-DISC-4	480V 3p 100A	76.2	100A
	-	-	-	-
	-	-	-	-
	CT ID	**Cable Gauges**	**Width [in]**	**Weight [lbs/ft]**
	AC-CT-1.7	TBD	TBD	TBD
	DC-CT-1.7.1	-	-	-
	DC-CT-1.7.2	2 x 262.6 MCM	4.180	4.541
	DC-CT-1.7.3	-	-	-
	CRTL-CT-1.7	2 x 22 AWG	0.337	0.034
	Water-to-Air Hx	Total Heat Generated [W]:	5282.0	
	GPM = 4.4	Heat Dissipated HVAC [W]:	264.1	
	CFM = 879.6	Heat Dissipated Proc. Water [W]:	5017.9	

3.4.2 Building Requirements

Each building includes a summary of its infrastructure requirements. These include total electrical load, Uninterrupted power Supply (UPS) demand, processed and deionized water flow rates, and total heat dissipation. The values are calculated from the rack-level data and are used to support infrastructure sizing, system integration, and building planning.

Table 8. Building Requirements

Data Export - Utilities	1001A	1002B	1003A	1004B	1005T	1006B	1007A	1008B	1009A	1010A	1011A	1012A	Total
Total Racks [qty]	24	11	22	18	27	29	25	17	22	25	23	16	259
Air-to-Air Hx [qty]	6	6	6	6	6	8	6	6	6	6	6	6	74
Water-to-Air Hx [qty]	18	5	16	12	21	21	19	11	16	19	17	10	185
Heat Dissipated in Proc. Water [kW]	81.9	24.0	74.3	53.4	92.6	102.9	81.3	50.6	73.8	103.4	76.9	42.5	857.4
Heat Dissipated in DI Water [kW]	0.0	0.0	231.7	0.0	0.0	0.0	0.0	0.0	463.4	0.0	0.0	0.0	695.1
Heat Dissipated in HVAC [kW]	0.0	0.0	231.7	0.0	0.0	0.0	0.0	0.0	463.4	0.0	0.0	0.0	695.1
Input Power (AC) [kVA]	638.2	183.3	1586.5	343.5	745.6	797.3	644.9	338.0	2602.6	622.9	581.8	291.9	9376.5
Processed Water [gpm]	79.2	22.0	74.8	52.8	92.4	92.4	83.6	48.4	79.2	83.6	74.8	44.0	827.2
DI Water [gpm]	0.0	0.0	61.4	0.0	0.0	0.0	0.0	0.0	122.8	0.0	0.0	0.0	184.2
Footprint [ft2]	227.3	104.2	208.4	170.5	255.7	274.7	236.8	161.0	208.4	236.8	217.9	151.6	2453.2

Additionally, a 2D layout of each building is generated to indicate specific rack placement by type, water and cable tray routing, sextupole link box placement, and overall footprint. These drawings provide infrastructure with valuable information for building construction.

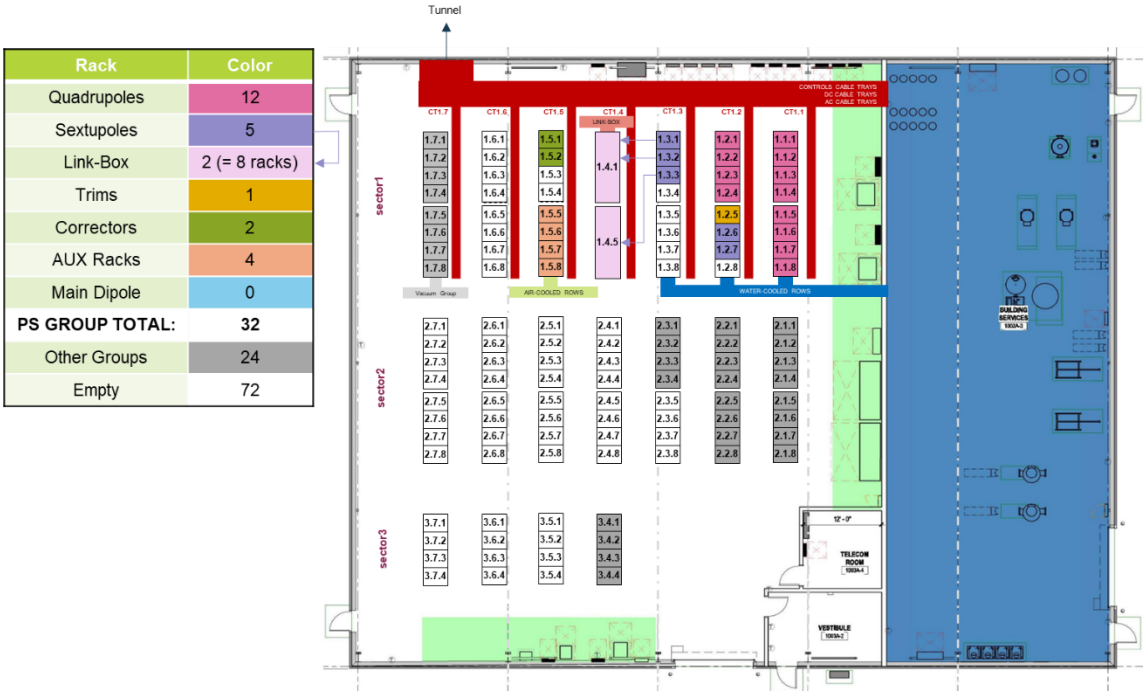


Figure 12. Building 1001A Layout

4 ESR Power Supply System Design

The ESR power supply system is designed to support physics-defined magnet strings using a combination of custom, BTP, and COTS solutions. The overall architecture emphasizes modularity, scalability, and standardization, allowing consistent implementation across all service buildings while accommodating a wide range of magnet types.

The ESR main dipole requires a custom power supply solution to meet the high power demands and strict ripple and stability requirements. Unipolar COTS power supplies are primarily used to power quadrupole, sextupole, and dipole trim magnets. Bipolar BTP power supplies are used to power all corrector magnets, as well as some dipole trim magnets operating at low currents. Both solutions integrate with BTP control and interface hardware such as the PSC, external interface chassis, and rack-mounted PDUs. These systems are designed to provide high stability, precise current regulation, and seamless integration with the control system and machine protection infrastructure.

Power Supply -Model/Magnets	Arrangements Qty of PS's	PS Max. Voltage (V)	PS Max Current (A)	PS Configuration	Current Ripple of max operating current in ppm RMS 0Hz-1kHz Greater than 1kHz 1kHz – 8kHz 8kHz-40kHz	Stability / Resolution PPM of max Current	Operation Mode
Main Dipole PS *es-dmainA-ps [249]* *es-dmainB-ps [249* *es-dmainC-ps [249]*	1 1 1 1	7500 2500 2500 2500	700 700 700 700	Custom Power supplies 2-4 Channel PSC - Analog Curr. Regulator – 2 DCCTs per Channel	10 N/A 1000 Plot in back up slides	10 (20 bit) 1	DC 1 Quadrant
Quadrupoles PS	291 574	20-200 20-100	120-668 120-500	COTS Unipolar Switch-Mode Power Converter 2-4 Channel PSC - Analog Curr. Regulator – 2 DCCTs per Channel	15 500 N/A N/A	10 (20 bit) 1	DC 1 Quadrant
Sextupole PS	81 121	50-400 50-200	7.5-200 7.5-200	COTS Unipolar Switch-Mode Power Converter 2-4 Channel PSC - Analog Curr. Regulator – 2 DCCTs per Channel	40 1000 N/A N/A	100 (18 bit) 3.8	DC 1 Quadrant
Trim PS (Dipole) COTS BTP COTS & BTP	34 22 10 2	80-500 80-500 5 0.9-100	0.3-12.5 1.6-10.4 0.3 0.1-15	COTS Unipolar Switch-Mode Power Converter BTP 4 Channel Bipolar Linear Mode Power Converter 2-4 Channel PSC - Analog Curr. Regulator – 2 DCCTs per Channel	10 N/A 1000 Plot in back up slides	50 (18 bit) 3.8	DC 1 Quadrant
Bipolar PS *Horizontal Corrector* *Vertical Corrector*	443 221 222	- 40 40	- 10 10	BTP 2 Channel Bipolar Switch Mode Power Converter 4 Channel PSC - Analog Curr. Regulator – 2 DCCTs per Channel	100 10000 N/A N/A	100 (18 bit) 3.8	DC (Slow) 4 Quadrant
					Blue shading: changes from PDR due to 6.4.2 lattice		

Figure 13. ESR Power Supply System Design and Requirements

4.1 Custom Power Supply for ESR Main Dipole

The ESR Main Dipole Power Supply system is a custom unipolar DC power conversion system designed to provide continuous power to the ESR main dipole magnet string. The system is required to deliver the full operating current and voltage necessary to support ESR operation across all defined machine energy levels while maintaining stable, repeatable DC output under steady-state operating conditions. The operating currents are used to determine operating voltages for each energy level. The dipole magnets are designed with tap configurations, which changes the load at each energy level. Therefore, the load at each energy level is calculated based on the tap configuration specifications, cable resistance is calculated and added, and margin is added for thermal fluctuations. 20% reliability margin is applied to both the operating currents and voltages to size the custom supply.

Table 9. ESR Main Dipole Specifications at all Energy Levels

Energy Level	Operating Current (A)	Total Resistance (Ω)	Operating Voltage (V)	Maximum Current (A)	Maximum Voltage (V)
18 GeV	391.40	15.75	6,166.08	469.68	7,399.30
10 GeV	214.50	15.75	3,379.21	257.40	4,055.06
5 GeV	556.00	6.94	3,860.90	667.20	4,633.07

4.1.1 Functional Requirements and Performance Specifications

The ESR Main Dipole Power Supply system is implemented as a series-connected DC power conversion architecture to provide the total output voltage required by the ESR main dipole magnet string while maintaining compliance with magnet voltage-to-ground limits. The system consists of three custom unipolar DC power supplies connected in series for the full dipole magnet circuit.

Each individual main dipole power supply unit shall be rated to provide a nominal output of 2500 V DC at up to 700 A DC in continuous operation. The combined main dipole power supply system, consisting of three supplies connected in series, shall provide a total output capability of up to 7500 V DC at 700 A DC to the main dipole magnet circuit. The system shall operate in DC mode and support both current regulation and voltage regulation modes as required by the overall system control architecture.

The main dipole power supply system shall support operation at the defined ESR operating energies of 5 GeV, 10 GeV, and 18 GeV. The power supply output range and regulation performance shall accommodate the corresponding operating current and voltage conditions associated with each energy level without requiring hardware reconfiguration of the power supply system.

The output current regulation accuracy, stability, drift, and ripple performance of the main dipole power supply system shall meet the ESR science requirements defined in EIC-ROD-044 and the associated technical notes governing ripple and stability performance for the ESR main dipole system. These performance requirements are not redefined in this document and are referenced as controlling requirements for the main dipole power supply design.

The main dipole power supply system shall be designed for continuous-duty operation and stable long-term steady-state performance at the nominal ESR operating points.

The power supply system shall provide interfaces for remote control, monitoring, and interlock integration through the ESR controls infrastructure. This includes support for centralized setpoint control, readback of key electrical parameters, operational state control (On/Off/Standby), and fault status reporting to the machine control system. Local control capability shall be provided for commissioning and troubleshooting.

The main dipole power supply system shall be compatible with the ESR facility electrical and cooling infrastructure. The system shall interface to facility AC power distribution and to the facility cooling water system, with final interface requirements and capacities to be confirmed during detailed design and vendor implementation.

4.1.2 Electrical Architecture and Operating Configurations

Each of the three main dipole power supplies contributes a portion of the total output voltage required by the dipole magnet string. The series configuration allows the total system voltage to be distributed across multiple power supply units, reducing the voltage stress on any single supply and enabling compliance with the voltage-to-ground ratings of the dipole magnets. The electrical interconnection of the three supplies is designed such that the combined output behaves as a single DC source from the perspective of the magnet load.

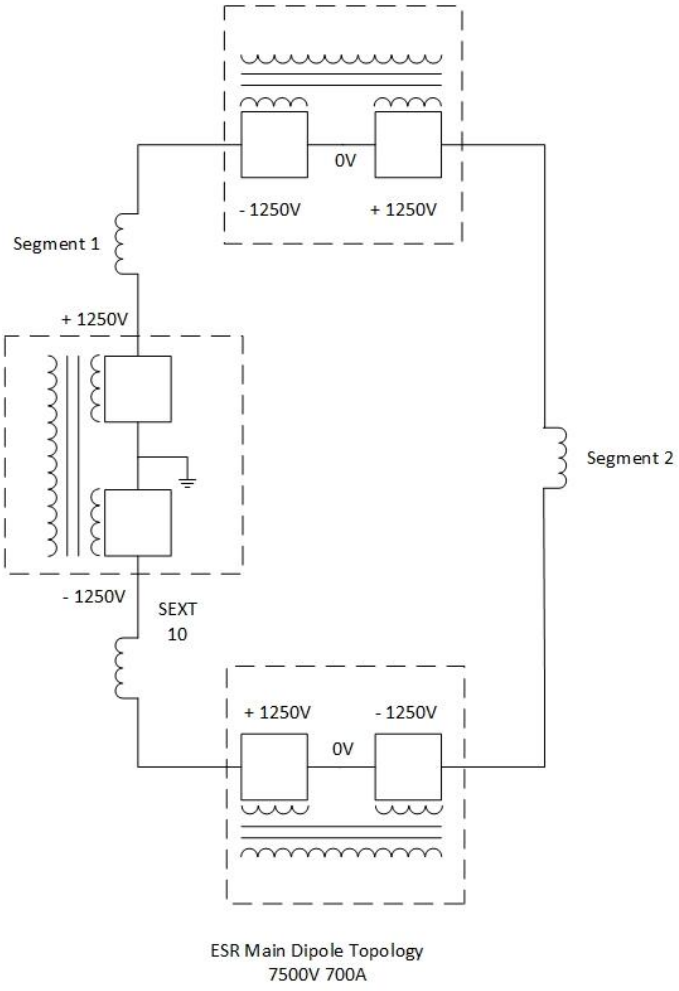


Figure 14. ESR Main Dipole Power Supply System Configuration

One of the three main dipole power supplies is configured with a ground reference to establish the system ground for the dipole circuit, while the remaining two power supplies operate with floating outputs relative to ground. This grounding configuration establishes defined reference points within the series string and is selected to control the maximum voltage-to-ground experienced by the dipole magnet circuit during normal operation and fault conditions.

To support stable series operation, one of the three power supplies is operated in current regulation mode (Master Supply) while the remaining two power supplies are operated in voltage regulation mode (Slave Supplies). This control configuration establishes a single current-regulating element

for the dipole string while the remaining supplies regulate their output voltages to support stable series operation and proper sharing of the total system voltage.

The main dipole power supply system shall provide interfaces to the ESR controls infrastructure to support remote command, monitoring, and interlock integration. The control implementation is expected to support high-precision current setpoint control and readback, system-level operational state control (On/Off/Standby), and fault status reporting to the machine control system. The specific implementation of the control interface, including the use of vendor-supplied control loops, BNL-developed controllers, PLC-based logic, or equivalent mechanisms, will be finalized during vendor selection and detailed design.

4.1.3 Voltage Balancing

The need to balance the voltages of the ESR main dipole power supplies arose from the realization that the magnet resistances were not uniformly distributed. This would generate an uneven workload seen by each of the three power supplies during worst-case operation at 18 GeV, due to unbalanced voltages.

Of the three power supplies that are all powered in series, the master supply center-tapped to true earth ground. Between the other two power supplies, a virtual ground exists that will, under ideal conditions, have a voltage measurement to ground of 0V. When the magnet loads are not balanced, the virtual grounds do not read zero. Therefore, careful assignment of magnet loads to specific supplies is required to maintain voltage balance across the ESR.

To identify how to best distribute the magnet loads, documentation of the resistance of each dipole magnet at each energy level was required, along with every magnet's unique S-coordinate for precise location. These measurements are crucial for determining which magnet and cable loads are assigned to each supply. The cable length formula described in section 3.2.1 is used to determine the cable runs for the ESR main dipole supply configuration.

Depending on the tap configurations of each dipole magnet, the resistance will be different at each energy level. The load parameters are provided to the EIC power supply group and a resistance per energy level is assigned to each magnet. Since they are technically in the IR6 subproject scope, the magnet types B2ER and D_SR are assumptions provided by the magnet group, as the magnets have not yet been designed.

Table 10. Main Dipole resistances per tap-configuration

Main Dipole			18 GeV Main		5 GeV Main		10 GeV Main	
Name	QTY	Model	Main Current (A)	Resistance (Ω)	Main Current (A)	Resistance (Ω)	Main Current (A)	Resistance (Ω)
B2ER	1	ir-td:550,B(T)=0.2087	391.40	0.05814	556.00	0.05814	214.50	0.05814
D13	2	ir-td:273,B(T)=0.0327	391.40	0.00310	556.00	0.00000	214.50	0.00310
	8	esr-td:273,B(T)=0.201	391.40	0.01698	556.00	0.00621	214.50	0.01698
	8	esr-td:273,B(T)=0.2081	391.40	0.01698	556.00	0.00621	214.50	0.01698
	352	esr-td:273,B(T)=0.2268	391.40	0.01876	556.00	0.00794	214.50	0.01876
	8	esr-td:273,B(T)=0.2456	391.40	0.02519	556.00	0.00794	214.50	0.02519
	144	esr-td:273,B(T)=0.2484	391.40	0.02519	556.00	0.00581	214.50	0.02519
	8	esr-td:273,B(T)=0.2526	391.40	0.02519	556.00	0.00794	214.50	0.02519
	4	ir-td:273,B(T)=0.2565	391.40	0.02713	556.00	0.00581	214.50	0.02713
	1	ir-td:273,B(T)=0.0692	391.40	0.02713	556.00	0.00581	214.50	0.02713
	5	ir-td:273,B(T)=0.2846	391.40	0.02713	556.00	0.00581	214.50	0.02713
	1	ir-td:273,B(T)=0.2837	391.40	0.02907	556.00	0.00581	214.50	0.02907
D2	1	ir-td:89,B(T)=0.1001	391.40	0.00194	556.00	0.00039	214.50	0.00194
	4	esr-td:89,B(T)=0.2011	391.40	0.00427	556.00	0.00427	214.50	0.00427
	4	esr-td:89,B(T)=0.2082	391.40	0.00427	556.00	0.00427	214.50	0.00427
	1	ir-td:89,B(T)=0.429	391.40	0.00427	556.00	0.00078	214.50	0.00427
	176	esr-td:89,B(T)=0.2269	391.40	0.00465	556.00	0.00465	214.50	0.00465
	4	esr-td:89,B(T)=0.2457	391.40	0.00504	556.00	0.00504	214.50	0.00504
	4	esr-td:89,B(T)=0.2527	391.40	0.00504	556.00	0.00504	214.50	0.00504
D_SR	11	ir-td:350,B(T)=0.3325	391.40	0.05814	556.00	0.05814	214.50	0.05814

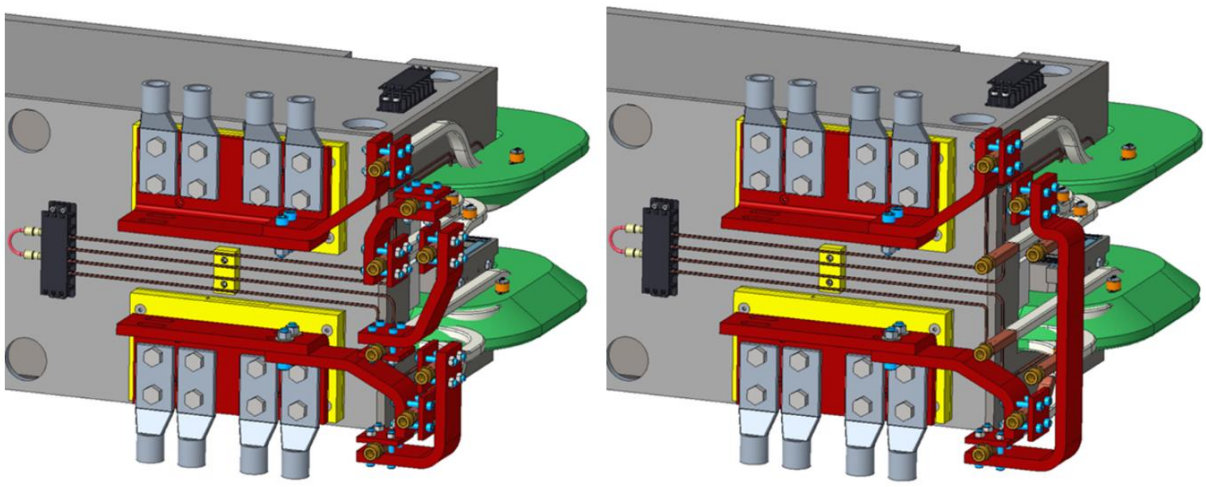


Figure 15. Example of a D13 magnet with 12-turn tap configuration (left) and 5-turn tap configuration (right)

Balancing the loads can be accomplished regardless of which building(s) the supplies are in; however, spreading the power supplies out around the ring will result in less cabling. The EIC power supply group worked closely with infrastructure to determine which buildings are best suited to house these supplies. Originally, the three supplies were given their own building and evenly spaced. Ultimately, the master supply was chosen to be housed in 1003A, while both slave supplies are located in 1009A. Buildings with provisions for DI water cooling influenced the decision, since this cooling method is required for the supplies. The slave supplies were placed in the same building to intentionally change the cable routing scheme to allow for certain magnets to be connected in series on the return path, helping to balance the loads.

The EIC power supply group developed a program to balance the voltages based on the resistances per energy level and the calculated cable resistances. The program required a specific magnet for where to begin the load for the first power supply. Keeping symmetry in mind, magnets es2-td315 and es3-td320 were chosen. Both magnets are adjacent to building 1003A, making them good candidates for where to begin the load of magnets for one power supply and where to terminate the load on another. The program uses a surface plot to visualize the balancing of the magnet resistances.

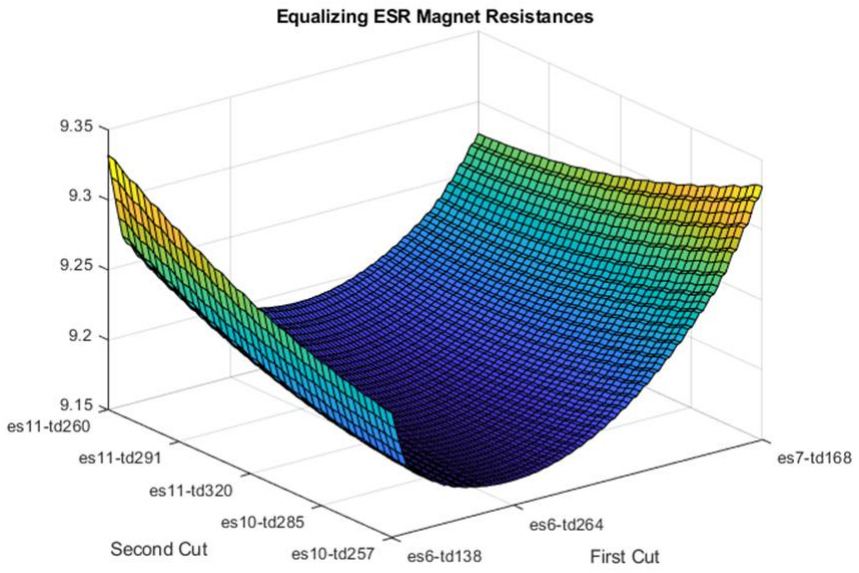


Figure 16. Surface plot of segment resistances

Figure 15 shows the first and last magnet in each segment, along with their S-coordinates. Then the total resistance of the segment is displayed, broken down by the total resistance of the magnets in the segment and the cable resistance.

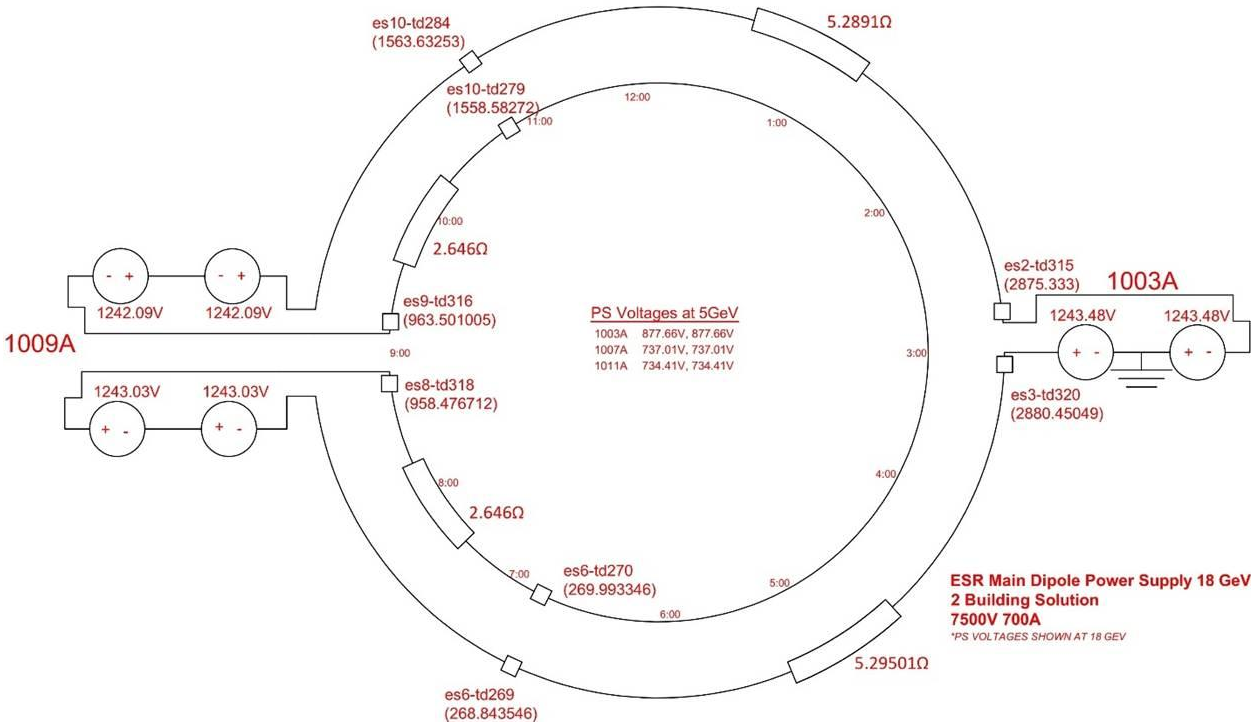


Figure 17. Voltage Balanced ESR Main Dipole Circuit (18 GeV)

The imbalance that exists between the power supplies during normal operation was quantified. At 18 GeV, the voltage imbalance was reduced to approximately 0.1% between the highest and lowest rated voltage supplies. This confirmed that the program did not make any errors when assigning the loads. The voltage imbalance is much higher at 5 GeV operation (about 20%). This is due to the magnet strings being balanced specifically for 18 GeV. The individual magnet resistances vary depending on the operating energy level. If the system were to be equalized and balanced at 5 GeV, there would be an imbalance at 18 GeV. Since the operating conditions are higher at 18 GeV, the choice was made to perform the balancing exercise at 18 GeV, as this will have the best effect on supply lifetime.

	Seg 1 18 GeV Ω	Seg 2 18 GeV Ω	Seg 3 18 GeV Ω	Seg 1 5 GeV Ω	Seg 2 5 GeV Ω	Seg 3 5 GeV Ω
Magnet Resistance	5.1763	5.0858	5.1654	2.5122	2.0019	2.0777
Cable Resistance	0.1187	0.2073	0.1237	0.1187	0.2073	0.1237
Cable+Magnet	5.2950	5.2931	5.2891	2.6309	2.2093	2.2015
Voltage	2,486.96	2,486.07	2,484.19	1,755.33	1,474.02	1,468.82
	18 GeV			5 GeV		
	% Imbalance:	0.112%		% Imbalance:	19.506%	

Figure 18. ESR Main Dipole Voltage Balancing Percent Imbalances at 18 GeV and 5 GeV

4.1.4 Main Dipole Supply Transmission Latency and Ground Fault Detection

The ESR main dipole control scheme uses a master-slave configuration in which one supply operates in current control while the other two operate in voltage control. Due to control system latency (~100 µs) and limited bandwidth (~1 kHz), the slave supplies lag the master during transients, creating temporary voltage mismatches. This behavior is especially important during

current ramps, where excessive ramp rates can lead to overshoot or voltage spikes due to the inductive nature of the load. The latency and ramp response analysis demonstrates that a 1-second or greater ramp rate is sufficient. A 60 second ramp-rate provides a safe operating margin, balancing system responsiveness with stability and protection against overvoltage conditions.

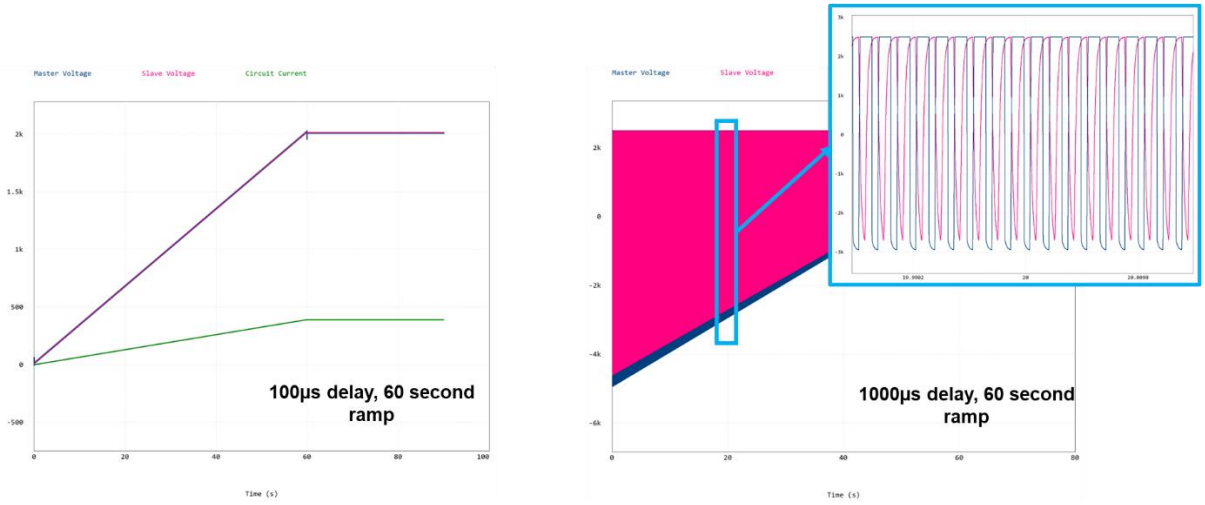


Figure 19. Effect of Transmission Latency on ESR Main Dipole Circuit

Building upon this analysis, focus is shifted to the ground fault detection scheme, which uses a center-tapped ground through a sense resistor to monitor leakage current. Under normal operation, only microamp-level leakage currents are present, but during a fault, current through the sense resistor increases significantly and is used to trigger protection mechanisms. The normal and fault block diagrams clearly show the difference in current paths and illustrate how fault conditions produce measurable signals that can be detected by the control system. This detection method allows for rapid identification and isolation of faults to protect both the power supplies and magnet string.

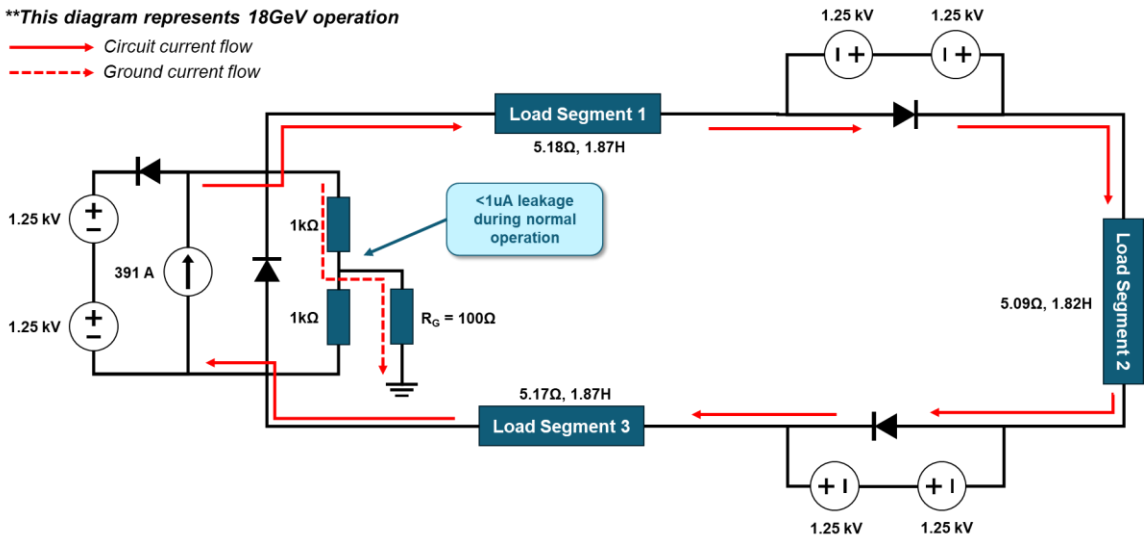


Figure 20. Block Diagram of ESR Main Dipole During Normal Operation

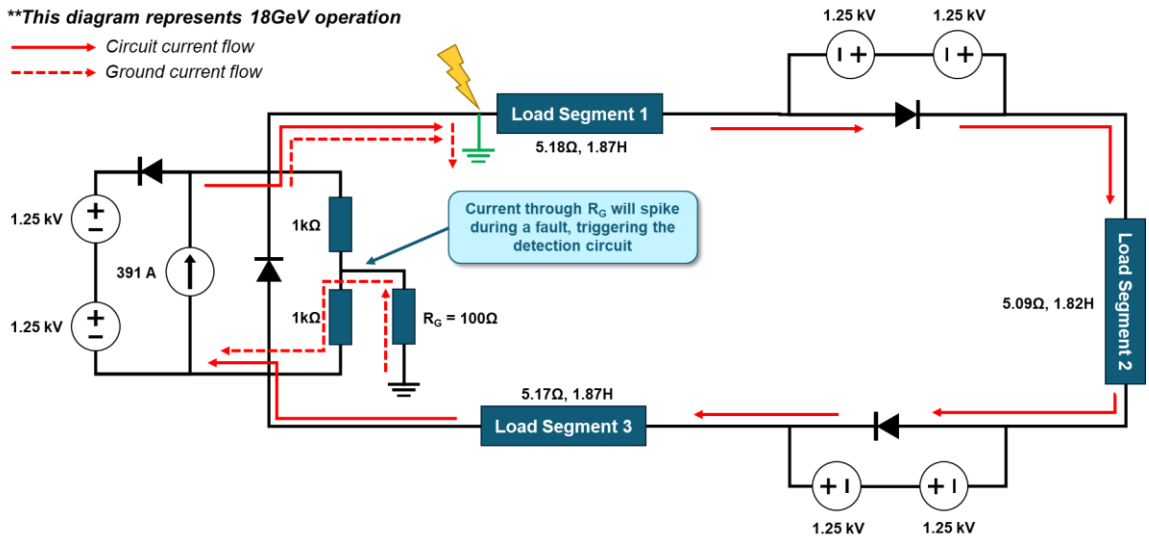


Figure 21. Block Diagram of ESR Main Dipole during Ground Fault Condition

To evaluate system behavior, a detailed simulation model was developed that includes the three power supplies, segmented magnet loads, and the full ground fault detection circuit. The model incorporates realistic elements such as control delays, bandwidth limitations, instrumentation amplifiers, and protection components like TVS diodes and fuse-based backup detection. The model diagram provides a system-level view of how these elements interact and enables simulation of various fault scenarios, including catastrophic shorts, insulation degradation, and delayed shutdown conditions. This modeling approach allows for validation of detection thresholds, timing, and component stress under different operating conditions.

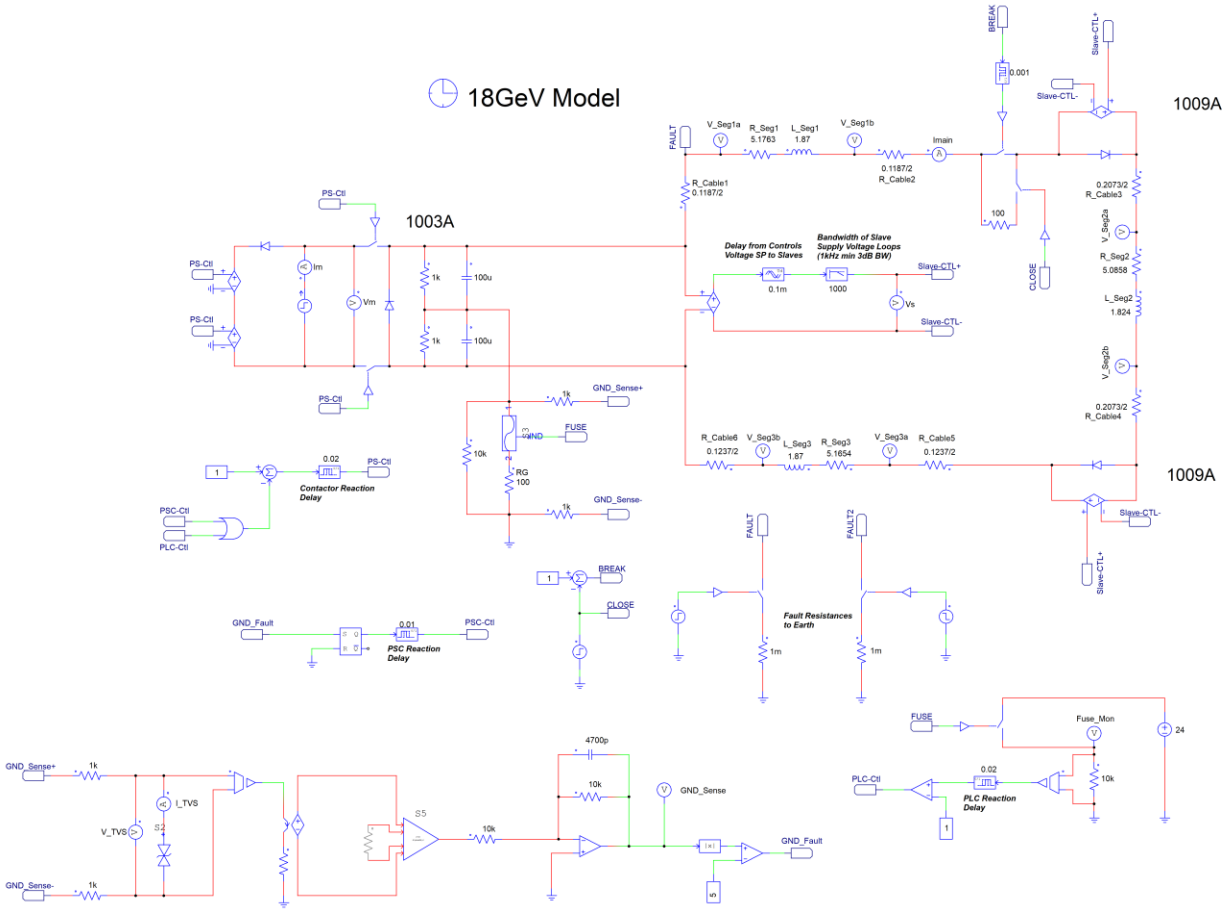


Figure 22. PSIM Model of ESR Main Dipole Circuit

Simulation results demonstrate that the primary detection system can identify faults and shut down the system within approximately 30ms, even for severe faults such as direct shorts to ground. In cases where the primary protection is disabled, a backup system using an indicator fuse and PLC interface successfully detects faults, though with longer response times. The results highlight system performance under both catastrophic and gradual fault conditions, including voltage, current, and energy dissipation in key components.

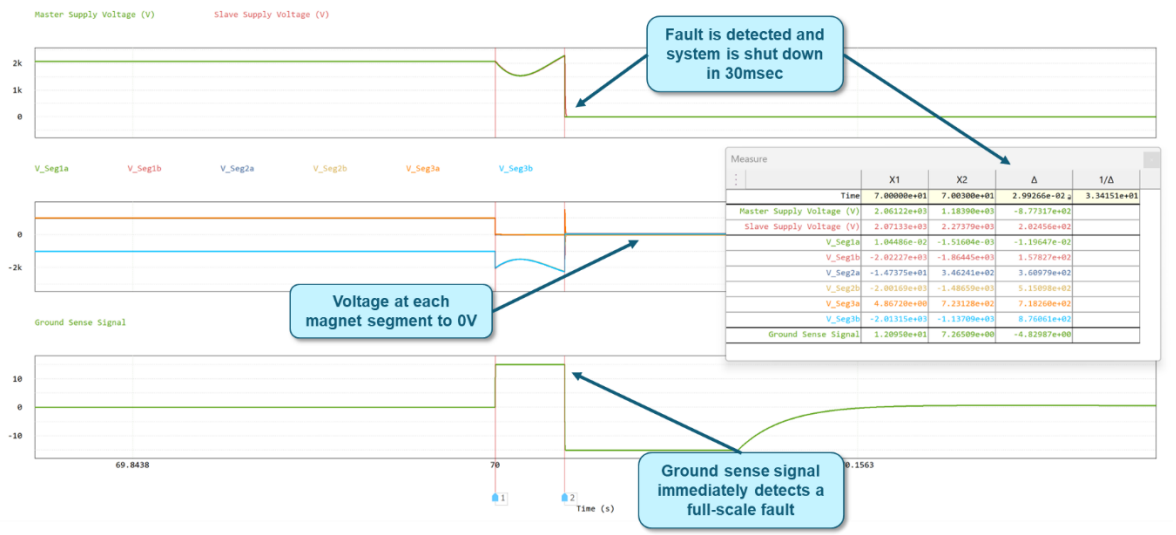


Figure 23. ESR main dipole simulation results from a direct short

In the ground fault detection analysis, the measurement resolution is evaluated using the least significant bit (LSB) of the PSC analog-to-digital converter (ADC) to determine the smallest detectable current. For an N-bit ADC with full-scale voltage V_{FS}, the voltage resolution is given by $\mathrm{LSB} = \mathrm{V_{FS}}/2^N$. The PSC employs a full-scale voltage of -10 to 10, or 20V. With a 16-bit ADC, this yields a very fine voltage resolution. For a typical sense resistor value of 100Ω the minimum detectable current is extremely small (well below the 10 ppm operating threshold) demonstrating that the PSC has sufficient resolution to reliably detect even very small ground fault currents. This confirms that the limiting factor in detection is not ADC resolution, but rather system noise and practical implementation constraints.

Overall, the analysis shows that while the center-tap resistor approach is effective, a simplified direct center-tap configuration can achieve similar detection performance while reducing continuous power dissipation, leading to a recommended design improvement for future implementation.

4.2 COTS Supplies for Quadrupoles, Sextupoles, and Dipole Trims

The ESR power supply system employs COTS unipolar switch-mode power supplies to support quadrupole, sextupole, and dipole trim magnets, selected for their ability to meet required current, voltage, ripple, and integration performance. Although these supplies operate in constant voltage mode, precise current regulation is achieved with the PSC using a closed-loop system with DCCT feedback, enabling high stability and accuracy suitable for operation. The different magnet families impose varying electrical demands, with quadrupoles requiring high current and tight stability, sextupoles operating across broader voltage ranges, and dipole trims requiring low current with high resolution for fine field adjustments.

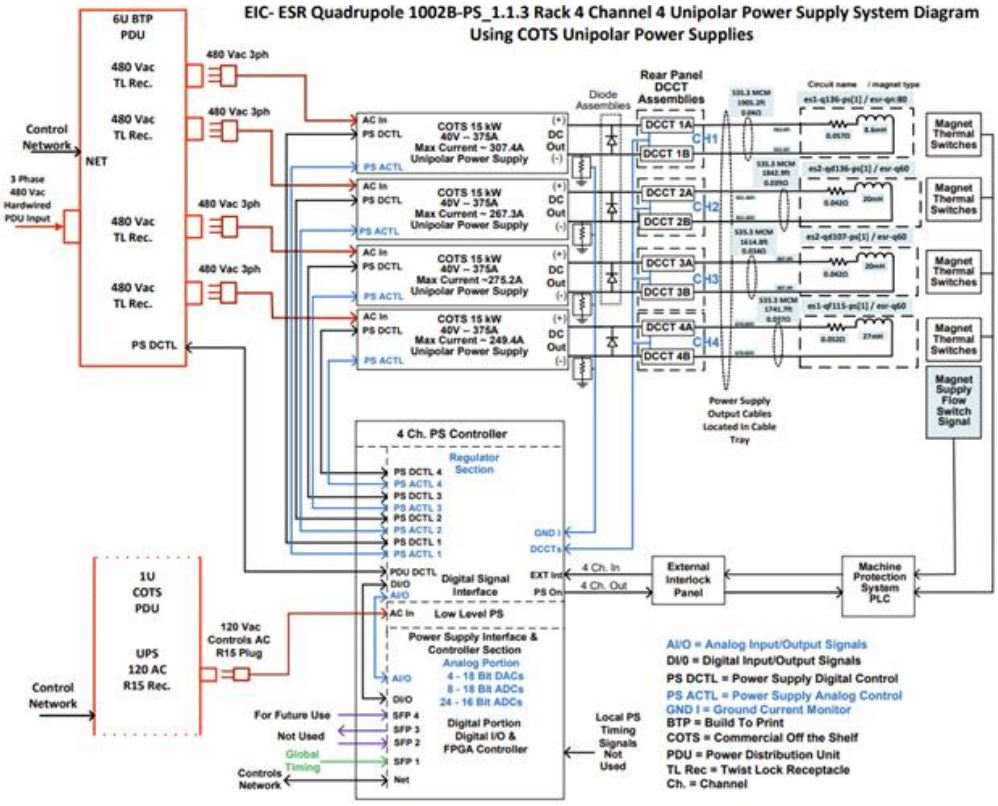


Figure 24. Single Unipolar Power Supply Rack Configuration

The system architecture supports a wide range of operating conditions and maintains strict ripple performance requirements to ensure beam stability. COTS supplies are integrated into coordinated multi-channel systems using PSCs, MCPCICs, and DCCTs, and can be configured in series or parallel arrangements to meet higher power demands. The architecture also supports flexible operation, particularly for sextupole systems that switch between high- and low-energy lattice configurations via link boxes. Overall, this approach provides a scalable and cost-effective solution that combines commercial hardware with precision external control to achieve the required performance across all ESR magnet systems.

4.2.1 Series and Parallel Power Supply Configurations

To satisfy the wide range of ESR magnet voltage and current requirements, COTS power supplies are configured using standardized series and parallel topologies that enable scalable performance while maintaining a consistent and maintainable architecture. In the ESR naming convention, the first number denotes the number of supplies in series (S) and the second denotes the number in parallel (P), such that a 1S2P configuration represents two supplies in parallel, while a 2S1P configuration represents two supplies in series. Series configurations are used when higher output voltage is required than a single supply can provide, with each unit operating in constant voltage mode and the total output equal to the sum of individual supply voltages; common examples include 2S1P and 4S1P arrangements. For higher current demands, supplies are connected in parallel, where each unit contributes a portion of the total current and coordinated load sharing is

required to prevent overstress; typical configurations include 1S2P, 1S3P, and 1S4P, which are widely used in quadrupole and sextupole systems.

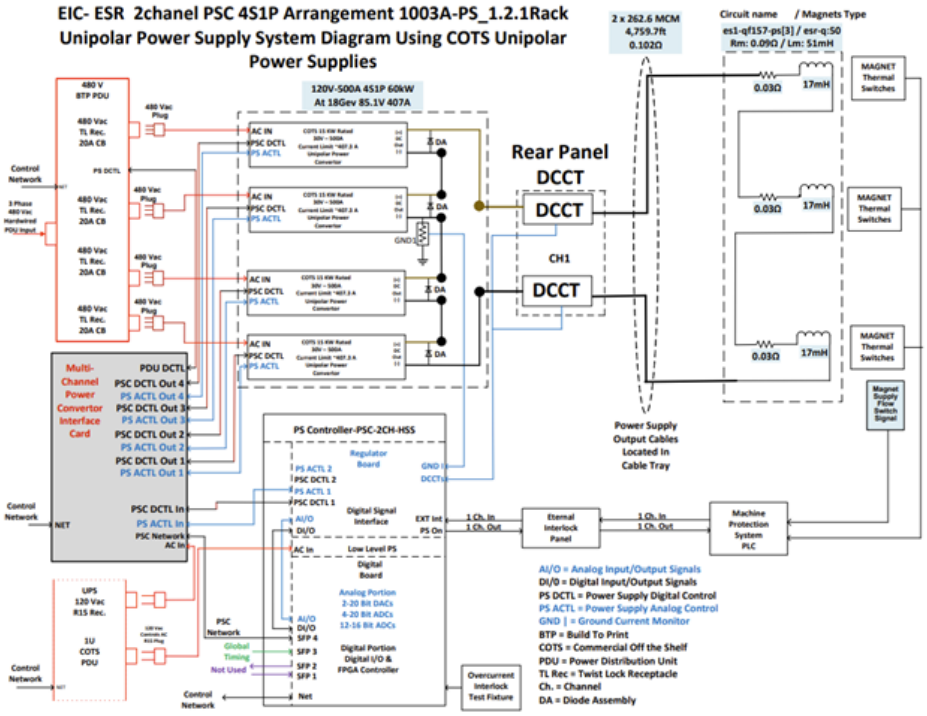


Figure 25. 4S1P Unipolar Power Supply Rack Configuration

All multi-supply configurations, whether series or parallel, require the use of the MCPCIC, while single power supply systems do not. The MCPCIC provides setpoint distribution, coordinated operation, current sharing for parallel systems, and overall stability for multi-supply performance. Following the latest lattice update, configuration constraints were introduced to simplify the system and improve reliability, limiting arrangements to a maximum of four power supplies and restricting configurations to either purely series or purely parallel topologies, with no mixed series-parallel combinations. In total, the ESR system includes 719 COTS power supplies, of which 234 are individually powered and 485 are used within 162 grouped arrangements. This standardized approach ensures consistent performance, scalability, and operational reliability across quadrupole, sextupole, and trim power supply systems.

Table 11. COTS Series and Parallel Configuration Summary

Configuration	Description	Number of Arrangements	Notes
1S2P	2 supplies in parallel	26	Current scaling
1S3P	3 supplies in parallel	5	Higher current demand
1S4P	4 supplies in parallel	12	Maximum parallel configuration
2S1P	2 supplies in series	53	Voltage scaling
4S1P	4 supplies in series	66	Maximum voltage configuration
Single PS	Individual supply (no grouping)	234	No MCPCIC required

In addition to rack system diagrams, highly detailed wiring diagrams have been produced. The wiring diagram serves as the foundational document for defining all internal rack interconnections, providing the complete electrical layout that is used by the mechanical design team to develop the 3D rack model, including detailed cable routing and length determination. It captures all critical connections within the rack, including PSC-to-power supply interfaces, DCCT feedback wiring, external interface connections, PDU AC distribution, and network/communication links. The diagram also specifies cable types and characteristics (such as 22 AWG multi-conductor control cables, shielded instrumentation cables, Ethernet/fiber communication lines, and grounding/monitoring connections) ensuring that all electrical and signal paths are clearly defined and standardized.

To minimize design effort and risk, the ESR system reuses proven cable assemblies from NSLS-II and ALS-U applications, maintaining the same cable types and connectors while only adjusting lengths to meet ESR-specific installation requirements. This standardization enables consistent fabrication, assembly, and verification processes across racks, significantly reducing engineering effort from approximately 150-200 hours per rack to just 3-5 hours (over a 95% reduction). The wiring design is replicated across 33 racks with only minor variations, primarily in DC output cabling to magnets, resulting in improved consistency, reduced procurement complexity, and lower installation risk while ensuring reliable system performance.

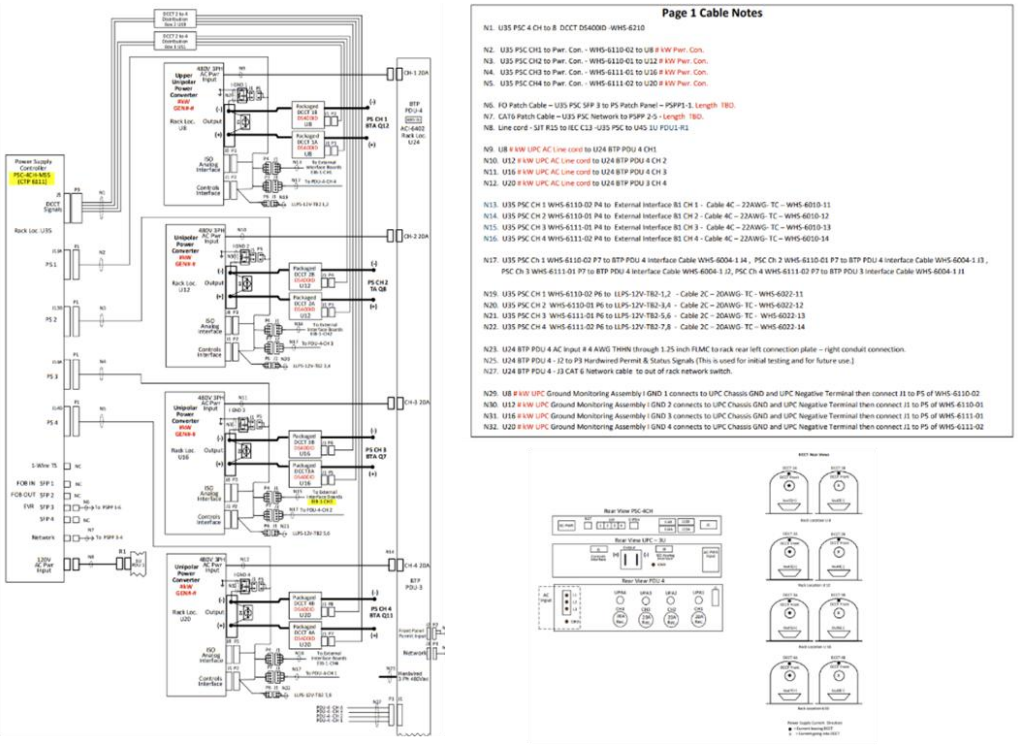


Figure 26. Interconnecting Wiring Block Diagram

3D rack models are used to provide a complete mechanical representation of the system, enabling precise equipment placement, cable routing, length extraction, and BOM generation to support assembly. Its use improves installation efficiency, cable management, thermal performance, and serviceability while reducing wiring errors and troubleshooting time.

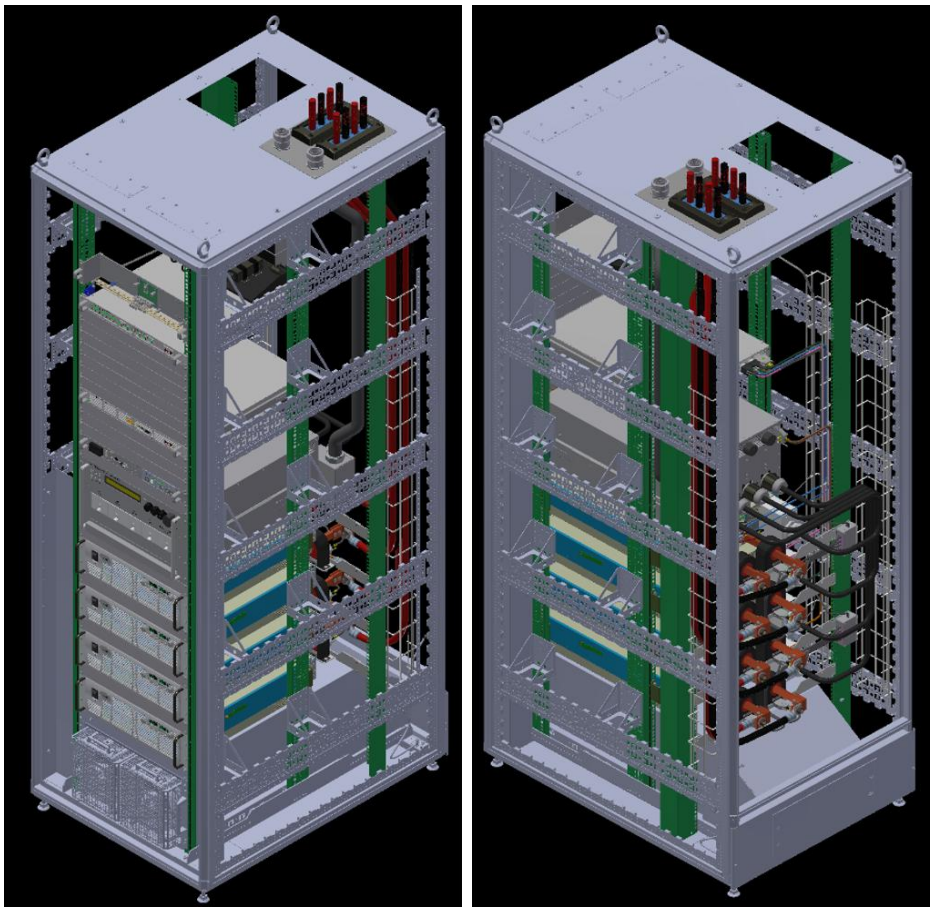


Figure 27. 3D Rack Model

4.2.2 COTS Supply Low Current Operation

EIC operation spans three energy levels, each requiring different operating currents from the supply. The difference between the highest and lowest current can reach on the order of 300 A. All power supplies are selected to meet the highest required current, but operating a supply far below its nominal range may impact regulation performance, particularly with respect to ripple.

Based on discussions with vendors, a minimum operating threshold of 5% of the maximum output voltage has been established. This condition is evaluated per every circuit and any power supply operating below this threshold is flagged for further review with the physics group. In the current design, only five strings are flagged and under investigation.

The mitigation strategies being discussed are the addition of a series resistive load to increase the operating voltage or selecting a lower rated power supply for the lower energy operation and switching between the supplies.

4.2.3 COTS Supply Ground Fault Detection

Ground fault detection for COTS-based power supply systems is implemented using a dedicated ground sense resistor that is directly monitored by the PSC. A resistive path to ground is established so that any leakage or fault current flows through the sense resistor, allowing the PSC to measure the resulting voltage using a precision differential amplifier. Because the measured voltage is directly proportional to the ground fault current, this method provides a simple, robust, and deterministic approach to fault detection. The grounding resistor value is selected as a balance between limiting fault current, which favors higher resistance, and maintaining sufficient detection sensitivity, which favors lower resistance.

The most challenging detection condition occurs when circuit resistance and inductance are both high, resulting in minimal ground fault current and therefore the smallest measurable signal. To address this, a nominal resistor value on the order of 100 Ω is chosen to ensure detectable signal levels while still limiting fault current to safe levels and remaining compatible with PSC measurement resolution and noise constraints. The PSC continuously monitors the ground fault signal in real time, compares it against configurable thresholds, and initiates a fast, deterministic shutdown when abnormal conditions are detected. Because this protection is implemented locally within the PSC, it provides low-latency response independent of network delays, ensuring reliable protection of both the power supplies and connected magnets.

At the system level, the grounding scheme maintains a single defined ground reference, while overall detection sensitivity is influenced by factors such as the sense resistor value, amplifier gain, noise filtering, and PSC ADC resolution. The effectiveness of the detection approach is validated through controlled fault injection using known resistances, allowing verification of detection thresholds and system response under representative operating conditions.

4.2.4 Sextupole Family Link Box Design

The ESR Sextupole Link Box is designed to allow for an easy transition between sextupole operating conditions. During 18 GeV operation, the sextupole families in the arcs will operate in the 90-degree configuration and during 10 and 5 GeV, they will operate in the 60-degree configuration. Magnet families will be permanently wired in the ring, so the link box is implemented to allow for different families to be connected to their appropriate power supplies. Each of the six new power supply buildings will contain two link boxes: one for defocusing sextupole magnets and another for focusing sextupole magnets.

Link box configuration diagrams are developed for both high and low energy configurations for all the different arcs for both focusing and defocusing sextupoles. These drawings are also intended to serve as a schematic guide for technicians responsible for reconfiguring the links when switching between high and low energy operations.

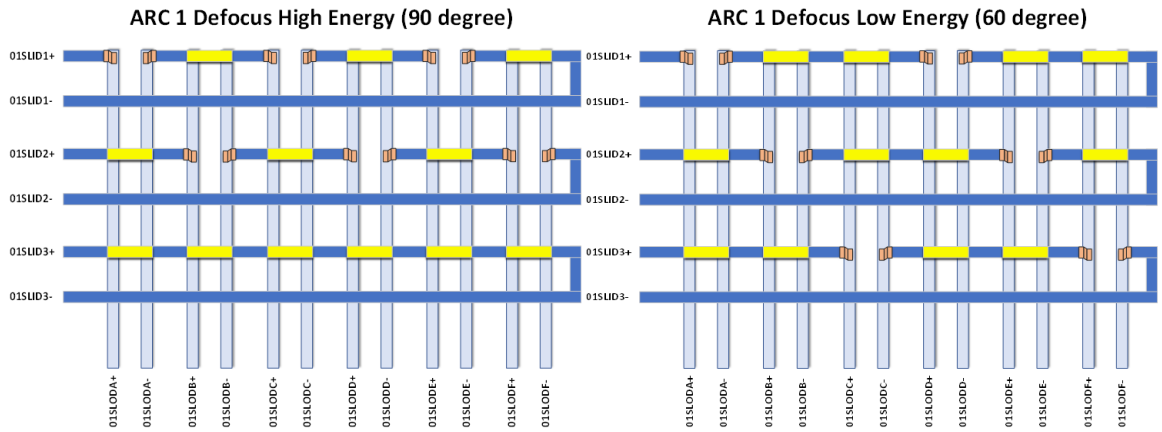


Figure 28. Example of Swapping between Configurations via Link box

The link boxes are made up of three integral parts: a 'Z' bracket, a Horizontal Link, and the bus work. These components are fabricated from oxygen-free copper due to its anti-corrosion properties. Each component has a different purpose:

- **Bus work**: The bus work connects directly to the power supplies, denoted as PS1+ and PS2+ in Figure 23. It then extends to the individual magnet families, providing a supply and a return path for power.
- **Z Bracket**: This component mates the bus bar from the power supply legs to the bus bars connected to the supply and return legs of the magnet family groups.
- **Horizontal Link**: This link is used to bypass magnet families that are not powered by a specific power supply, allowing another power supply to pick them up via the Z brackets.



Figure 29. Link box components. From left to right: Bus work, Z-bracket, Horizontal Link

To ensure the components can safely carry the required currents, their dimensions were calculated. The sextupole magnets have a maximum current of 160A. With a 20% margin, the maximum current is 192A. The power supplies for these magnets are specified for a current of 200A. The

bus work and links were sized based on a cross-sectional area of 1000A/in² for the main bus work and an area of 250A/in² for overlapping sections. These calculations were based on the maximum power supply current of 200A.

Based on the 535.5 MCM cable and the corresponding cable lugs, which are approximately 2 inches wide, the bus work width is chosen to be least 3 inches to allow for extra space. Using the 1000A/in² rule for a 200A current, the required cross-sectional area for the bus work is 0.2 in². With a 3-inch width, this would require a thickness of only 0.067 inches, which is too thin to securely mount the lugs. To be safe, a bus work thickness of ½ inch is used (same as used in existing link boxes in RHIC). This provides a cross-sectional area of 1.5 in², a margin of 650% over the required 0.2 in².

4.2.5 COTS Supply Testing Results

Comprehensive testing has been performed to evaluate the ripple performance and overall suitability of candidate COTS power supplies for use in the ESR system, combining both vendor-provided validation and in-house verification. Potential vendors conducted ripple testing to demonstrate compliance with ESR requirements, confirming that selected units can meet specifications without additional external filtering. A key observation from this testing is that operation in constant current (CC) mode produces significantly higher ripple compared to constant voltage (CV) mode. As a result, the ESR architecture operates COTS supplies in CV mode while delegating precise current regulation to the external current loop in the PSC. Vendor results indicate that at least one candidate has successfully met all ripple requirements and completed full validation.

Independent verification is performed through in-house testing using a controlled and repeatable setup designed to ensure fair comparison across multiple vendors. Testing is conducted on three candidate power supplies under identical conditions, including the same magnet configuration (Q50 quadrupole equivalent), cabling, instrumentation, and operating parameters. High-resolution time-domain data is acquired using a Tektronix 12-bit Series 4 oscilloscope and processed using a custom MATLAB workflow. This analysis includes time-domain ripple evaluation, voltage and current FFT spectrum generation, and band-limited RMS ripple calculations, providing consistent, repeatable, and frequency-resolved characterization of each unit's performance.

Ripple measurements are taken directly at the power supply output while driving a representative inductive magnet load, which is critical for capturing realistic ESR operating behavior. The test setup includes a COTS power supply operating in CV mode, a Q50 magnet equivalent load (17mH, 30mΩ), and high-bandwidth voltage measurements across the load, with optional current validation. Operating conditions include approximately 10 V and 350 A, with a ripple requirement of 15 ppm over the 0–1 kHz range. The MATLAB-based analysis converts measured voltage ripple to current ripple, ensuring accurate representation of actual magnet performance.

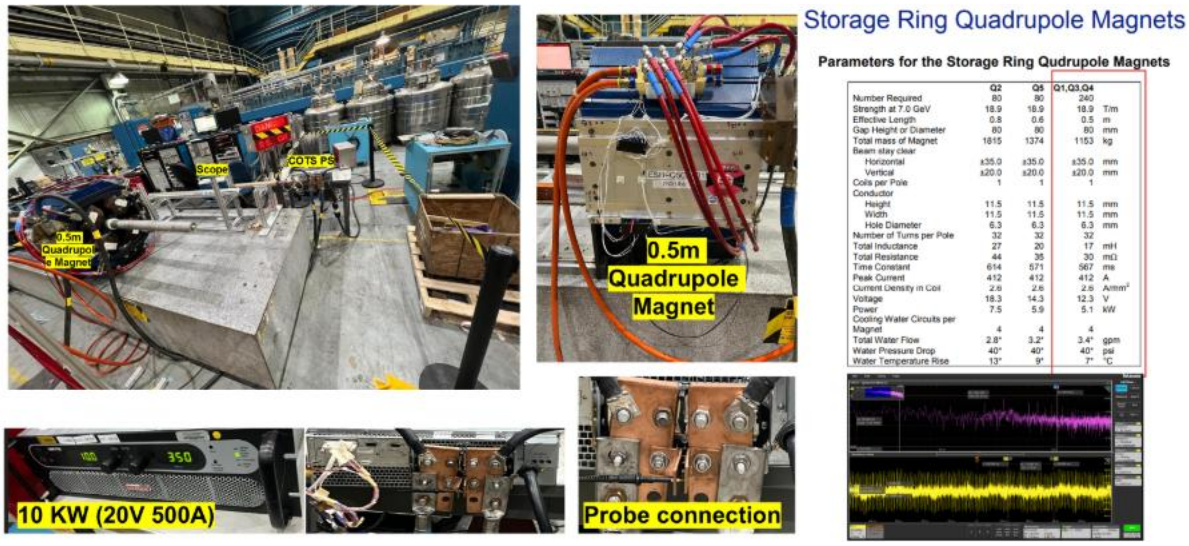


Figure 30. In-house Ripple Testing with Q50 Equivalent Magnet

Measured results demonstrate that current ripple within the 0-1 kHz band meets ESR requirements, while higher-frequency components are significantly attenuated by the magnet's inductive impedance. This confirms that the magnet itself plays a dominant role in filtering ripple and that voltage ripple from the power supply is effectively translated into acceptable current ripple through the system impedance. Comparative testing across vendors is ongoing under identical conditions, enabling direct performance benchmarking. Final selection will be based on ripple performance, stability, and compatibility with the overall ESR system architecture.

An ACL is implemented to ensure that all procured COTS power supplies meet ESR performance requirements through a structured and traceable validation process. The ACL defines key parameters including electrical performance metrics such as ripple, stability, and accuracy, as well as test procedures, measurement methods, acceptance thresholds, and documentation requirements. Verification is carried out in a staged approach beginning with vendor qualification testing to confirm baseline performance, followed by incoming bench-level acceptance testing of delivered units, system integration testing with magnet loads and PSC control, and finally full system validation under operational conditions. This progressive methodology ensures that performance is verified at each stage before deployment, reducing risk and ensuring consistency across all units.

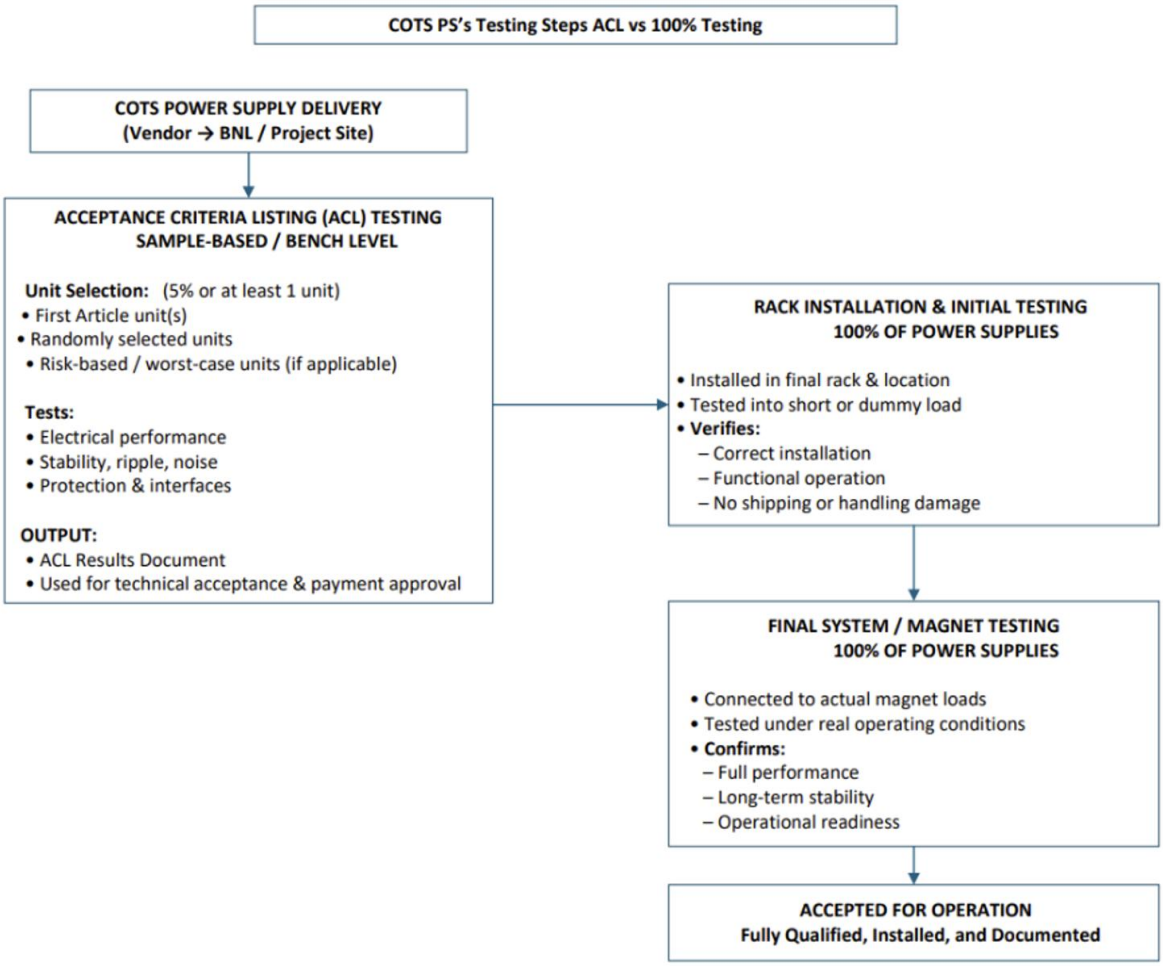


Figure 31. COTS Testing Phases

Ripple and stability are evaluated separately as part of the ESR validation philosophy to isolate power supply performance from system-level effects. Ripple is first measured at the power supply level under controlled conditions to confirm compliance with ESR specifications. Once validated, the power supply is integrated into the full system, where stability is assessed as a function of the complete closed-loop operation, including PSC control, DCCT feedback, and environmental influences. This approach ensures that individual power supply performance is independently verified while also confirming that the integrated system behaves as expected under realistic operating conditions.

Testing results across vendor evaluations and in-house verification demonstrate that COTS power supplies are capable of meeting ESR ripple requirements without additional filtering. Standardized measurement methods, including high-resolution oscilloscope acquisition and MATLAB-based FFT analysis, provide accurate and repeatable characterization of performance. Comparative testing across multiple vendors under identical conditions enables direct benchmarking, with at least one vendor demonstrating full compliance. The ACL-driven process ensures that validation

progresses from bench-level testing through full system verification, supporting reliable integration and consistent performance across the ESR power supply system.

Table 12. COTS Supply Testing Categories

Test Category	Description	Outcome
Vendor Testing	Multi-configuration ripple evaluation	Demonstrated compliance capability
In-house Lab Testing	Q50 magnet-based system testing	Validated under real operating conditions
Measurement Method	Tektronix 12-bit oscilloscope + MATLAB FFT	High accuracy and repeatability
Ripple Performance	Current ripple (ppm RMS, band-limited)	Meets ESR ripple requirements
Comparison Testing	Evaluation across three potential vendors	One vendor fully compliant
ACL Verification	Structured validation process	Bench → Rack → System verification completed

4.3 BTP Bipolar Power Supplies

The ESR power supply system requires two unique BTP bipolar power supplies. All correctors will be powered by a 2-channel bipolar power converter unit that is modeled after a proven design from NSLS-II. The supply is compact, efficient, and designed to seamlessly integrate with the other BTP equipment from NSLS-II, such as the PSC and the DCCT chassis. *Electron Storage Ring Corrector Power Supply Design Report* is a full report on the design and testing of the ESR Corrector BTP BPC.

Additionally, some of the dipole trim circuits are required by physics to operate at or below 300mA operating current. This super low current led the EIC power supply team to come up with a design for a 4-channel BTP bipolar power converter.

4.3.1 NSLS-II BTP Bipolar Power Converter

There are seven different BPC models that have been developed by the NSLS-II electrical engineering group. One of the models, BPC-2CH-S-16V-35A, is a 560W dual channel power converter, built into a 1U chassis. For EIC, the basis of this model will be redesigned to fit EIC needs. Ultimately, both the horizontal and vertical corrector magnets will be powered by a 400W BPC designed to provide 40V and 10A. Before detailing the design modifications, it is important to understand the base design of the NSLS-II model.

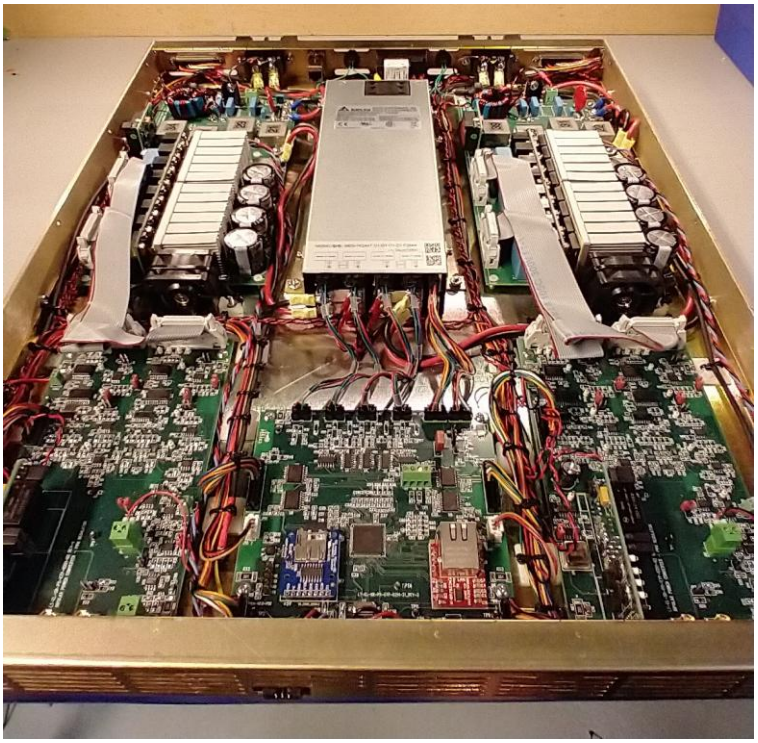


Figure 32. NSLS-II BPC-2CH-S-16V-35A

The 16V-35A model features a front-end AC-DC power converter that provides 24V DC buses to each channel, which features a power amplifier board and a Pulse Width Modulation (PWM) regulator board. A single control board is designed to monitor/control both channels.

The front-end power converter is a COTS configurable medical grade power supply. The device fits in a 1U chassis and is Underwriters Laboratories (UL) recognized. The input to the supply is two-phase 208VAC and connects to the BPC via a 208VAC-10A double fused power entry module. The supply is configured into two isolated 1kW triple slot modules, each providing 24V DC output. The unit has an efficiency up to 93% and a power factor of 0.95.

The BPC design utilizes a single control board for both channels. The 16 MHz, 8-bit microcontroller in use is the Atmega2560-16AU. The control board provides both over current and over temperature interlocks. Analog hall sensors monitor the converter's output current and 10-bit analog-to-digital converters (ADCs) on the control board are used to digitally compare against a preset over current limit. 1-wire temperature sensors are mounted on the ends of heatsinks mounted to the SiCFETs on the power amplifier board. The temperature sensors provide thermal feedback to the control board, which compares against a preset over temperature limit. The thermal feedback is also used to control cooling fan speeds. The fans are DC with PWM control capabilities.

The controller board also connects to the PSC, providing isolated digital input-output data for housekeeping. The controller board utilizes serial peripheral interface (SPI) communication at 8 MHz for transferring housekeeping data to the PSC. An SD card module holds bootup configuration data, such as the IP address, MAC address, 1-wire temperature sensor unique identifiers, and hall sensor gains. The controller board also utilizes 400 kHz I^2C communication

for retrieving housekeeping data from the front-end power converter, as well as the 1-wire temperature sensors. The board is under watchdog timer supervision, and the C code is developed with that standard Arduino IDE with Arduino libraries.

The BPC features two PWM-regulator boards (one per channel). Each regulator provides analog voltage feedback, interleaved H-bridge control, and hall sensor current feedback for current sharing. The interleaved PWM signals operate at 250kHz and are 90° out of phase. The timing jitter is as low as 5 nano-seconds peak-to-peak. Half bridge dead time is built in and adjustable. The voltage loop for the power supply setpoint and feedback control is present on the PWM board as well.

The last stage of the BPC is the power amplifier and filtering stage. There are two power amplifier boards (one per channel) and each board features two interleaved H-bridges, constructed of SiCFETs with 30 milli-Ohm drain to source resistances. The SiCFETs are cooled by PWM controlled DC fans, which push air through mounted COTS heatsinks. A single bridge output switching frequency is 500 kHz, so the output after interleaving is 1 MHz switching frequency. Isolated gate drivers are built into daughter boards. The hall sensors measure the current of each half bridge and provide feedback to the PWM board. Low frequency filtering is present on the output of the power amplifier board, including custom common mode chokes and inductors hand measured and matched to 1%. A high frequency output filter board is connected in parallel with the output of the power amplifier board and the output of the power converter. Transient voltage suppression (TVS) diodes are present on the power amplifier and output filter board.

4.3.2 BTP Bipolar Power Converter for ESR Correctors

To fit ESR needs, the BPC-2CH-S-16V-35A converter is modified to a BPC-2CH-S-40V-10A converter and design upgrades are made based on lessons learned from ALS-U production testing. The ESR design will still be a 1U two channel device. The increase in voltage requires the front-end power converter to be changed and the higher voltage DC bus has a downstream effect on the rest of the supply. All board and chassis components are examined and modeled in simulation software. A concept block diagram of the BPC, with an increased DC bus voltage is shown below.

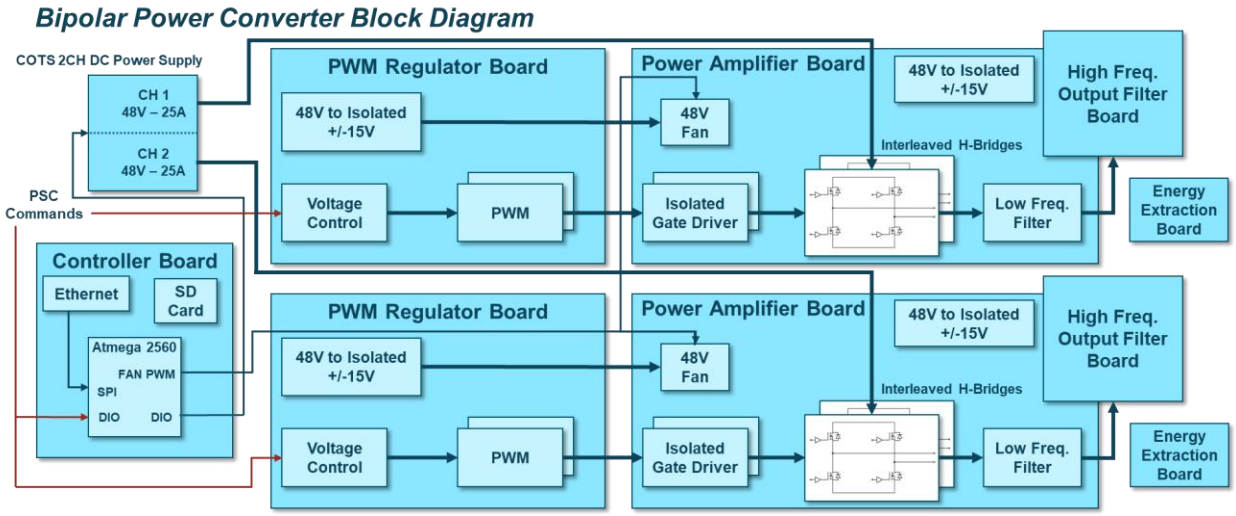


Figure 33. ESR Corrector BTP BPC Block Diagram

The ESR Corrector BPC is modeled to ensure proper functionality when powering the ESR corrector magnet loads. The model features a 25A current source, voltage limited to 48V DC. This power source is fed into an array of capacitors and resistors that matches the components on the power amplifier board. Next, the DC bus is passed on to interleaved H-bridges. The H-bridge switches are modeled as the SiCFETs present on the power amplifier board. A parameter file is used to fill in values directly from the real-world component's data sheet. The interleaved H-bridge output then feeds into a common mode choke modeled to represent the hand-wound choke on the power amplifier board. Lastly, the low frequency filter stage and high frequency output filter board components are modeled in parallel with the common mode choke and the load. The maximum load is entered for both vertical and horizontal correctors and the outputs studied.

The H-bridges are PWM controlled at 2-phase 0°, 90° 250 kHz switching frequency, with dead band time. This is accomplished with the modeled voltage feedback circuit and comparator models. The voltage feedback is modeled as resistive dividers on both legs of the output, which are passed on to a sub-circuit modeled to represent the voltage loop on the PWM boards. The voltage control is updated to 1V input equal to 4V output. The increase in voltage also required the TVS diodes to be sized up, which are also modeled as sub circuits. The power converter model features a soft ground on the output, which matches the real BPC design.

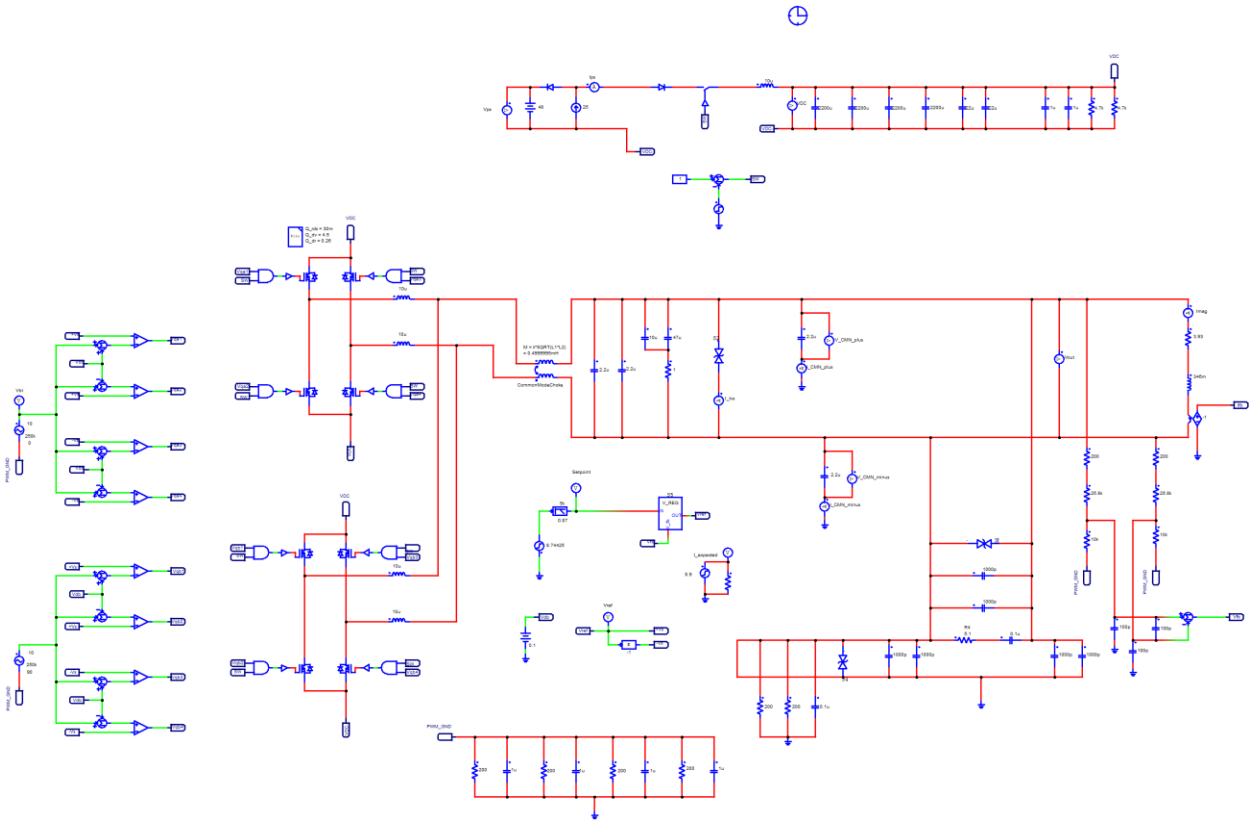


Figure 34. Circuit Model of BPC-2CH-S-40V-10A

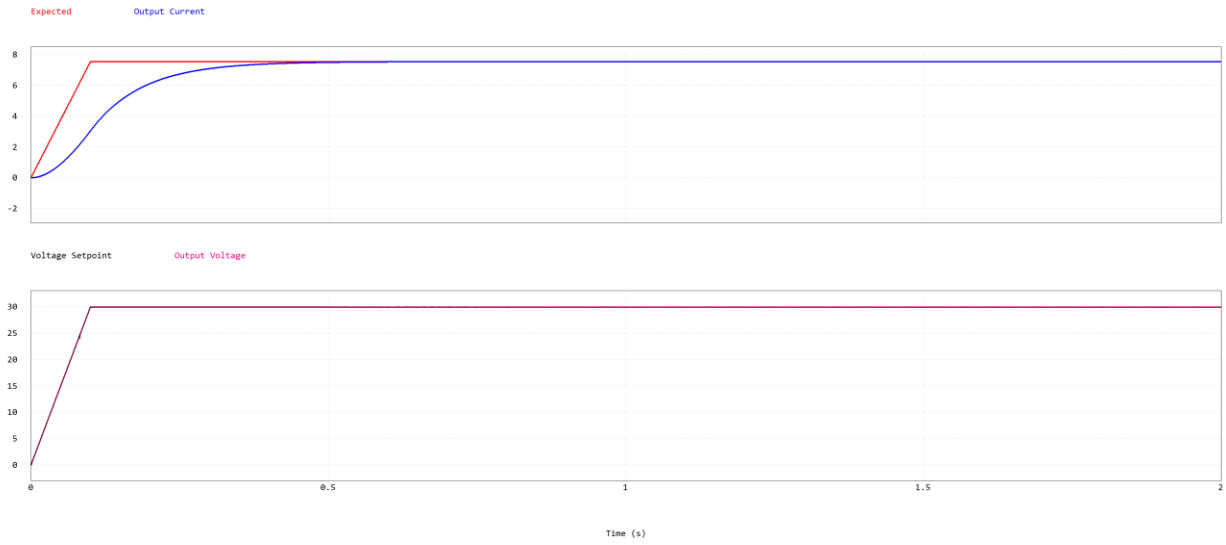


Figure 35. Output Voltage and Current of BPC Simulation (Vertical Corrector Load)

Increasing the DC bus from 24V to 48V requires all bus voltage exposed components to be analyzed. The electrical parameters of the components are changed, but all physical properties maintained to avoid any redesigning of the printed circuit board (PCB) layouts. All modifications to the BPC design are documented in official drawings and entered into the EIC design room.

The reverse diodes present on the power amplifier board H-bridges were reselected for higher reverse voltage. On the PWM board, the voltage feedback resistors were modified to provide the new voltage feedback ratio. The input voltage range of the DC-DC converters on the power amplifier and PWM power daughter boards were increased, and the same component series was maintained. The voltage rating of tantalum capacitors on these daughter boards also needed to be increased. Lastly, the TVS diodes are selected to clamp at higher voltages, to enable higher voltage output while still providing protection against transients. The transient effects are modeled and studied to select the best TVS diode.

The most significant change in the design is to the front-end power converter. The triple slot modules are modified to 48V-25A outputs. Additionally, the increase in DC bus voltage requires a new cooling fan to be selected, while maintaining the PWM control feature. This is challenging due to the tight space constraints and limited fan availability; however, Orion and Delta manufacturers produce a DC cooling fan of the same size, with very similar features. Since the Orion fan is more readily available, it is chosen for the design.

The original BPC design features over current and over temperature protection, but no direct over voltage protection. Although the PSC will protect the power supply against over voltage, the power supply should be able to protect itself. Therefore, upgrades to the original designs were implemented.

The PWM board already has circuitry in place to provide +/-10V analog feedback to the PSC, representing the output voltage. The controller board can receive analog input signals with a range of 0-5V, so a circuit that divides the +/-10V signal by four and adds 2.5V is required. This is accomplished with a simple dual-op amp circuit. The circuit is added to the PWM board and the harness between the PWM board and controller board is modified to provide the controller board with the new analog signal. The controller board code is modified to allow for an over voltage limit to be set, and the supply will now trip if this limit is exceeded. The controller board can respond to a fault condition in approximately 20 micro-seconds.

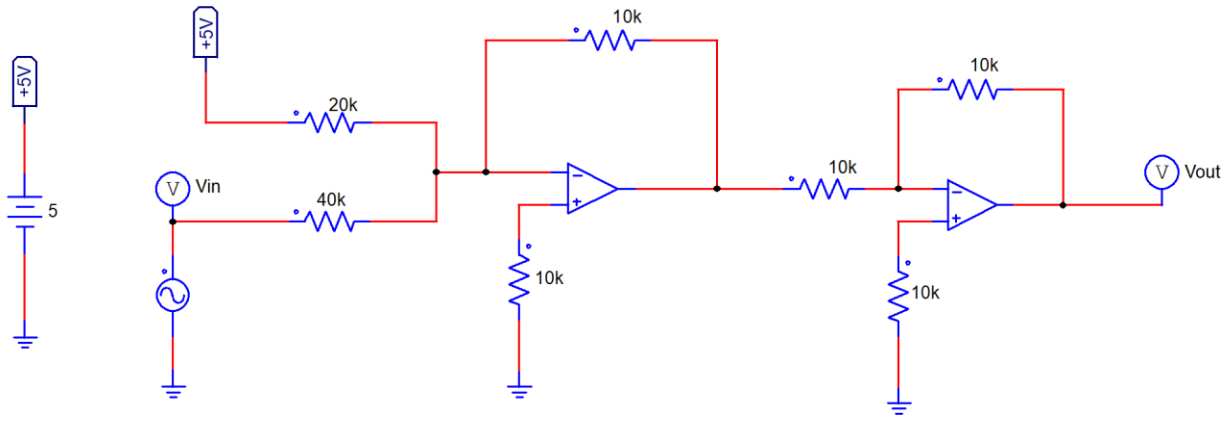


Figure 36. Output Voltage Feedback to Controller Board Circuit

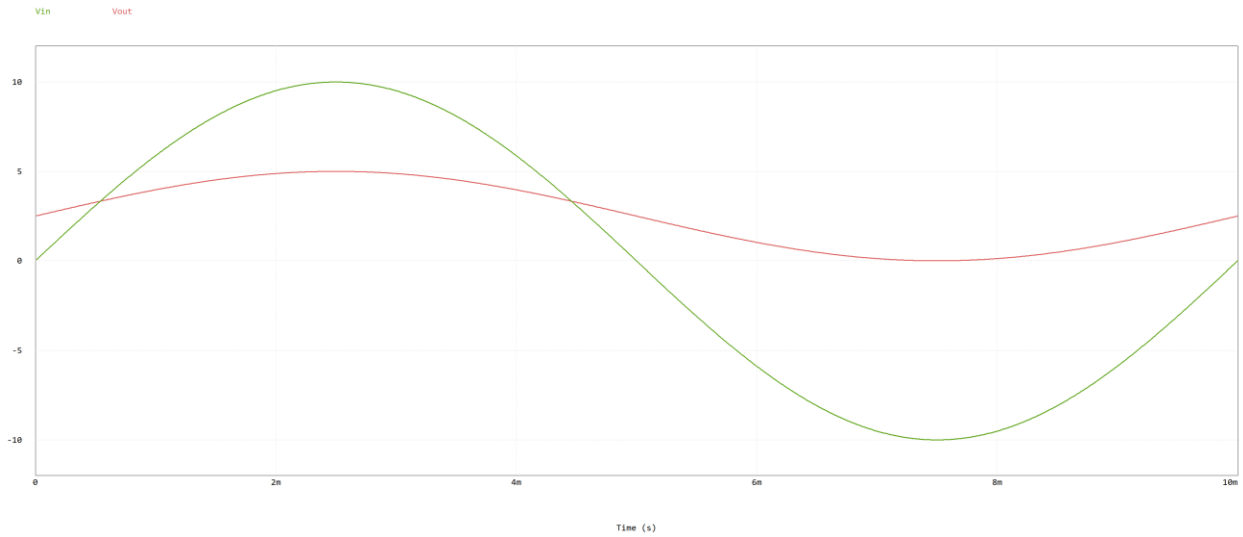


Figure 37. Conversion of +/-10V signal to 0-5V

The BTP converters are designed to interface with the other BTP and COTS equipment that is going to be used across all of ESR. This allows for efficient and compact rack solutions in the service buildings.

Two BTP dual channel power converters will be controlled by a single four channel PSC. The PSC will monitor status and detect fault conditions. The two BPCs are powered by a 0U COTS PDU, which provides multiple two phase 208VAC output channels from a single three-phase 208VAC input. A four channel DCCT chassis will be mounted in the back of the rack. The DCCT chassis is 2U and is designed to align with the two 1U BPC outputs, which allows for cable or bus work to pass through the DCCTs. This system allows four magnets to be powered by a total of 3U of occupied rack space. Additional equipment includes a 1U PDU for powering the PSC and an external interlock panel that interfaces with the machine protection system and thermal switches on the magnets. This equipment is present in all ESR power systems.

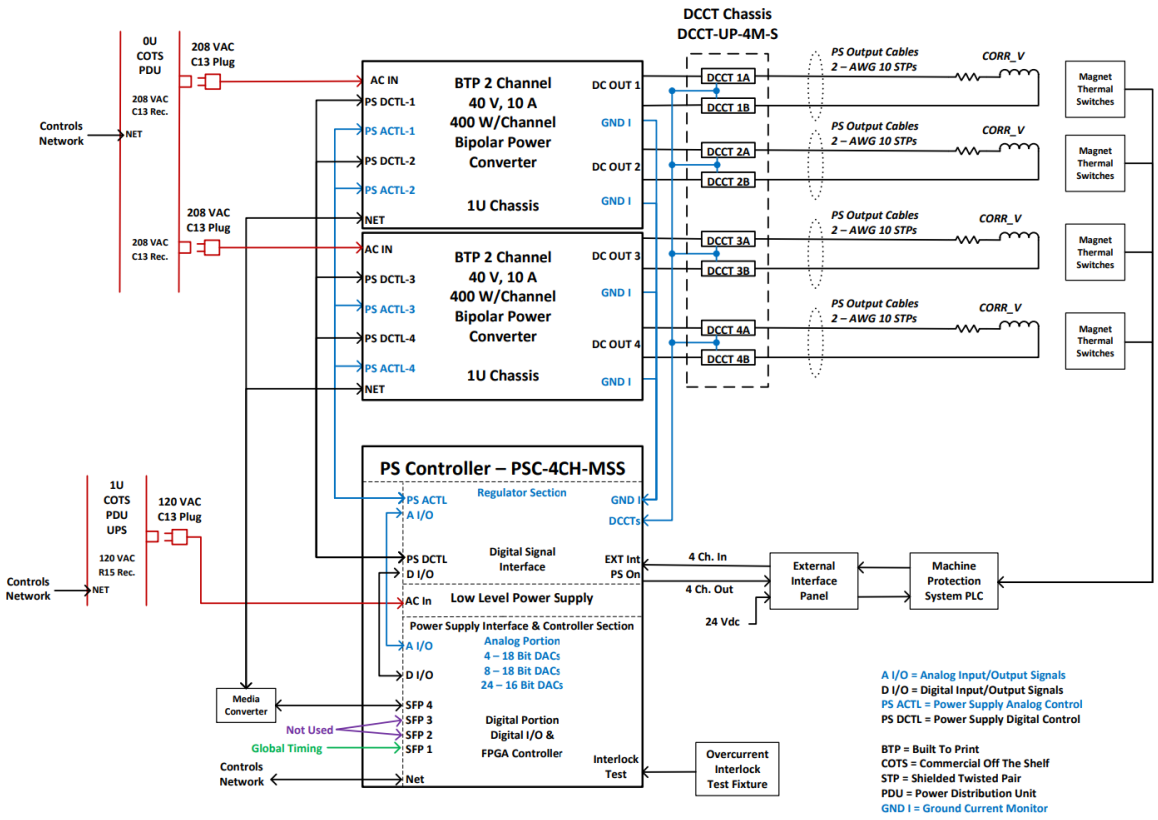


Figure 38. ESR Corrector BPCs Interfacing with Auxiliary Equipment in a Rack

4.3.3 BTP Bipolar Power Converter for ESR Dipole Trims

The ESR trim dipole power supply system is designed to support fine magnetic field adjustments in the main dipole magnets, where embedded trim coils require extremely low current and voltage operation. These trim circuits operate at currents as low as 0.1 A with voltage requirements on the order of 1-2 V, necessitating a low-power, high-precision bipolar supply architecture. A total of 34 trim dipole circuits is required, consisting of 22 unipolar COTS supplies, 10 BTP bipolar power converters, and 2 unique hybrid cases. The unique cases require dual-mode operation, where a COTS supply supports high-current operation (e.g., 100 V, 15 A or 50 V, 7.5 A), while the BTP BPC handles low-current precision operation down to ~0.1 A. The BTP BPC is specified at 5 V, 0.3 A, enabling fine control at low current levels while maintaining stability requirements.

The trim power supply is implemented as an externally controlled analog system driven by the PSC PID loop. The PSC outputs a voltage setpoint (±10 V range), which is processed through an instrumentation amplifier and analog signal conditioning chain before driving a power buffer stage capable of supplying up to 500 mA. The system eliminates the need for a DCCT by using a precision burden resistor in series with the load, allowing current measurement via voltage drop.

The burden resistor is designed to produce 1 V at maximum current:

$$R = \frac{1V}{0.3A} = 3.33\ \Omega$$

This is implemented using three 10 Ω precision resistors in parallel. The signal chain includes multiple gain stages (instrumentation amplifier and inverting amplifiers) to condition both setpoint and feedback signals, ensuring stable closed-loop control.

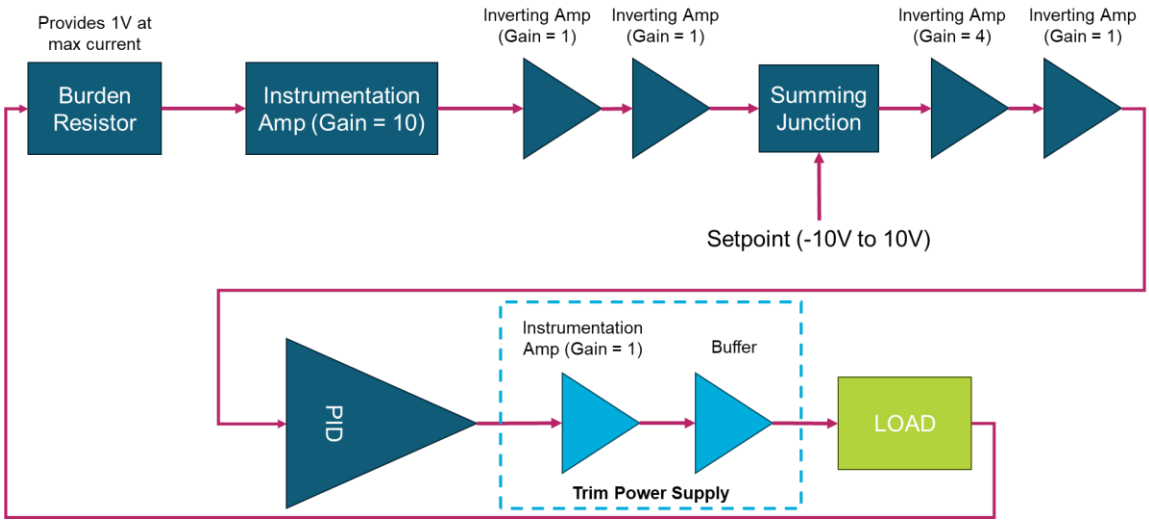


Figure 39. ESR Dipole Trim BTP BPC Block Diagram

The output stage is built around the OPA547 power operational amplifier, selected for its wide supply range (±4 V to ±30 V), high output current capability (500 mA continuous), and stability characteristics (unity gain stable, ~65° phase margin at 1 MHz). The amplifier is configured as a voltage follower, meaning output voltage tracks the input setpoint.

Voltage limits are constrained by supply rails:

$$V_{out,max} \approx +12V, V_{out,min} \approx -14.9V$$

The maximum expected voltage drop across the output stage is ~10 V, including a 20% design margin for thermal and dynamic conditions. Thermal analysis confirms that operation without a heatsink is insufficient, requiring a TO-220 mounted heatsink for safe operation under continuous load.

The system is powered directly from the PSC ±15 V rails, eliminating the need for a dedicated external supply. Each PSC regulator can supply up to 1 A, with total current consumption per two channels calculated as:

$$I_{total} = 300mA \times 2 + 1.5mA \times 2 + 35mA \times 2 = 673mA$$

This remains within regulator limits. Control is implemented using PSC ON commands, where a digital isolator drives an optocoupler and PNP transistor to energize a solid-state relay

(AQW212EX), enabling ±15 V distribution. A “power-good” signal is returned via optocoupler feedback.

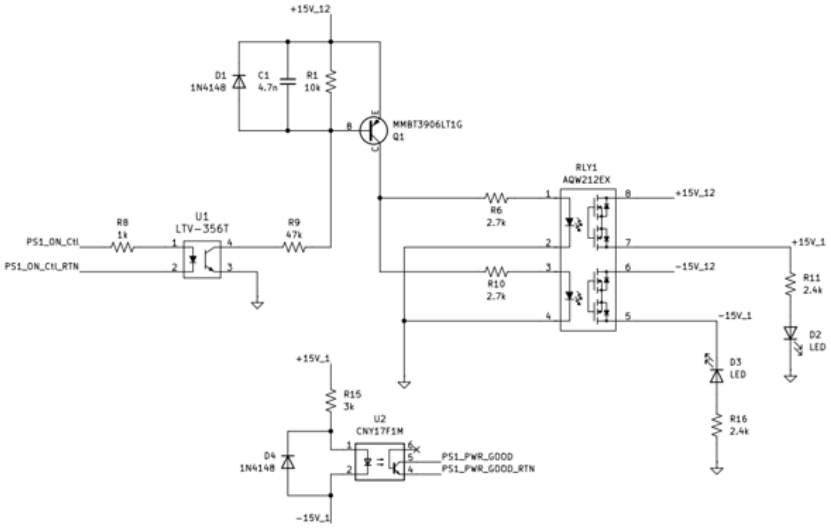


Figure 40. ESR Dipole Trim BTP BPC On-Command and Readback Circuit

Inductive coupling between the main winding and the trim coils will cause voltage to be induced when the main windings are being AC cycled and under the condition that the magnets trip off on an interlock. The induced voltage across all dipole trim BTP circuits is analyzed and TVS diodes are selected for output stage protection. The energy consumption for each TVS diode circuit is taken into consideration and multiple TVS units are placed in parallel to keep the devices within specification.

A prototype of the ESR dipole trim BTP BPC was built and tested successfully. The prototype only features a single channel, but the final design will be a 4-channel device.

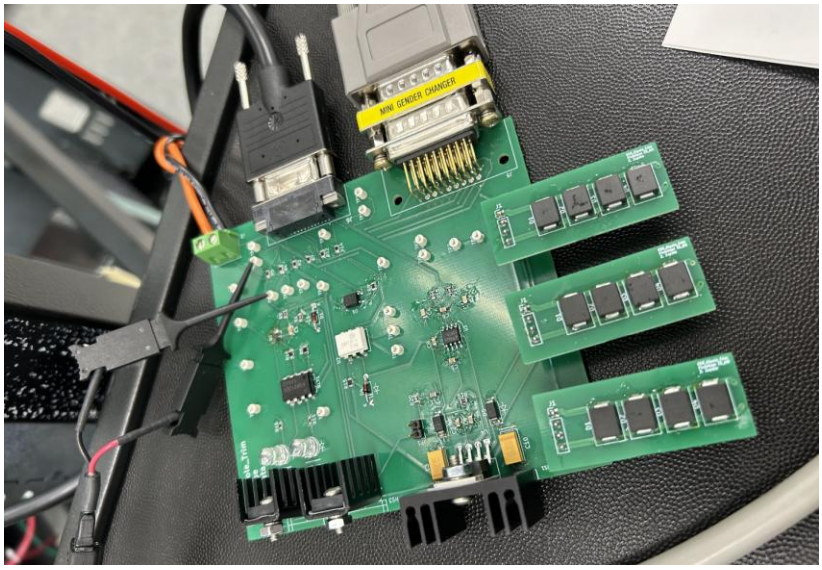


Figure 41. ESR Dipole Trim BTP BPC Prototype

One BTP 4CH 5V-0.3A BPC will be controlled and powered by a single 4CH PSC. The PSC also monitors status and detects fault conditions. No DCCT chassis is used for this application since the PSC internal burden resistors are used for current monitoring. Four magnets are powered by 2U of occupied rack space. The external interlock panel connects to thermal switches on magnets for machine protection.

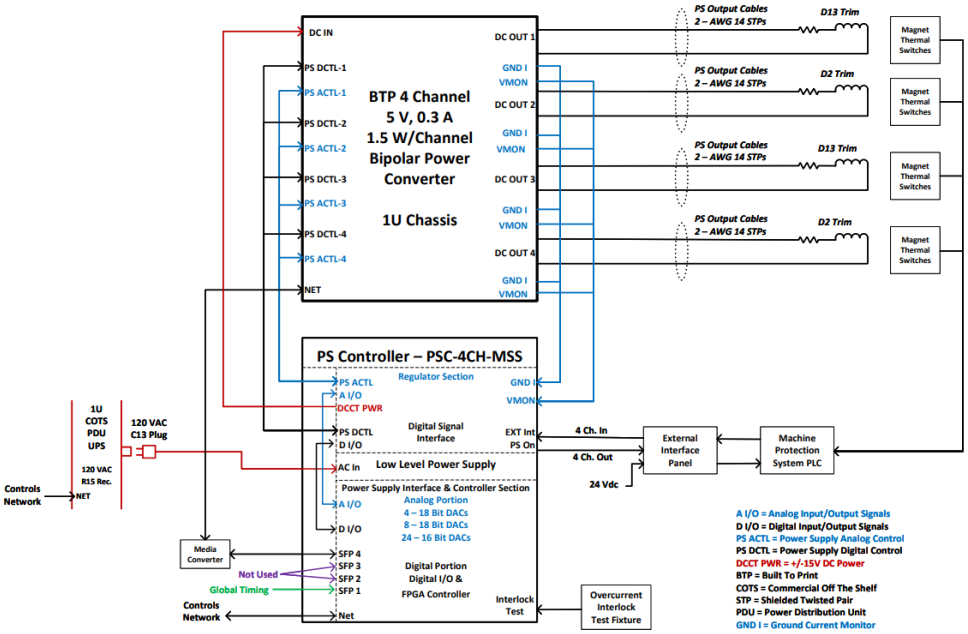


Figure 42. ESR Dipole Trim BPCs Interfacing with Auxiliary Equipment in a Rack

Ultimately, the ESR trim dipole power supply design provides a highly specialized, low-current, high-precision solution tailored to the unique requirements of trim coil operation. By leveraging PSC-based control, precision analog design, and careful protection against induced transients, the system achieves the required performance in ripple, stability, and dynamic response. The use of a simplified architecture without DCCTs, combined with robust protection and scalable hardware implementation, results in a compact, efficient, and maintainable solution suitable for integration across all ESR trim dipole circuits.

4.3.4 BTP Ground Fault Detection

Both BTP designs for the ESR correctors and dipole trims feature ground fault detection circuitry. For the ESR correctors, an internal 100Ω resistor is part of a soft ground on the output to earth ground. The voltage across this resistor is monitored and passed along to the analog input on the PSC for ground fault monitoring.

The ESR dipole trim BTP design uses a different method of ground fault detection. Since there is no available soft ground resistor in the chassis to monitor, two sense resistors are placed in series with the load, before and after. The voltages across these resistors are monitored by analog inputs to the PSC and they are compared for differences. If the difference exceeds a set threshold, the PSC will trip the supply, just like it would for the ESR corrector BTP units.

4.3.5 BTP Test Results

Since the ESR Corrector BPC follows the same design topology of the tried and tested ALS-U models, the primary point of concern is the effect of the increased bus voltage on current ripple.

The PSC will provide the current regulation for this power supply system. The four channel PSC used in the ESR Corrector BPC system has an 18-bit resolution, which means less than 10ppm stability can be achieved. The point of concern is temperature fluctuations. A detailed metrology analysis was conducted on the PSC. The entire PSC circuit, starting with the digital-to-analog (DAC) setpoint and DCCT and working through the burden resistor and all cascading amplifiers is analyzed. All temperature drift coefficients are added in quadrature for a total of 6.36 ppm/°C. Therefore, a temperature rise of 16°C will be required to exceed 100ppm. The ESR Corrector BPCs will be under strict temperature control to ensure stability is met.

To estimate the expected current ripple from the ESR Corrector BPC, an existing NSLS-II BPC will be used to take voltage ripple measurements, which will then be converted to expected current ripple, based on the ESR Corrector load. The ESR Corrector BPC will feature a 48V DC Bus. The NSLS-II BPC features the same design topology but uses 24V for the DC bus. Since the NSLS-II BPC is two channels, the channels will be wired in series to simulate the effect of a single channel with a 48V DC bus. The series connected supply will operate approximately at 32V and 8A, which is the approximately the operating point for the vertical correctors.

The device used to measure the voltage ripple is the Tektronix MSO44 Oscilloscope. The FFT magnitude function produces an FFT signal across a desired frequency band in units of V_{RMS}. The data is extracted directly from the scope to a csv file and plotted in excel.

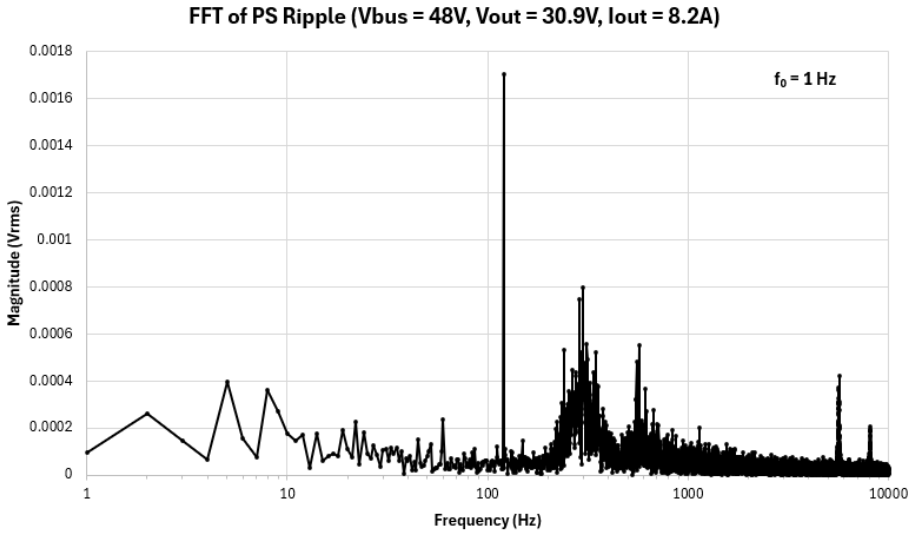


Figure 43. FFT of BPC Voltage Ripple under ESR Corrector Power Supply Operating Conditions

Since the data collected is in RMS voltage, it can be converted to RMS current according to the following relationship, using the load parameters of the circuit.

$$I_{RMS}(f) = \frac{V_{RMS}(f)}{\sqrt{R^2 + (2\pi f L)^2}}$$

The RMS current can be related to average power in a resistive load as follows.

$$P_{AVG} = I_{RMS}^2 R$$

Parseval's theorem states that the average power of a waveform is conserved between the frequency and time domain. Therefore, the summation of the powers at each frequency of the signal in the frequency domain must equal the total power of the signal in the time domain.

$$P_{total} = P_{f1} + P_{f2} + \cdots + P_{fn}$$

Substituting power for RMS current squared times resistance allows for the total RMS current up to the n^{th} frequency to be realized as the sum of squares up to and including the n^{th} frequency.

$$I_{RMS_total}^2 R = I_{RMS1}^2 R + I_{RMS2}^2 R + \cdots + I_{RMSn}^2 R$$

$$I_{RMS_total} = \sqrt{\sum I_{RMSi}^2}$$

Lastly, the total RMS current over a frequency range can be converted to ppm of the power supply. For the ESR Correctors (both horizontal and vertical), the power supply is specified as 40V, 10A.

$$I_{ppm} = \frac{I_{RMS_{total}}}{10} * 10^6$$

Using these mathematical relationships to manipulate the collected data, the results for the horizontal and vertical corrector are realized. It should be noted that the oscilloscope will return FFT data with a data point at 0Hz. This must be omitted from the above calculations, as it is a DC value and not pertinent to ripple measurements.

Five total tests were performed. The first test was an initial run and after the data was analyzed, the next four tests were taken to confirm the validity of this testing method. Data was collected and analyzed with the converter off, as well as at different set point levels, to get an idea of the noise floor associated with the equipment. Subsequent tests after the initial test see that data collected contains the time domain and frequency domain data. As a sanity check, the RMS voltage of the time domain is calculated and compared to the square root of the sum of squares of the FFT data. The results are computed for both the horizontal and vertical corrector circuit loads.

The current ripple results are shown below. It should be noted that these results are calculated from the simulation of a real circuit that will include the maximum operating voltage and resistance (due to cable length). These results meet the requirements provided by physics.

Table 13. ESR Corrector BTP Ripple Testing Results

Test	Magnet	0-1kHz (mA_{RMS})	1-10kHz (μA_{RMS})	0-1kHz (ppm)	1-10kHz (ppm)
1	Horizontal	0.20	1.83	20.25	0.18
	Vertical	0.15	1.37	15.20	0.14
5	Horizontal	0.16	1.83	15.86	0.18
	Vertical	0.12	1.37	11.91	0.14

For the ESR dipole trim BTP units, prototype testing was performed using a 4 Ω, 36 mH load with ±8 V input and 240 mA output. Results show strong agreement with PSIM simulations in terms of voltage response and control behavior. Ripple measurements indicate the device is well within specification, but to get a legitimate measurement, a very precise probe capable of reading very low voltages accurately is required.

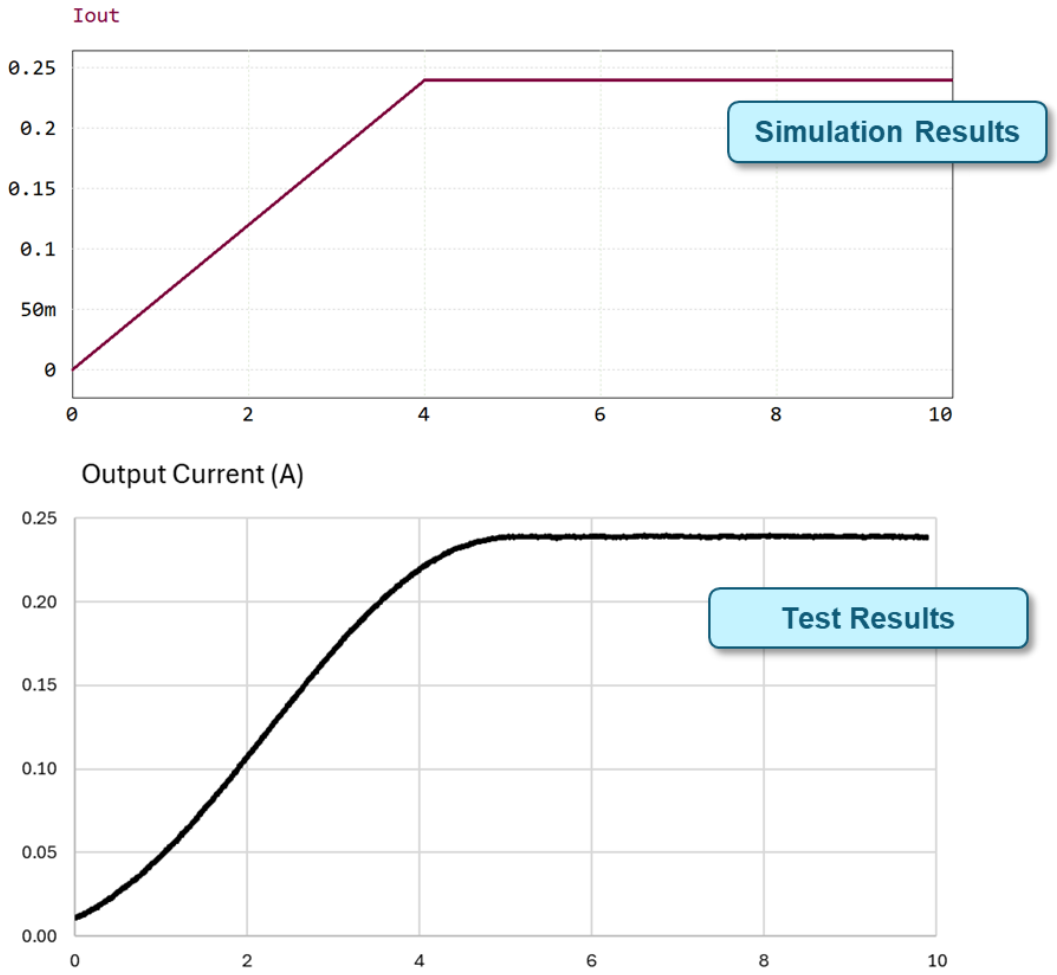


Figure 44. ESR Dipole Trim BTP BPC Simulation VS. Prototype Test Results

An ACL is implemented to ensure that all procured BTP power supplies meet ESR performance requirements through a structured and traceable validation process.

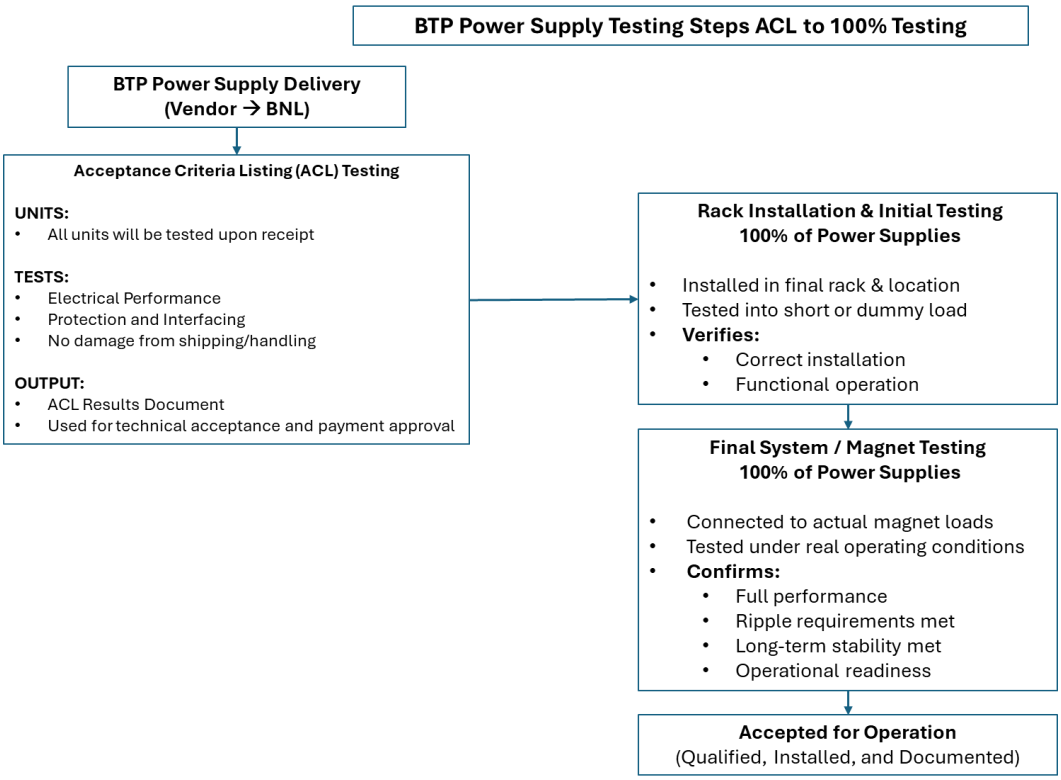


Figure 45. ESR BTP Testing Phases

4.4 Rack Design

The ESR power supply systems are housed in high-density, modular equipment racks designed to integrate power conversion, control, protection, and thermal management within a standardized framework. These racks are adapted for higher density, improved thermal stability, and scalability across multiple service buildings, with a strong emphasis on standardization, efficient space utilization, and ease of installation and maintenance. To accommodate different power and stability requirements, racks utilize either water-to-air heat exchangers for high-performance applications or air-to-air cooling for lower power systems, providing flexibility while maintaining alignment with facility infrastructure constraints.

4.4.1 Power Supply Racks

The ESR power supply racks are designed as standardized, high-density 19-inch enclosures that integrate power conversion, control, protection, and thermal management into a single, unified platform. Based on NSLS-II experience and adapted for ESR-specific requirements, the design addresses constraints such as limited cooling water flow (4.4 GPM per rack) and available airflow capacity while maintaining high power density and thermal stability. Each rack provides approximately 45U of usable equipment space within a 52U enclosure, with an additional ~7U bottom-mounted section dedicated to thermal management via an air-to-water heat exchanger. The

racks support a wide range of components, including COTS power supplies, PSCs, MCPCIC interface hardware, rack-mounted PDUs, and interlock systems. Designed for heat loads up to ~10 kW (with typical operating loads between ~1 and 7.2 kW), the system utilizes front-to-back airflow at approximately 883 CFM, matched to facility constraints. Mechanical features such as slide-mounted equipment, rear cable routing with segregation of power and control wiring, and the use of prefabricated cable harnesses enable improved maintainability, consistent assembly, and reliable high-current connections across all installations.

Table 14. Power Supply Rack Design Parameters

Parameter	Value	Notes
Rack Type	19-inch enclosure	Standard industrial format
Usable Height	45U	Excludes cooling section
Cooling Section	~7U (bottom-mounted)	Heat exchanger location
Max Heat Load	~10 kW	Design capacity
Typical Heat Load	~1–7.2 kW	ESR operating range
Airflow	~883 CFM	Matched to 4.4 GPM limit
Water Flow Limit	4.4 GPM	Facility constraint
Cooling Method	Air-to-Water HX	Primary solution
Mounting	Slide rails	Serviceability
Electrical Distribution	Rack-mounted PDU	Per-supply protection
Cable Routing	Rear exit	Segregated power/control

Across the ESR, a total of 259 power supply racks are distributed among multiple service buildings, supporting 850 power supply arrangements and approximately 2,710 magnets in total. Individual buildings host between 11 and 29 racks depending on location and system requirements, with corresponding variation in arrangements and magnet counts. This large-scale deployment is enabled by a highly standardized rack design, allowing identical mechanical and electrical configurations to be replicated across all buildings while accommodating differences in magnet types, power requirements, and cable routing. The result is a scalable and infrastructure-compliant system that tightly integrates mechanical, electrical, and thermal considerations to ensure reliable operation, reduced installation time, and long-term maintainability across the full ESR power supply network.

4.4.2 Rack Thermal Design

Thermal management is a critical aspect of ESR power supply performance, as temperature variations directly impact current stability, DCCT accuracy, and analog control loop behavior. To address this, the ESR system employs a rack-level controlled cooling approach in which each rack is independently regulated to maintain stable operating conditions. The baseline solution utilizes a bottom-mounted air-to-water heat exchanger integrated into each rack, supplied with facility chilled water at approximately 55°F. Air is circulated in a closed-loop front-to-back path at roughly 883 CFM, ensuring uniform internal temperature and minimizing sensitivity to ambient conditions. Each rack includes a dedicated control system consisting of an RTD sensor positioned mid-rack for temperature feedback and a Belimo valve actuator to regulate chilled water flow,

enabling closed-loop thermal control. The system is designed to support heat loads up to approximately 10 kW per rack, with typical operating ranges between 5 and 7.2 kW, while maintaining temperature stability on the order of ±0.3°C to ±1.7°C depending on performance requirements.

Table 15. Rack Thermal Design Parameters

Parameter	Value / Criteria	Notes
Cooling Type (Primary)	Air-to-Water HX	Rack-integrated
Airflow	~883 CFM	Per rack
Water Flow Limit	4.4 GPM	Facility constraint
Cooling Medium	Chilled water (~55°F)	Facility supplied
Max Heat Load	~10 kW	Per rack
Typical Heat Load	~5–7.2 kW	ESR operation
Temperature Stability	±0.3°C / ±1.7°C	Based on ppm requirement
Control Method	RTD + Belimo Valve	Closed-loop control
Airflow Type	Closed-loop internal	Rack-contained

Cooling method selection is driven by both stability requirements and rack heat load to ensure alignment between thermal and electrical performance. Systems requiring high precision (<100 ppm stability) use water-to-air heat exchangers regardless of load, while systems with ≥100 ppm stability may use air-to-air cooling only if the heat load is below 3 kW; above this threshold, water-to-air cooling is required. Across the ESR, a total of 262 thermally managed racks are deployed, including 177 racks using water-to-air cooling and 85 racks using air-to-air cooling, with no in-row cooling systems required. This distribution reflects an optimized approach that balances performance, efficiency, and facility constraints. Overall, the standardized rack design integrates thermal, electrical, and mechanical considerations into a cohesive platform, ensuring reliable operation and consistent performance across the full ESR power supply system.

Table 16. Rack Cooling Selection Criteria

Stability Requirement	Rack Heat Load	Cooling Method	Notes
< 100 ppm	Any	Water-to-Air HX	Required for high precision systems
≥ 100 ppm	< 3 kW	Air-to-Air Cooling	Low power systems
≥ 100 ppm	≥ 3 kW	Water-to-Air HX	Required due to thermal load

4.4.3 Auxiliary Racks

The ESR power supply system architecture assigns four types of auxiliary racks to each building, totaling 48 auxiliary racks in the design. Each rack receives a strip PDU, an air heat exchanger, and allocated space for the required equipment, ensuring that space and AC Inputs are accounted for and reserved. The spreadsheet defines the content and configuration of each auxiliary rack as follows:

- **PLC Aux Rack:** houses the PLC equipment that receives interlock signals from the marshalling boxes in the tunnel and routes them to the PSCs within the building.
- **UPS Aux Rack:** the current approach considers a centralized UPS distribution, where a dedicated rack receives AC power from a service panel and distributes UPS power to other racks.
- **QUENCH Aux Rack:** this rack houses the quench detection system. The design relocates the quench detectors currently installed in RHIC alcoves into the new service buildings. Although ESR magnets are warm, the ESR scope includes supporting the HSR quench detection system. The existing system is already operational, and upgrades are under development.
- **TAP Aux Rack:** these racks are introduced to accommodate systems associated with higher-voltage magnets. Space and basic requirements are reserved in the current design, while further evaluation is ongoing to confirm their necessity and final configuration.

4.5 Supporting Equipment in Power Supply Racks

The ESR power supply racks integrate several key supporting subsystems that enable coordinated control, protection, and interface with accelerator systems, ensuring reliable delivery of high-current power while maintaining stability and safety. These include the PSC, MCPCIC, PDU, External Interface Panel (EIP) for interlocks, and DCCTs for high-accuracy current measurement. The overall architecture follows a centralized control philosophy in which the PSC performs closed-loop current regulation using DCCT feedback, while COTS power supplies operate in voltage mode. The MCPCIC distributes setpoints and coordinates multiple supplies, the PDU manages AC distribution and sequencing, and the interlock system ensures safe operation through fault detection and shutdown. This separation of control, power delivery, and protection functions improves system robustness, scalability, and maintainability.

All supporting components are physically and electrically integrated within the rack using a structured signal flow that ensures stable and predictable operation. Setpoints originate from the PSC, are distributed by the MCPCIC to individual power supplies, and delivered to the magnet load, while DCCTs provide feedback to close the control loop. Interlock signals are routed through the EIP and PDU to enforce protection actions. The design emphasizes isolation between analog, digital, and high-power domains, consistent signal routing to minimize noise, and modular interfaces for scalability. Multiple layers of protection are incorporated, including PSC-based regulation, interlock monitoring of thermal and flow conditions, PDU-controlled sequencing, and MCPCIC coordination for multi-supply systems. The architecture supports a wide range of configurations through standardized interfaces and expandable channel capacity, and all

components undergo staged verification, ensuring consistent performance and reduced integration risk across the ESR system.

Table 17. Supporting Equipment Functional Summary

Component	Function	Key Features
COTS Power Supply	Power conversion	Voltage-mode operation, high power density
Power Supply Controller (PSC)	Current regulation and control	Analog PID loop, DCCT feedback, fault detection
MCPCIC	Signal distribution and coordination	Setpoint distribution, current sharing, sequencing
Power Distribution Unit (PDU)	AC distribution and protection	Circuit protection, controlled sequencing, interlocks
External Interface Panel (EIP)	MPS and control interface	Signal isolation, level translation, status routing

4.5.1 Multi Channel Power Converter Interface Card

The MCPCIC is a central element of the ESR power supply architecture, designed to coordinate multi-supply operation with high precision and reliability. A total of 162 MCPCIC units, each configured for 4-channel operation, are deployed across the system, with one unit assigned per power supply arrangement. The MCPCIC distributes analog setpoints from the PSC to multiple COTS power supplies through isolated signal paths, ensuring low-noise transmission and consistent regulation across channels. It supports up to 16 channels per card and enables coordinated current sharing for parallel configurations as well as synchronized operation for series configurations. Integrated timing control introduces approximately 100ms delays between channel activations to limit inrush current and protect system components during startup. In addition to setpoint distribution, the MCPCIC routes digital control and status signals, interfaces with the PDU for AC enable sequencing, and propagates fault signals through the interlock system, forming a tightly coupled control and protection layer within the rack.

The MCPCIC hardware is built on a high-density 16-layer PCB with approximately 1900 components, reflecting the complexity of its mixed-signal design. Precision analog routing is used to maintain signal integrity for setpoint distribution, while optical isolation separates low-level control signals from high-power field interfaces to minimize noise coupling and ground loop effects. A microcontroller-based control system (ATmega) manages sequencing, monitoring, and communication, including RS-485 interfaces for robust data exchange. The card supports multiple voltage rails (5V, ±15V, 3.3V, 12V) and integrates fault detection logic capable of triggering coordinated shutdown across all connected supplies. Validation is performed through a structured, multi-stage process that includes verification of voltage rail tolerances, isolation boundaries, signal

integrity, sequencing behavior, and setpoint tracking accuracy within ≤1% across the operating range. This combination of high channel density, precise analog performance, integrated protection features, and rigorous validation ensures that the MCPCIC provides reliable, scalable coordination for ESR multi-supply configurations.

Table 18. MCPCIC Design Summary

Parameter	Value / Description	Notes
Function	Multi-supply coordination	Setpoint distribution and control
Channels Supported	Up to 16	Per MCPCIC card
Setpoint Distribution	Analog (isolated)	PSC-driven
Current Sharing	Coordinated distribution	Supports parallel operation
Startup Sequencing	~100 ms inter-channel delay	Limits inrush current
PCB Architecture	~16-layer design	High-density, mixed-signal layout
Component Count	~1900 components	High integration complexity
Interfaces	PSC / PS / PDU / EIP	Full system integration
Validation Approach	Structured in-house test procedure	Bench → Rack → System validation

4.5.2 Power Supply Controller

The PSC is the core regulation and control subsystem within the ESR power supply architecture, responsible for precision current control, high-resolution feedback acquisition, and deterministic fault handling at the channel level. It consolidates multiple legacy hardware functions into a single integrated platform, reducing system complexity while standardizing interfaces across all power supply families. The PSC is built around a modular digital/analog architecture using a PicoZed Zynq-7030 System-on-Module, which combines FPGA fabric for real-time deterministic processing with an embedded ARM processor for supervisory control. The hardware is partitioned into a digital processing assembly and an analog regulation assembly to separate time-critical functions from higher-level processing. The digital assembly provides high-resolution DAC outputs (18-bit or 20-bit) for current setpoints, high-resolution ADC inputs for DCCT feedback, additional diagnostic ADC channels, digital I/O for control and interlocks, and local memory for buffering high-speed diagnostic data. The analog assembly implements precision signal conditioning and a high-bandwidth, low-noise analog PID control loop, ensuring stable current regulation while maintaining full digital observability of loop signals such as error, setpoint loopback, and regulator output.

Each PSC channel operates as a closed-loop current regulator, using high-resolution DAC-generated analog references and DCCT-based current feedback acquired through precision ADCs. The architecture supports both unipolar and bipolar operation depending on system configuration and may utilize multiple ADC channels to monitor supply and return currents for enhanced diagnostics and ground fault detection. Control features include smooth ramp generation, deterministic execution of preloaded ramp tables, and step-response “jump mode” for testing and characterization. Fault detection and interlock handling are implemented directly in FPGA

firmware, enabling low-latency, deterministic response independent of network delays. The PSC monitors conditions such as overcurrent, overvoltage, ground faults, DCCT validity, and power converter status, with all faults latched until explicitly cleared. Additional design features include snapshot-based diagnostics, where high-rate waveform data is captured in local memory during transient events, allowing detailed post-mortem analysis without continuous high-bandwidth data streaming. These design parameters enable the PSC to deliver precise, stable, and reliable current control across the ESR power supply system.

The PSC Automated Test Equipment (ATE) is a dedicated validation platform designed to verify the high-precision analog and digital functionality of the PSC prior to system integration. Because direct testing with operational power supplies and magnet loads is impractical for production and regression testing, the ATE provides a controlled, repeatable environment for comprehensive verification. The system consists of a multi-channel tester PCB with embedded firmware, cable interfaces to the PSC under test, and a host computer that executes automated test sequences. It emulates the full range of PSC interfaces, including digital status signals for unipolar and bipolar converters, DCCT current feedback, fault conditions, heartbeat signals, and On/Off/reset responses, as well as configurable magnet and converter dynamics through plug-in tuning boards.

A key design feature of the ATE is its integrated 20-bit precision current source, which enables accurate calibration of PSC DCCT ADC channels, along with channel-level relay switching that allows seamless transition between functional testing and calibration modes without reconfiguration. The ATE supports automated verification of channel behavior, setpoint generation accuracy, DCCT feedback acquisition and calibration, fault detection and interlock response, digital I/O transitions, and control loop performance under emulated load conditions. Although certain specialized interfaces such as EVR timing and fast orbit feedback are not exercised, the ATE provides high coverage of the primary regulation, diagnostics, and protection functions. This enables its use for production acceptance testing, regression validation following hardware or firmware updates, and pre-integration verification, ensuring consistent performance and reducing risk prior to deployment in ESR racks.

4.5.3 Power Distribution Units

The system relies on two types of PDUs: COTS and BTP. For systems that operate with 208V 1p (like the correctors and some low power sextupoles), a COTS PDU is being used: EVMA8365X. This is a 20Ch. PDU that can power all 208V 1p inside a rack.

The BTP PDU design is based on adapting proven LSII 3-phase PDU models to meet the specific electrical, mechanical, and operational requirements of the ESR power supply system. These PDUs serve as the interface between facility mains and individual power supplies, distributing power through an input circuit breaker and multiple protected output channels. Existing LSII designs for 208V and 480V systems were selected as baseline platforms and modified to align with ESR load demands, resulting in both direct-use models and newly derived configurations with adjusted channel counts, breaker ratings, and component selections. The design process emphasizes reuse of established, validated hardware while introducing targeted modifications, such as resizing breakers, adjusting channel configurations, and selecting appropriate current transducers, EMI filters, and wiring. This ensures compatibility with ESR operating conditions and cost efficiency.

New ESR-specific PDU models were developed to accommodate system requirements not covered by the original LSII designs, including configurations with reduced channel counts (e.g., 2-channel units) and higher current capabilities for 480V systems. Electrical sizing is performed using standardized calculations for channel and input currents, incorporating design margins, power factor, and efficiency considerations to ensure safe and reliable operation. The mechanical design remains largely consistent with the original LSII layouts to simplify fabrication and integration, while all units comply with UL 508A standards and maintain a consistent short-circuit current rating (SCCR) of 5 kA. This approach results in a modular, standardized, and scalable PDU solution tailored to ESR requirements. More detailed design information, calculations, and component selections can be found in *Adaptation of LSII's 3p PDUs Models for ESR's PS Systems.* There are five different BTP models that can power the entire system:

- 3P BTP PDU 4 X 20A 480V X 70A
- 3P BTP PDU 4 X 25A 480V X 100A
- 3P BTP PDU 2 X 20A 480V X 45A
- 3P BTP PDU 4 X 20A 208V X 70A
- 3P BTP PDU 2 X 20A 208V X 40A

4.5.4 DCCT

DCCTs are selected for every COTS supply application. For these supplies, a COTS DCCT is selected based on the nominal current of the string. These are referred to as packaged DCCTs, as they include integrated instrumentation within a dedicated enclosure, in contrast to the unpackaged DCCTs used for BTP systems.

Table 19. COTS Packaged DCCT Models

Model	Nominal Current	Turns Ratio
DS50ID	75	1:500
DS200ID	300	1:500
DS300ID	450	1:1000
DS600ID	900	1:1500
DN1000ID	1500	1:1500
DM1200ID	1500	1:1500

The BTP units will feature a special BTP DCCT Chassis. The chassis size is 2U and is mounted in the back of the rack. The chassis aligns with two 1U-2CH BPCs, which allows the output bus to pass through the DCCTs. The design has been tested at NSLS-II and is ready for deployment.

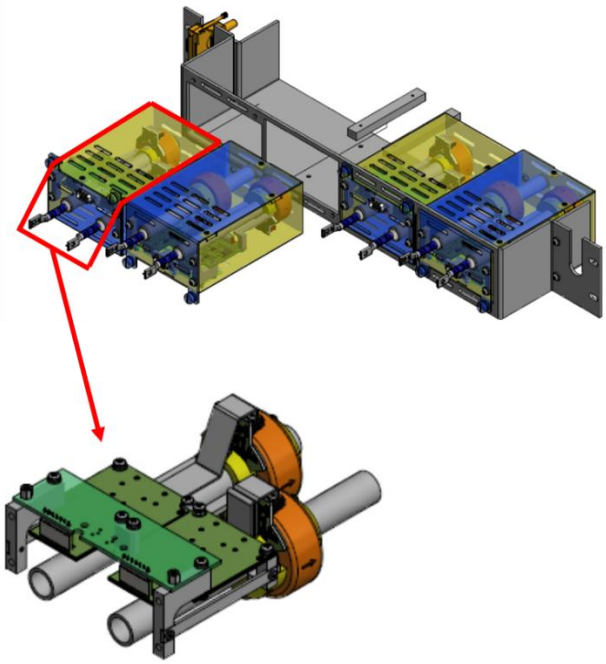


Figure 46. BTP DCCT Chassis

4.6 Controls Interface

The PSC is integrated into the EIC controls environment. Operators, high-level applications, timing systems, and machine protection infrastructure interact with PSC hardware. Time-critical regulation, interlock processing, and local diagnostics are implemented within the PSC with a focus on system-level integration, including timing distribution, reference waveform generation, network interfaces, supervisory control, and operator interaction.

4.6.1 Common Platform Integration

The PSC interfaces to the Controls Group "Common Platform," which provides standardized hardware and firmware for timing distribution and data transport across EIC subsystems, including BPMs, LLRF, instrumentation, and power supply interfaces.

The Common Platform is implemented as an FPGA-based 2U carrier chassis that hosts application-specific daughtercards. For power supply applications, it is fitted with SFP daughtercards, which provide fiber-optic interfaces between the Common Platform and PSC chassis. Each carrier can host multiple PSC fiber links, enabling scalable deployment across EIC service buildings without custom point-to-point timing hardware.

4.6.2 Timing and Event Distribution (TDL & "TDL-Lite")

Global timing reference and event codes are distributed throughout EIC using the Timing-Data Link (TDL), synchronous to the master 100 MHz timing reference. The PSC participates in the timing system using a reduced-rate derivative of the TDL protocol ("TDL-Lite") implemented over a point-to-point fiber link between each PSC and the Controls Common Platform SFP daughtercard.

The TDL-Lite link preserves packet structure and synchronization characteristics of the full TDL system while operating at a line rate compatible with PSC transceivers. This link provides:

- Deterministic timing reference to the PSC
- Distribution of timing events used to trigger synchronized setpoint execution
- System-wide timestamping of PSC readback data
- A low-latency upstream path for selected power supply status and diagnostic data

Timing synchronization and timestamping enable coordinated multi-power-supply ramp execution and correlation of PSC diagnostics with machine events.

4.6.3 Reference Waveform Generation and Synchronized Setpoints

Generation of synchronized reference waveforms is the responsibility of the Controls System. High-level waveform definitions are produced using Controls Group waveform generation tools derived from prior accelerator systems. These waveforms are distributed to PSCs over the timing and data distribution network and executed synchronously using timing events.

Reference waveform generation supports:

- Time-dependent functional definitions
- Parameterized waveform computation
- Synchronization to global timing events
- Coordinated multi-channel setpoint delivery

The division of standardized waveform generation logic from power supply-specific control logic increases the maintainability of the system across both controls and Power Supply groups.

4.6.4 EPICS Integration and Supervisory Control

Each PSC is integrated into the EIC controls environment using EPICS. The Controls System provides operator interfaces and high-level application access to PSC configuration, operating modes, diagnostic readbacks, snapshot data retrieval, and fault state visualization.

Supervisory control responsibilities include:

- Loading ramp tables and waveform parameters
- Selecting PSC operating modes
- Coordinating multi-PSC operations
- Managing configuration and version control
- Providing operator displays and alarms

EPICS provides the primary interface between human operators, automation tools, and PSC hardware. The details of PSC internal control and regulation behavior are defined in the PSC section and are not repeated here.

4.6.5 Network Communication Architecture

Network communication between the Controls System and PSCs uses standard Ethernet infrastructure. Supervisory control, configuration, and data retrieval are transported over TCP/IP, while selected fast diagnostic or status paths may use UDP-based links where appropriate.

Controls-side networking is responsible for:

- Routing configuration and setpoint data to PSCs
- Aggregating diagnostic and snapshot data
- Enforcing data rate limits and timeout policies
- Integrating PSCs into the facility network security and addressing scheme

This layered networking architecture decouples supervisory control traffic from timing-critical data paths, preserving deterministic PSC behavior while enabling scalable deployment across ESR service areas.

4.6.6 Fast Protection and Feedback Participation

The Controls Interface provides deterministic low-latency bi-directional data paths that allow PSC channels to participate in system-level machine protection and beam-based feedback when required. Status and selected diagnostic data from PSCs can be propagated upstream via the TDL-Lite link to the Controls Common Platform and machine protection infrastructure.

Control-side processing coordinates PSC participation in:

- Fast machine protection systems
- Interlock response strategies
- Beam-based feedback loops requiring synchronized current or status feedback

The controls layer provides orchestration and data routing, while deterministic fault detection and channel shutdown remain local to the PSC hardware as described in section 4.5.2.

4.6.7 Operator Workflows, Alarms, and Recovery

The Controls System provides operator-facing tools for monitoring PSC status, visualizing diagnostics, managing alarms, and coordinating recovery actions following fault events.

Controls-side responsibilities include:

- Alarm presentation and prioritization
- Fault visualization and historical logging
- Coordinated recovery workflows across multiple PSCs
- Coordinated sequencing for mode and operational setting changes
- Support for commissioning and machine studies

Fault latching and protection behavior are implemented locally within the PSC and described in the PSC section. The Controls Interface provides system-level visibility and operator workflows to support safe and efficient recovery.

4.7 Beam Based Alignment

The design basis, physics requirements, and supporting bench test results establish the ESR BBA shunt hardware as a practical and technically credible solution for beam-based alignment on series-powered quadrupoles in the EIC Electron Storage Ring. By temporarily diverting a controlled fraction of current from a selected quadrupole, the system produces the local optics perturbation required for BBA without the cost and complexity of dedicated power supplies for each magnet.

The concept has been reduced to a buildable local chassis with defined resistor ratios, DC-rated switching, controlled transient suppression, and a credible thermal path. The remaining work is installation-specific verification and calibration, not further concept development. The system is thus ready for controlled fabrication, commissioning and subsequent routine use for ESR beam-based alignment measurements.

4.7.1 BBA Objective

The Electron Storage Ring (ESR) of the Electron-Ion Collider requires quadrupole magnetic centers to be aligned to the circulating beam with sub-100 μm precision. Because many ESR quadrupoles are powered in series from common high-current power supplies, conventional beam-based alignment (BBA) methods based on independent adjustment of individual magnet currents are not practical. The system described in this report addresses that constraint by temporarily diverting a controlled fraction of current from a selected quadrupole magnet through a local shunt branch. The resulting localized reduction in quadrupole strength produces a measurable orbit response at the beam position monitors (BPMs), from which the beam offset relative to the magnetic center can be inferred.

The proposed hardware consists of a resistor-based shunt assembly, a DC-rated contactor, a relay-driven PLC interface, and an RC snubber network for transient suppression. The assembly is mounted on the magnet girder to keep the high-current loop short and to provide a credible thermal path into the local support structure. Bench validation has confirmed the expected static current division, repeatable switching behavior, and transient response consistent with circuit simulation. On that basis, the design is technically sound and ready for controlled on-site commissioning.

4.7.2 System Requirements and Operating Concept

The ESR BBA system is intended to impose a controlled local perturbation in quadrupole strength so that the corresponding orbit response can be measured with BPMs and used to infer beam-to-magnet offset. The design is governed by four requirements:

- The perturbation must be large enough to generate a clear BPM signal
- The shunt hardware must operate safely in a high-current inductive DC circuit
- The shunt-in and shunt-out states must be reversible, deterministic, and repeatable
- The system must integrate cleanly with PLC sequencing so that measurements can be executed remotely and reproduced reliably.

At the reference operating point, the nominal ESR quadrupole current is approximately 412 A DC, with lower current available during commissioning or reduced-energy operation. Depending on

quadrupole family and local optics sensitivity, the required current diversion is about 5% to 10%. Only one BBA chassis shall be active at a time in order to avoid unnecessary global optics changes and to simplify controls and protection logic.

Optics analysis at 18 GeV provided the required perturbations so that the induced tune shift remains approximately 0.03 while preserving adequate BBA sensitivity. The most demanding cases imply a BPM resolution target of roughly 1 μm for one-second averaged orbit data. In normal use, the shunt branch is inserted only for the measurement interval: a controlled fraction of the series current bypasses the selected quadrupole, the differential orbit response is recorded, and the beam offset relative to the magnetic center is then inferred from the shunt-in/shunt-out difference.

Table 20. Physics-Derived Shunt Requirements for ESR Quadrupole Beam-Based Alignment

Quadrupole	Target ΔG/G	Required Rshunt / Rcoil	Magnet family
HQF_1	7.5%	12.3	Q50
HQD_1	7.5%	12.3	Q50
HQF_3	7.5%	12.3	Q50
HQD_3	7.5%	12.3	Q50
HQF_5	7.5%	12.3	Q50
HQD_5	7.5%	12.3	Q50
HQF_7	7.5%	12.3	Q50
HQD_7	7.5%	12.3	Q50
HQF_9	7.5%	12.3	Q50
HQD_9	7.5%	12.3	Q50
HQF_11	5.0%	19.0	Q50
HQD_11	6.0%	15.7	Q50
HQFSS_9	7.5%	12.3	Q60
HQDSS_9	5.0%	19.0	Q60
HQFSS_10	7.5%	12.3	Q60
HQDSS_10	6.0%	15.7	Q60
HQFLSS_10	10.0%	9.0	QLA120
HQDLSS_10	10.0%	9.0	QLA120
HQNFSS_2	7.5%	12.3	QN80
HQNDSS_2	7.5%	12.3	QN80

Note. Under the steady-state resistive approximation, the quadrupole coil and shunt branch form a parallel current divider, so the required current diversion is given by $\Delta G/G \approx I_{shunt}/I_{total} = 1/(1 + R_{shunt}/R_{coil})$

4.7.3 Electrical Design

Each local BBA chassis contains the shunt resistor network, the switching contactor, and the transient-suppression snubber circuit. The shunt branch is connected locally at the magnet and is used only during BBA measurements. High-current conductors are kept short to minimize loop inductance and voltage drop, while long runs to the PLC or service building are restricted to low-power control and optional status signals.

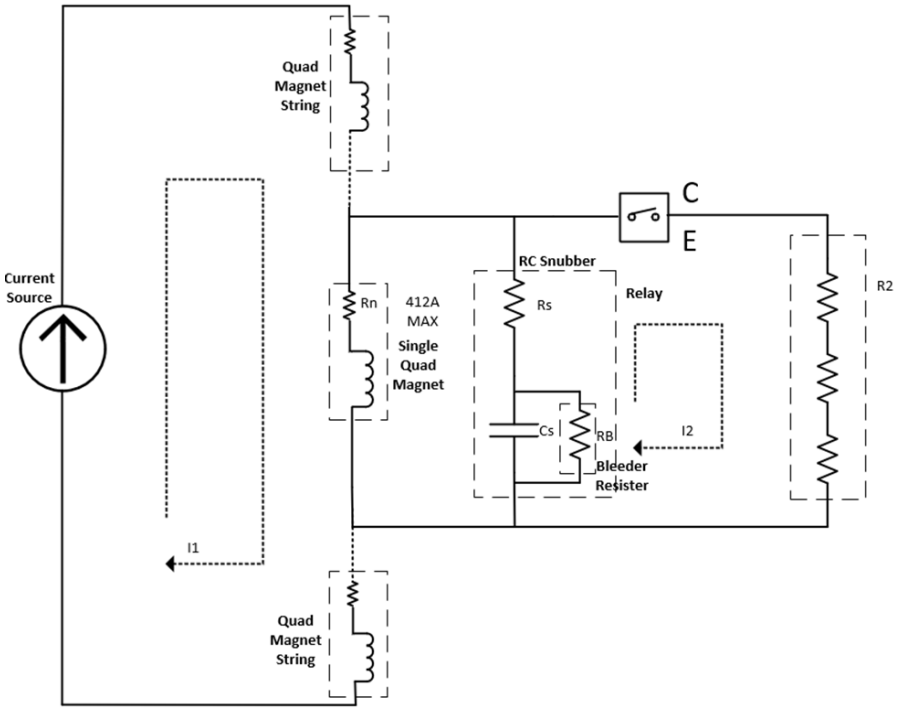


Figure 47. BBA System Block Diagram showing magnet and shunt resistor

For initial sizing of the shunt, the quadrupole coil may be represented by an effective DC resistance, Rq. If the desired bypass fraction is defined by $f = I_{shunt}/I_{total}$, the shunt branch resistance is chosen so that the steady-state current division produces the required current diversion. Under the steady-state resistive approximation, the required shunt resistance is:

$$R_{sh} = R_q(1 - f)/f$$

Equivalently, if the required ratio R_{shunt}/R_{coil} is specified from the optics analysis, the diverted-current fraction is:

$$f = 1/(1 + R_{shunt}/R_{coil})$$

The values in Table 1 therefore provide the direct link between the physics-derived BBA requirement and the electrical sizing of the shunt resistor branch.

The contactor operates in a coupled inductive circuit formed by the quadrupole, the shunt branch, and the associated power cabling. Interruption of current in this network can produce significant transient overvoltage at the contactor terminals if no suppression is provided. An RC snubber is therefore included to provide a temporary energy-absorption path during switching, limit peak voltage, and reduce ringing in the transient response.

The BBA chassis uses Riedon PF2272 heatsink-mounted power film resistors in two functions: as the primary shunt resistors that divert a controlled fraction of quadrupole current, and as the series damping resistor in the snubber network. The snubber network consists of a PF2272 resistor in series with a 1000 µF, 600 V non-polar film capacitor, with bleeder resistors connected across the capacitor to ensure controlled discharge after switching. Worst-case circuit simulation at the

maximum expected operating current predicts a transient limited to approximately +250 V and −50 V, indicating acceptable damping and contactor-voltage control for the intended application.

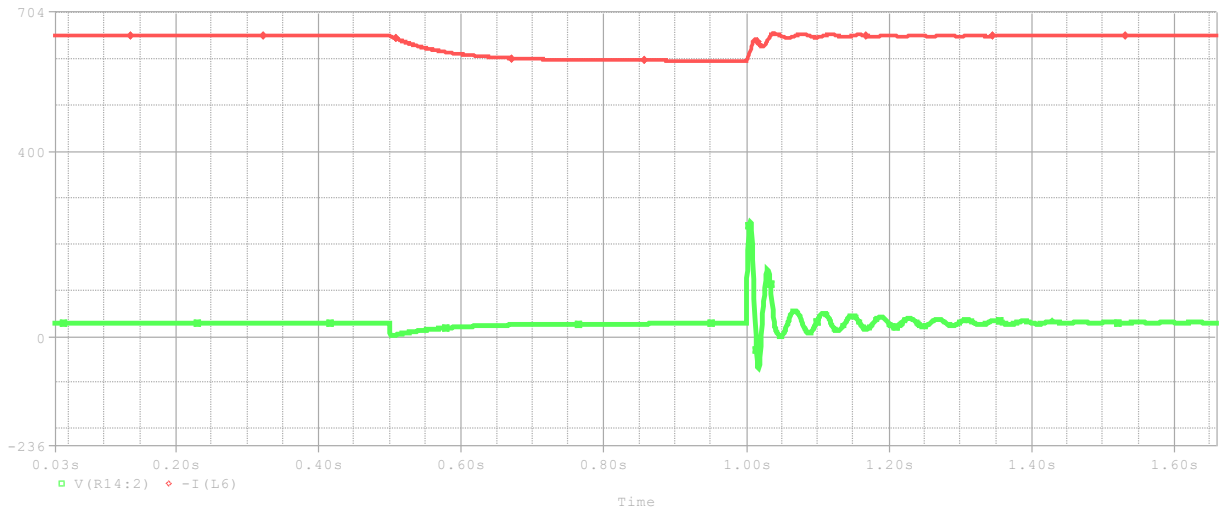


Figure 48. Simulation Showing Spikes in magnet during BBA excitation. RED is Magnet current and green is Magnet Voltage, spike is +250V/-50V, decaying sinewave, about 40HZ

The ALEV100CA contactor is used for the shunt switching function because it provides DC-rated switching appropriate for the BBA circuit. The contactor coil is driven through a relay-based PLC output module, which provides the required interface between the controls system and the 24 VDC coil. The contactor also includes an auxiliary contact that may be routed back to the PLC for status monitoring; however, this readback function is optional and is not required for basic operation. The control sequence shall include a request for shunt insertion, a dwell period for electrical settling, initiation of beam measurement, a command for shunt removal, and return of the system to its normal operating state. Where implemented, the auxiliary contact may be used to confirm contactor state as part of the controls logic.

Table 21. Principal Components of the Local BBA Chassis

Component	Selected part / family	Function
Shunt resistor family	PF2272 / PF2274 / PF2276	Selected by magnet family and dissipation
Snubber resistor	Riedon PF2272	Series damping resistor in the RC snubber
Snubber capacitor	1000 µF, 600 V non-polar film capacitor	Transient energy absorption during contact opening
Contactor	ALEV100CA, 24 VDC coil	DC-rated switching of the shunt branch
Bleeder network	High-value resistor(s) across snubber capacitor	Controlled capacitor discharge after switching
PLC coil drive	Relay-based 24 VDC output module	Drives the contactor coil from the controls system
Optional status input	ALEV100CA auxiliary contact	Optional PLC state monitoring

4.7.4 Thermal and Mechanical Design

The thermal performance of the BBA resistor assembly is governed by the power dissipated in each chassis-mounted resistor and the effectiveness of the thermal path from the resistor body into the supporting structure. The selected resistor family includes the Riedon PF2272, PF2274, and PF2276 models, with junction-to-case thermal resistances of 0.35 °C/W, 0.23 °C/W, and 0.11 °C/W, respectively. Additional thermal resistance contributions arise from the case-to-heatsink interface and the heatsink-to-structure path, both of which are controlled through proper mounting, surface preparation, and the use of thermal interface material.

Thermal verification has been performed on a per-resistor basis using representative power dissipation values and conservative assumptions for ambient temperature and interface thermal resistance. The junction temperature is evaluated as

$$T_{j,i} = T_{amb} + P_i\left(R_{jc,i}+R_{c-hs}+R_{hs-m}\right)$$

Where P_i is the dissipated power and the thermal resistances represent the heat flow path from the resistor junction to the mounting structure. $R_{jc,i}$ is the model-specific junction-to-case thermal resistance of shunt resistor, $R_{c,hs}$ is the case-to-heatsink thermal resistance, and $R_{hs,m}$ is the heatsink-to-structure thermal resistance.

This steady-state evaluation provides a conservative upper bound on temperature rise.

As a representative case, consider a PF2272 resistor dissipating 70 W under a 60 °C ambient condition. Using $R_{jc} = 0.35$°C/W, $R_{c-hs} = 0.10$°C/W, and $R_{hs-m} = 0.10$°C/W, the total thermal resistance is

$$R_{tot} = 0.35 + 0.10 + 0.10 = 0.55\,°C/W.$$

The corresponding temperature rise is

$$\Delta T = 70 \times 0.55 = 38.5\,°C,$$

yielding a junction temperature of

$$T_j = 60 + 38.5 \approx 99\,°C.$$

This result remains well below specified resistor limits of 150 °C, providing substantial thermal margin under conservative steady-state assumptions.

In actual operation, the BBA excitation is applied only for short durations (on the order of a few seconds per measurement cycle). Under these conditions, the thermal response is dominated by the thermal mass of the resistor and mounting structure, and the junction temperature does not reach steady state. Consequently, the transient temperature rise during normal operation is significantly lower than the calculated steady-state values, providing additional margin.

The resistor mounting arrangement is an integral part of the thermal design. The PF2272, PF2274, and PF2276 devices are rated for 200 W, 300 W, and 600 W, respectively, when mounted to an adequate heatsink, but only 5 W without heatsinking. The resistors are mounted on a 9 in × 10 in aluminum plate attached directly to the magnet girder, providing effective heat spreading and a low-resistance thermal path to the surrounding structure. This configuration also minimizes loop inductance in the high-current branch by keeping the shunt assembly physically close to the quadrupole.

Based on the combination of conservative steady-state analysis, short-duration operating conditions, and validated mounting configuration, the thermal performance of the BBA resistor assembly is considered adequate. No additional field-side thermal calculation is required beyond standard installation verification of mounting quality and electrical connections.

For the high-current power branch, 10 AWG copper conductors are used for the short magnet-to-BBA connections and are adequate for the expected current and installation length, subject to standard verification of insulation class and installation practices.

4.7.5 Bench Validation and Expected Field Performance

A prototype BBA shunt chassis was designed and fabricated in house with support from EIC engineering, design, and CAD personnel. Bench validation was performed with a representative resistive-inductive quadrupole load in order to verify current division, switching behavior, transient response, and status-readback capability prior to field installation.

The completed bench tests confirmed that the basic circuit behavior is consistent with the intended operating concept. Static current division was observed within the target band, indicating that the resistor sizing and current-sharing method are sound. The measured transient waveform exhibited damped ringing consistent with the circuit model, supporting the adequacy of the selected snubber network. Peak transient behavior scaled in a manner consistent with simulation expectations, and relay timing was repeatable at approximately 15ms for both closure and opening operations.

Table 22. Bench Validation Summary

Test	Observed result	Significance
Static current division	Measured bypass fraction within the expected target band	Confirms resistor sizing and current-sharing concept
Transient waveform	Damped ringing consistent with circuit simulation	Supports adequacy of the selected snubber network
Peak transient voltage	No unexpected overstress; results scaled with model expectations	Supports acceptable voltage margin at prototype level
Relay timing	Approximately 15ms and repeatable for closure and opening	Suitable for deterministic PLC sequencing
Auxiliary contact readback	State change observed on both transitions when connected	Optional interlocked logic is feasible

These results directly support a pre-installation readiness review. The bench program validates electrical behavior and switching performance; it does not replace the machine-level commissioning needed to confirm BPM orbit response and final optics sensitivity. In field operation, the governing performance metric becomes the orbit signal-to-noise ratio at the BPMs, so the shunt fraction must remain large enough to produce a clear differential orbit signal while small enough to avoid unnecessary optics disturbance or protection trips.

4.7.6 Manufacturing Plan and Residual Risks

The manufacturing plan for the ESR BBA hardware is in progress, with final manufacturing documentation either complete or under technical review. Commissioning shall proceed following the completion of documentations through applicable hold points: verification of mechanical installation and electrical continuity, confirmation of PLC logic and fail-safe de-energization, reduced-current energization of the magnet, acquisition of shunt-in and shunt-out waveforms over multiple switching cycles, and verification of resistor temperature rise prior to enabling beam-based alignment measurements.

The remaining risks are not fundamental to the design but are associated with installation and calibration. Key concerns include thermal coupling, contact resistance in the switching path, and uncertainty in cable and magnet parameters. These effects can influence the effective bypass fraction and transient behavior and will be addressed through installation verification and commissioning measurements.

The prototype BBA assembly has completed BNL Electrical Equipment Inspection (EEI), and production units will be fabricated as identical builds. A failure mode assessment confirmed that interrupting current with a fuse is not appropriate in the inductive circuit. Instead, resistor redundancy has been incorporated to prevent excessive temperatures under single-component failure conditions. In addition, BBA component faults are expected to produce measurable beam detuning, providing an independent operational indication of system integrity.

4.8 Magnet Interlock and Machine Protection

The ESR Magnet Interlock and Machine Protection System (MPS) provides a coordinated, fault-tolerant framework to ensure safe and reliable accelerator operation by continuously monitoring critical system parameters and enforcing rapid protective actions when faults occur. The system integrates power supplies, magnet protection devices, and control infrastructure using a distributed, modular architecture with centralized PLC-based decision-making, enabling fast and deterministic shutdown of power supplies while maintaining isolation between tunnel equipment and control systems. It protects magnets, power supplies, personnel, and overall accelerator operation by preventing unsafe conditions, and incorporates functions such as thermal monitoring, cooling supervision, interlocks, rack-level interfaces, and integration with Beam-Based Alignment controls. Standardized interfaces and scalable design ensure consistent protection performance across all ESR racks and buildings.

4.8.1 Interlock and MPS PLC Interface

Each building is equipped with a dedicated PLC responsible for monitoring interlock signals and executing protection logic locally. Each PLC includes an MPS module, a BBA module, and digital input/output modules to handle interlock signals and control actions. Communication between PLCs is achieved via PROFINET industrial Ethernet, enabling coordinated operation and ensuring consistent, system-wide protection across all ESR buildings.

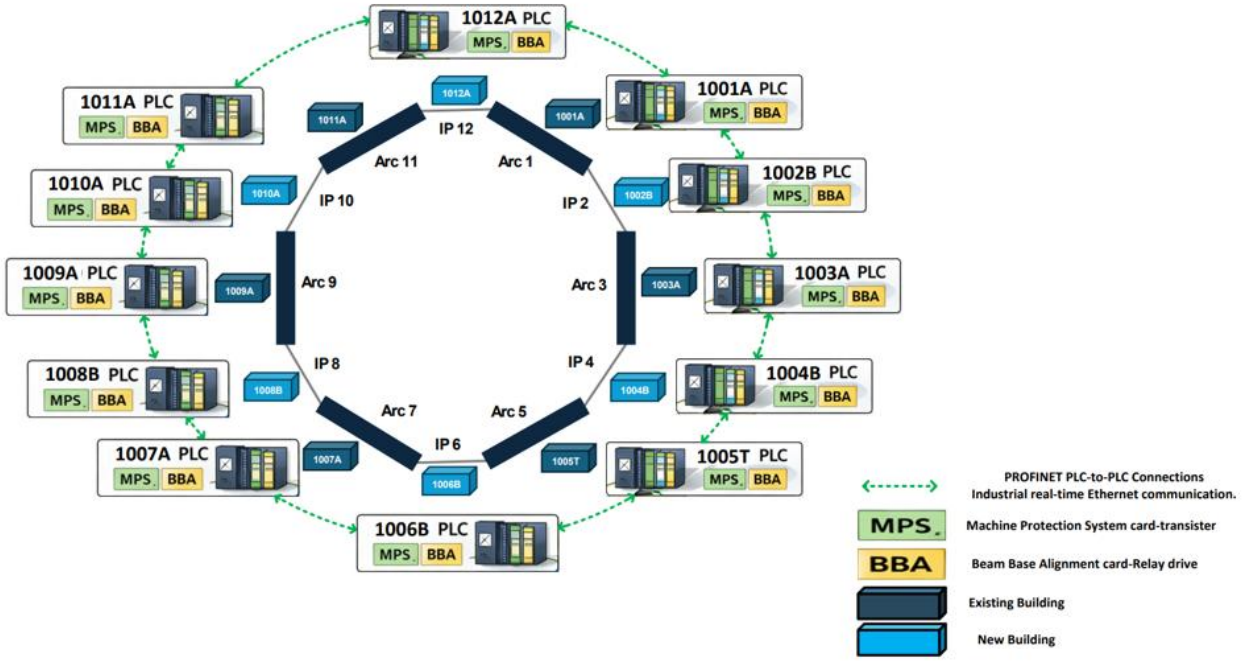


Figure 49. Distributed PLC Architecture across ESR buildings showing PROFINET Communication and Integration of MPS and BBA Modules

4.8.2 Rack-Level Interlock Interface and Thermal Control Integration

At the rack level, interlock signals are routed through the EIP, which provides signal conditioning, isolation, and interface between PLC and PSC systems. The rack also includes a temperature control system that regulates cooling water flow using a Belimo valve actuator based on measured rack air temperature.

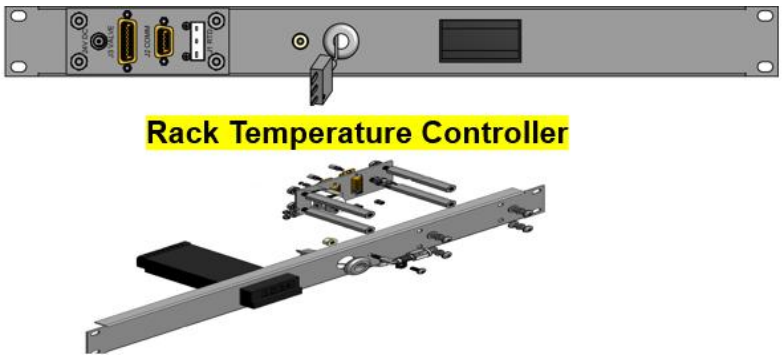


Figure 50. Temperature Controller

The EIP serves as the interface between the PLC-based protection system and the PSC, providing optical isolation to ensure safe and noise-immune signal transfer. It converts 24 V PLC signals to TTL levels required by the PSC, routes power supply ON status signals to both the PLC and safety systems and accepts thermal and flow interlock inputs for protection. The inclusion of LED indicators supports local diagnostics and troubleshooting, while the overall design enables consistent, modular integration across all ESR racks.

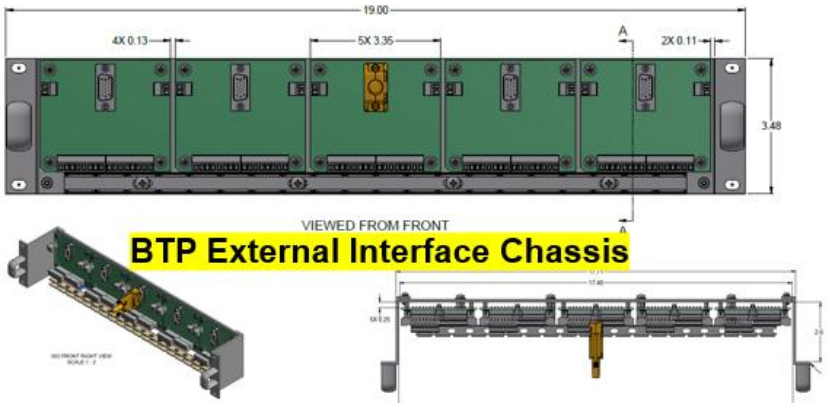


Figure 51. External Interface Chassis

4.8.3 MPS Logic and Operation

The MPS PLC continuously monitors and evaluates all interlock signals to enforce protection logic and ensure safe system operation. Inputs include magnet thermal switch chains, cooling system flow interlocks, power supply status signals, and external interlock inputs, all processed using fail-safe logic. Based on these inputs, the PLC performs functions such as detecting thermal faults and abnormal conditions, identifying open-circuit or wiring issues, aggregating multiple interlock signals, and issuing trip commands to the PSCs. This architecture enables fast fault detection and deterministic shutdown response, ensuring reliable protection of the ESR system.

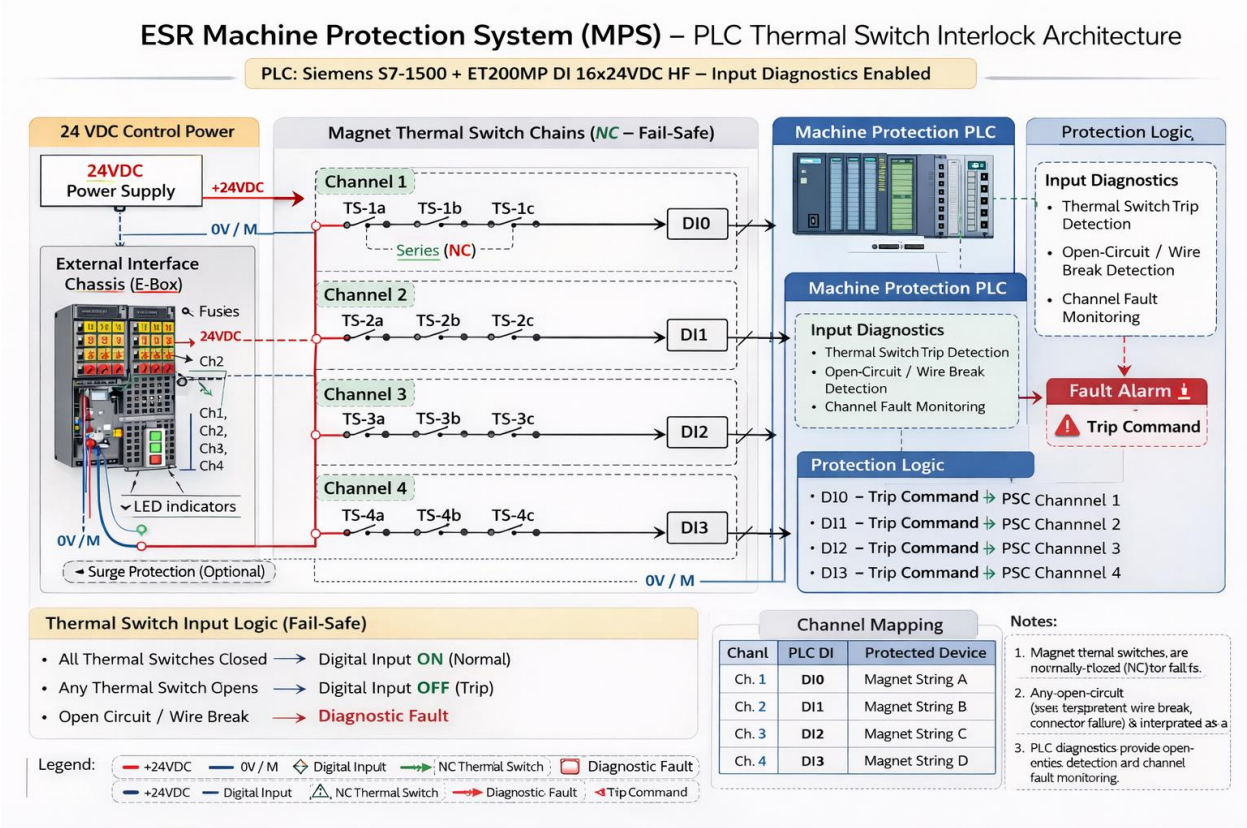


Figure 52. PLC-based interlock architecture showing thermal switch chains, diagnostics, and trip logic

4.8.4 Solid-State Relay (SSR) Interface for MPS Signals

To improve reliability and eliminate mechanical wear, solid-state relay (SSR)-based interfaces are used for signal transfer between the PLC and PSC. These interfaces provide galvanic isolation and signal conditioning between the low-voltage logic domain and industrial control signals.

The SSR-based interface uses digital isolation, solid-state switching, current limiting, and transient protection to provide reliable signal transfer between control and field domains. This design offers faster response, improved noise immunity, and longer lifetime compared to mechanical relays, while supporting fail-safe interlock signaling compatible with MPS requirements.

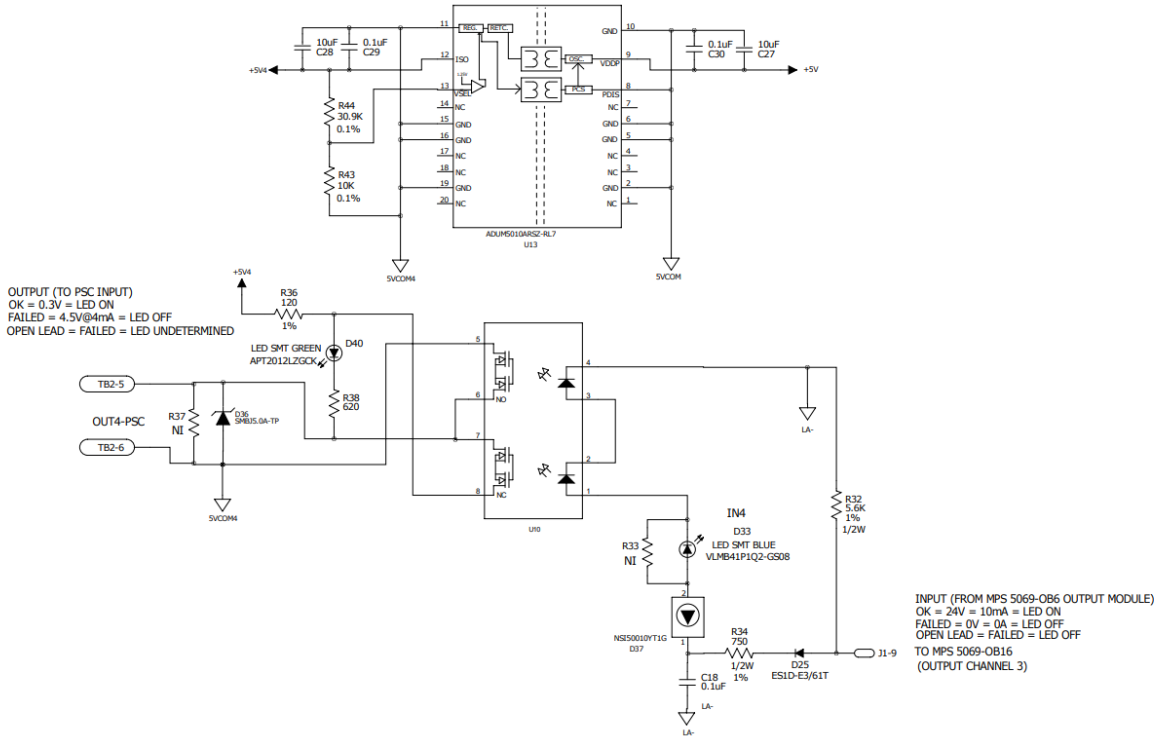


Figure 53. Solid-State Relay (SSR) Based Isolated Interface Between PLC and PSC

4.8.5 Magnet Thermal Switch Monitoring and Isolation

Each magnet is equipped with multiple snap-action thermal switches used for over-temperature protection. These switches are connected in series (fail-safe configuration) and monitored by the PLC.

The thermal interlock system is designed with a fail-safe Normally Closed (NC) configuration, enabling detection of both fault conditions and open-circuit or wiring issues. Signals originate at magnet-mounted snap-action thermal switches (typically one per coil or pole and additional switches on cooling inlets) and are routed through tunnel instrumentation cables to marshalling cabinets before reaching PLC inputs. Isolation between tunnel equipment and control systems is implemented at the interface level, ensuring safe and noise-immune signal transfer.

The signal path follows a structured flow from magnet to power supply shutdown (Magnet → Thermal Switch → Tunnel Cable → Marshalling → PLC → PSC → Shutdown), with isolation requirements varying by magnet type. Quadrupole and sextupole systems use 300 V isolation via epoxy or Kapton insulation combined with DIN rail isolators, while dipole systems require higher isolation (~2.5 kV), achieved using isolation transformers. This architecture ensures robust protection, proper signal integrity, and safe interfacing across all ESR magnet systems.

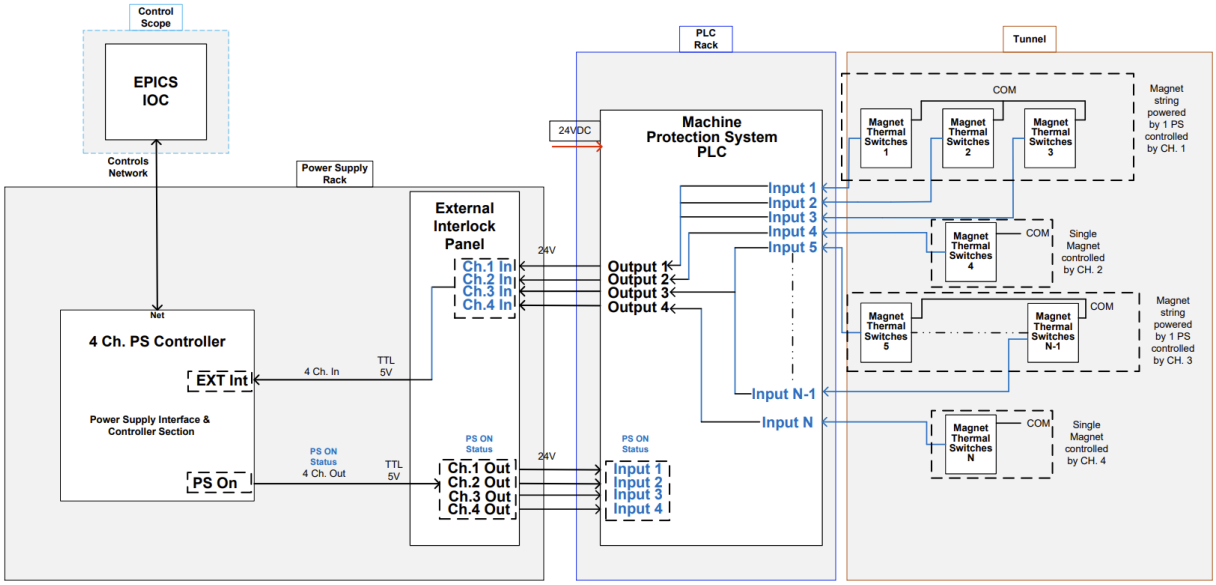


Figure 54. End-to-end interlock system showing signal flow from magnet thermal switches to PLC and PSC shutdown

4.8.6 BBA PLC Integration

The BBA system is integrated into the PLC architecture to enable remote control, monitoring, and safe operation. The BBA system provides controlled current bypass functionality for beam alignment without requiring dedicated power supplies.

The BBA control architecture is integrated into the PLC-based system, where the PLC provides relay drive control for BBA circuits, monitors status and faults via auxiliary contacts, and interfaces with the EPICS IOC for operator control. Communication is handled through Ethernet between the PLC and IOC, while direct digital I/O (24 V) links the PLC to BBA hardware, enabling coordinated operation between protection and beam alignment systems. A single PLC can manage multiple BBA units within a building, supporting remote operation, continuous status monitoring, and fault detection as part of the overall accelerator control system.

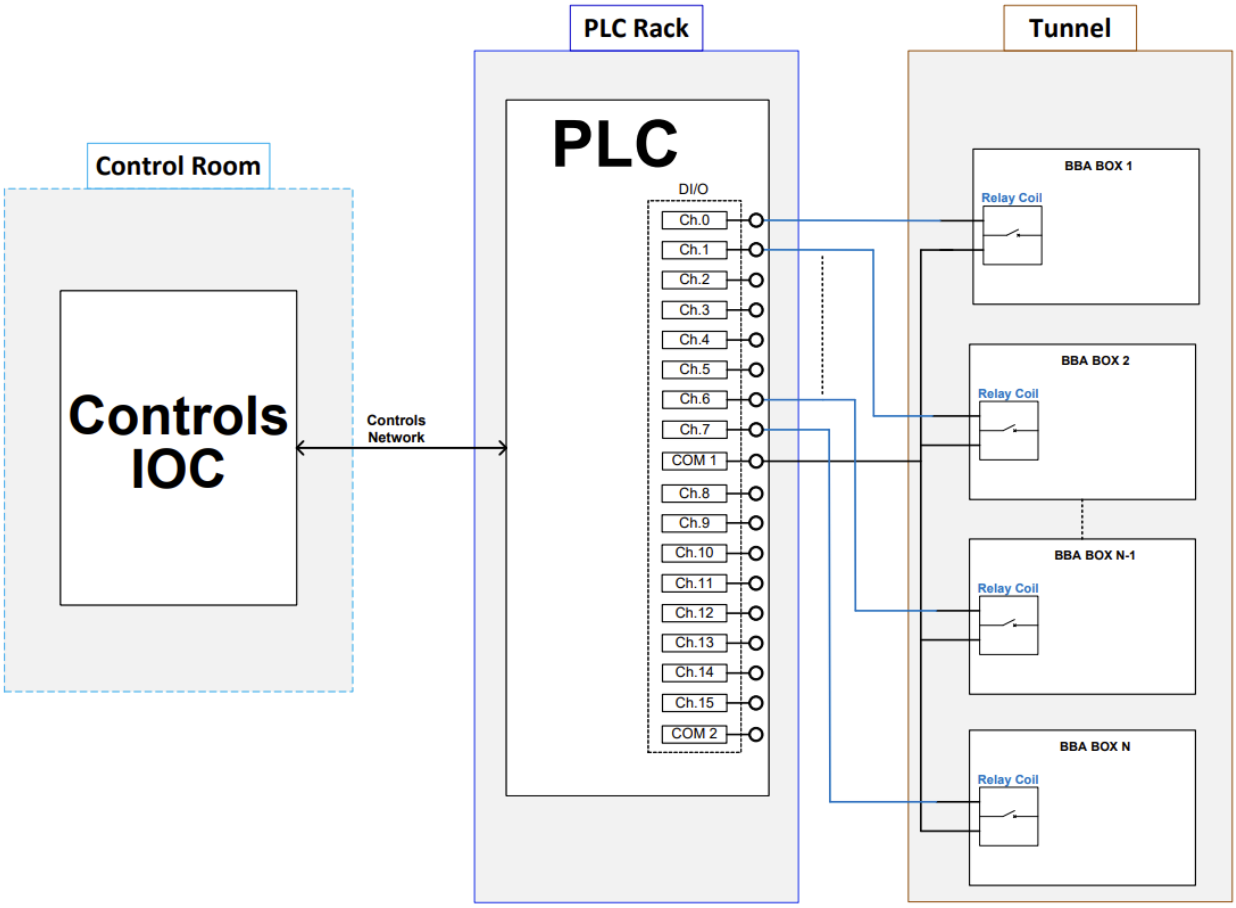


Figure 55. PLC integration for BBA showing relay control, IOC interface, and connection to multiple BBA units

4.9 Cables

The ESR cabling system uses standardized, high-reliability DC and instrumentation cables to connect power supplies, magnets, and control systems through structured cable tray routing, with careful attention to electromagnetic coupling, insulation, and installation practices. Separate shielded control cabling and magnet-specific isolation strategies, combined with consistent labeling and polarity conventions, ensure reliable operation, noise immunity, and safe integration of power, control, and protection systems across the ESR.

4.9.1 DC Cables

All DC cables will be run in continuous cable trays from the rack in the service building where the power supply resides to the magnet(s). All cable drops to individual components will have horizontal supports every 3ft and vertical supports every 4ft. DC cables will be various gauges between 14 AWG and 535 MCM, exact quantities of each can be found in the ESR architecture design spreadsheet. Cables will be NRTL listed, cable tray-exposed run rated, plenum fire rated and have a radiation compatible jacket. More information on acceptable cable types and materials can be found in the EIC Tray Cable Guide [EIC-SEG-STD-002]. Any cable size 1/0 AWG and

larger will be single conductor diesel locomotive cable (DLO) for its high strand count, high flexibility, and ease of pulling during installation. Cables smaller than 1/0 AWG will be two conductor multiconductor cable. All 500 MCM cable will be single conductor medium voltage type cable and is to be used only for the main dipole power supplies and magnets. Minimum voltage ratings for DLO is 2000V, multiconductor is 600V, and 500 MCM MV is 5kV.

Cables of opposite polarities on the same magnet string will be run in coupled pairs to keep electromagnetic fields to a minimum. Polarity is a bit of a misnomer here, in strings with multiple magnets it is not practical to denote each cable as being positive or negative. The only true positive and negative cables are those coming out of the positive and negative power supply output terminals. After the cables reach the first (or last) magnet in a string, one can only reference a positive or negative cable in relation to another magnet. So, when speaking about coupling cables of opposite polarities, every cable that has current flowing in the clockwise direction will be paired with a cable of the same string with current flowing in the counterclockwise direction, or vice versa.

The following statements do not apply to the main dipole magnets as they are a special case. The main dipole cable routing is dependent on the voltage balancing sequence covered in section 4.1.3. Magnets are powered in clockwise order, with the first magnet in a string to receive power always being the most counterclockwise, or leftmost. In all cases, the positive conductor coming out of the power supply will run uninterrupted to the A terminal of the counterclockwise most magnet. Similarly, the negative conductor coming out of the power supply will run uninterrupted to the B terminal of the clockwise most magnet. For every other magnet within the string, conductors will connect the B terminal of the previous magnet and to the A terminal of the next magnet, traversing clockwise. Cables will be placed in cable trays next to or as close as possible to each other and will travel the entire length of the string in this manner as a mated pair.

For single conductor cables this is easily achieved, as cables can be routed across magnets and service building entrances in one continuous cable run. As cables drop in and out of trays to connect to magnets, the pairing cable will stay in the tray as one complete cable for the length of string. There is no need for splices or magnet passthroughs to keep cable pairs together as they traverse the string.

For multiconductor cables in a string with multiple magnets, special attention must be paid to keep cable pairs coupled at all times. A string with magnets located only either clockwise or counterclockwise of the service building is simpler to handle. In this instance, the multiconductor cable jacket must be cut to expose the individual conductor needed to make the connection to the magnet. Multiconductor cables in cable trays must have sufficient electrical isolation, which the outer cable jacket inherently provides. Therefore, it is preferable to keep all cable jackets cuts located outside of the cable tray. Magnets will be built with integrated pass-through terminals specifically for the conductor that is not actively powering the magnet to continue uninterrupted. This pass-through terminal will have no electrical connection to the rest of the magnet and is only used for keeping cable pairs together. In practice this will look like the first conductor in a cable connecting to the B terminal and the second conductor connecting to the passthrough terminal on the previous magnet, and the same first conductor connecting to the A terminal with the second

conductor connecting to the passthrough terminal on the next magnet. The figure below illustrates this. All statements made follow the exact same conventions of the previous paragraphs, with the added nuance of the pass-through terminals to preserve cable jacket integrity in the trays.

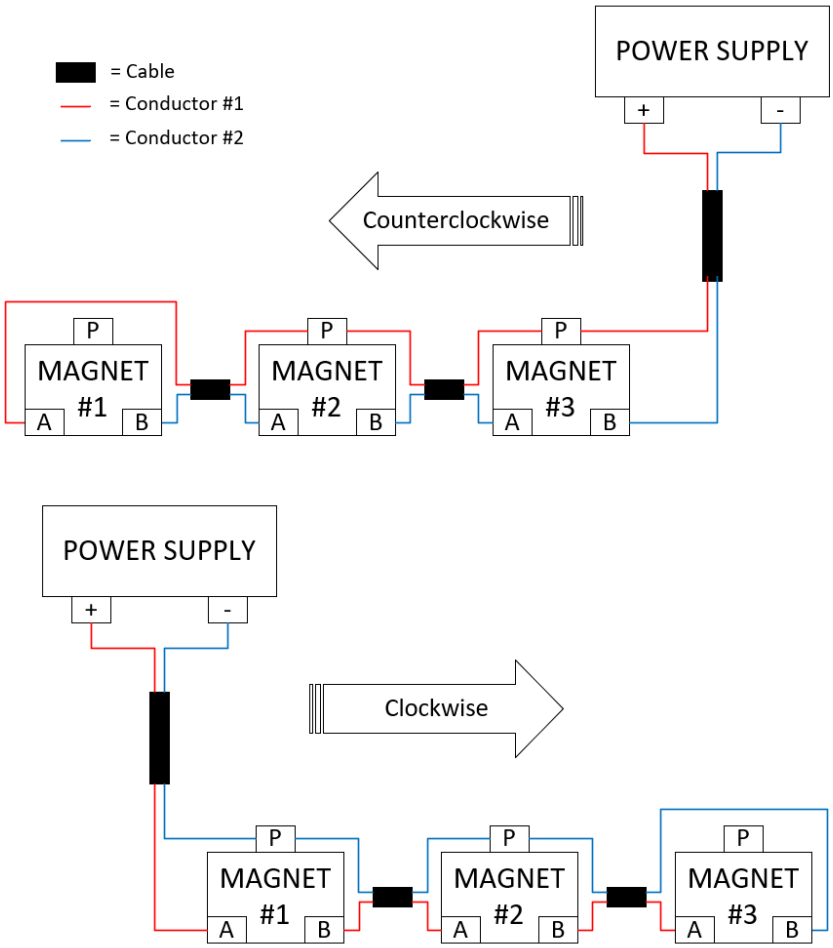


Figure 56. Cable Routing with Power Supply Outside of Magnet String Span

Having multiconductor cables on a string with magnets located both clockwise and counterclockwise of the service building add another layer of nuance. The cable coming from the power supply must diverge so the positive goes to the counterclockwise most magnet, and the negative goes to the clockwise most magnet. While it is not preferable to have cut jackets in cable trays, it is required in this case. Cables will be spliced in the tray such that there is a cable coming from the power supply, a second cable going counterclockwise, and a third cable going clockwise. See the figure below for a visual representation. Splice connectors with heat shrink tubing and two-breakout heat shrink boots will be used to achieve sufficient electrical continuity and isolation in the tray. Other than the splices, this case follows all the conventions of the previous paragraphs.

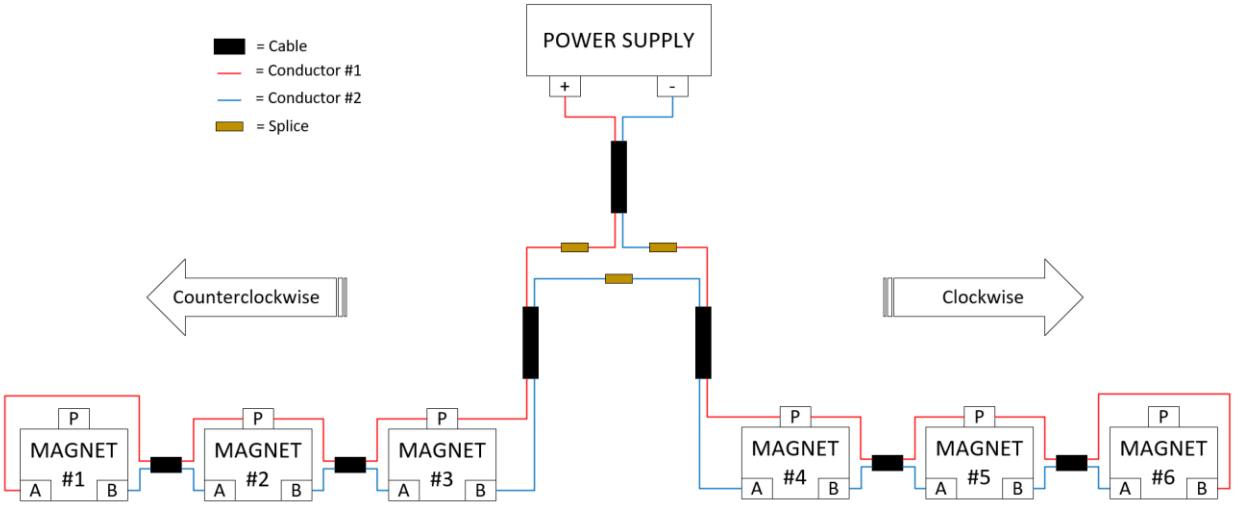


Figure 57. Cable Routing with Power Supply Inside of Magnet String Span

Cable pull and termination lists can be found in the supporting documents folder. These lists contain all the DC cables from the power supplies to the magnet strings. Each cable will have a temporary label applied at the time of pulling with the cable ID, and the final label with all cable information will be applied at the time of termination.

4.9.2 BBA Cables

Control wiring between the PLC and the BBA contactor coil is implemented using a dedicated two-conductor 16 AWG cable, providing a 24 VDC supply and return path for the coil. The conductor size is selected based on limiting voltage drop while maintaining sufficient margin relative to the contactor coil pickup requirement. For the maximum expected cable length of 2000 ft one-way (4000 ft round trip), and a coil current of approximately 0.25 A, the total loop resistance is estimated to use a conductor resistance of approximately 4.0 Ω per 1000 ft. This results in a loop resistance of

$$R = 4.0 \times \frac{4000}{1000} = 16.0\ \Omega,$$

and a corresponding voltage drop of

$$V = I \times R = 0.25 \times 16.0 = 4.0\ V.$$

With a 24 V supply from PLC module, this yields approximately 20 V at the contactor coil under worst-case conditions. The specified coil pickup voltage is 19.2 V at 20 °C, indicating that the available voltage remains above the required threshold even at maximum cable length. This confirms that the selected 16 AWG conductors provide adequate electrical margin for reliable operation. In practice, additional margin is expected for shorter cable runs and due to conservative assumptions used in the calculation.

The return conductor is referenced to the PLC common, ensuring a complete and stable control circuit. The use of a single standardized conductor size simplifies installation, reduces wiring variability, and ensures consistent performance across all BBA locations without the need for parallel conductors or mixed wire sizes.

In addition to the primary control circuit, a second two-conductor 16 AWG cable is installed to support optional auxiliary contact wiring for status monitoring. While auxiliary readback is not required for normal system operation, this provision allows implementation of contactor state verification or interlock logic if needed, without requiring additional cabling or modification to the installed system.

4.9.3 Machine Protection System (MPS) Cables

The MPS cabling infrastructure provides the physical link between tunnel-installed equipment, rack-level interface hardware, and the PLC-based protection system, ensuring reliable signal transmission, electrical isolation, and noise immunity across the ESR. The network connects magnet thermal switches, cooling system interlocks, marshaling cabinets, EIP, PSC signals, and PLC I/O modules using shielded instrumentation cables rated for 600 V. These cables, typically 16-22 AWG with foil shielding and drain wires, support 24 VDC control signals while providing sufficient insulation margin and mechanical robustness for both tunnel and rack environments. Signal routing follows a structured path from magnet to tunnel cable trays, through marshalling cabinets and isolation interfaces, to PLC inputs and onward to PSCs, while maintaining strict separation between power and control cabling to minimize electromagnetic interference.

Electrical isolation is achieved through a combination of shielding practices, interface-level isolation, and magnet-specific strategies. Quadrupole and sextupole systems use 300 V isolation via epoxy or Kapton insulation with DIN rail isolators, while dipole systems require significantly higher isolation (~2.5 kV), implemented using isolation transformers. Signals are primarily discrete, fail-safe digital interlocks (e.g., normally closed thermal switches and flow switches), with 24 V PLC-level signals converted to TTL levels at the PSC via the EIP, which also provides optical isolation and signal routing. This layered approach ensures reliable operation, fast fault detection, and safe integration between tunnel systems and control infrastructure.

Table 23. MPS System Cable Summary

Parameter	Specification	Notes
Cable Type	Shielded instrumentation cable	Twisted pair recommended
Conductor Size	16–22 AWG	Typical for control and interlock signals
Insulation Rating	600 V minimum	Standard for cable tray use
Shielding	Foil shield with drain wire (preferred)	EMI protection
Number of Conductors	2–8 conductors (typical)	Based on channel grouping
Signal Type	24 VDC digital signals	Interlocks and status signals
Temperature Rating	75–90°C	Suitable for tunnel/rack environments
Jacket Type	See EIC-SEG-STD-002	LSZH for enclosed areas if required
Grounding	Single-point shield grounding	Avoid ground loops
Routing	Separate from power cables	Noise immunity

4.9.4 Magnet Polarity

EIC-ROD-053 is the record of decision regarding magnet conventions for all EIC magnetic elements. The document is summarized in the following paragraphs. It defines standardized naming and magnetic polarity conventions for all magnets used in EIC facilities, ensuring consistency in their design, construction, installation, and operation. A key challenge addressed is the presence of both positively and negatively charged beams in the same system. While their behavior in magnetic fields differs, requiring the right-hand rule for positive beams and the left-hand rule for electron beams, the conventions ensure magnets are built and installed uniformly regardless of beam type.

It explains how magnets are classified and oriented, distinguishing between normal and skew configurations based on pole positions when viewed from the lead end. Proper identification and documentation of this lead end and the final installed orientation are essential, as magnet orientation directly affects how forces are applied to the beam. In some cases, rotating a magnet can reverse its effect, making accurate records of direction and polarity critical.

The ROD standardizes electrical connections by requiring all magnets to have permanently marked “A” and “B” terminals, along with clearly identifiable coil wiring. Power supply terminals are defined consistently, and the relationship between current direction and magnetic field is shown in the figures in the ROD. These same conventions apply to trim (secondary) coils, which must also be clearly labeled and documented. Solenoids follow the same concept, with positive current on the “A” terminal producing a magnetic field going into the plane when viewed from the lead end.

5 Conclusion

The ESR Power Supply System design presented in this report demonstrates a high level of technical maturity, completeness, and readiness for implementation. The system requirements, derived directly from physics specifications and formalized through EIC Records of Decision, are clearly defined, traceable, and consistently applied across all subsystems. Ripple, stability, and operational performance requirements have been rigorously translated into engineering specifications using validated analytical methods, including power spectral density conversions and system-level modeling. These requirements have been systematically incorporated into the design of custom, COTS, and BTP power supply solutions, ensuring that all magnet families are supported with appropriate and optimized architectures.

The overall system architecture reflects a well-integrated and highly coordinated design approach, combining standardized rack configurations, modular supporting equipment, and scalable control and protection systems. The use of PSC-based closed-loop current regulation, MCPCIC coordination for multi-supply configurations, and PLC-based machine protection ensures deterministic, low-latency operation and robust system protection. Critical design considerations have been thoroughly analyzed using simulation tools and validated through experimental testing. The selection of standardized interfaces, reusable hardware platforms, and proven designs from NSLS-II and ALS-U further strengthens system reliability while reducing technical risk.

Extensive validation and testing efforts confirm that the proposed designs meet or exceed ESR performance requirements. Vendor testing and in-house verification have demonstrated that COTS power supplies satisfy ripple and stability specifications under realistic operating conditions. BTP power converter designs, including both corrector and trim dipole solutions, have been modeled, prototyped, and tested to validate electrical performance, transient response, and protection mechanisms. The implementation of a structured ACL process ensures that all components will undergo rigorous verification from vendor qualification through full system integration. Additionally, supporting systems such as rack thermal management, PDUs, interlocks, and cabling infrastructure have been designed with detailed engineering analysis and aligned with facility constraints, safety standards, and operational requirements.

The ESR power supply system design also demonstrates strong integration with controls, infrastructure, and machine protection systems. The adoption of standardized communication frameworks, combined with modular PLC-based protection and BBA integration, ensures seamless operation within the broader EIC environment. The cabling, grounding, and isolation strategies provide reliable signal integrity and safety across all operating conditions. Furthermore, the design incorporates maintainability, scalability, and future upgrade capability.

Based on the comprehensive definition of requirements, the maturity of the design, and the successful validation of key subsystems, the ESR Power Supply System is considered technically complete and ready to advance to the procurement phase. The combination of proven design methodologies, validated performance, and structured quality assurance processes provides high confidence that the system can be manufactured, integrated, and operated to meet the demanding requirements of the Electron-Ion Collider.

Appendix A – Supporting Documents

A.1 Record of Decision

1. EIC-ROD-036 (ESR Main Magnet Dipole Power Supply and Trim Changes)
2. EIC-ROD-040 (Water Requirements for ESR Power Supplies)
3. EIC-ROD-042 (Design of ESR Sextupole Link Boxes and Power Supply Configurations)
4. EIC-ROD-043 (Procedure to Select DC Cables for ESR DC Power Supplies)
5. EIC-ROD-044 (ESR Power Supply Stability Requirements)
6. EIC-ROD-053 (Magnet Conventions for EIC Magnetics)
7. EIC-ROD-055 (ESR PS PDR Regarding Addition of Water Flow Switches as Interlocks)
8. EIC-ROD-058 (Cable Length and Building Selection Process)

A.2 Tech Notes

1. The ESR BNL-226328-2024-TECH (Maximum Allowable Voltage Ripple ESR Main Dipole PS)
2. ESR Main Dipole Voltage Balancing Tech Note.docx

A.3 Technical Specifications and Statements of Work

1. ESR Main Dipole TechSpec Rev5.docx
2. SOW ESR Main Dipole.docx
3. ESR Unipolar COTS PS Tech Spec.docx
4. SOW_COTS_PS.docx
5. EIC_PSG_SOW_RACKS-003.docx
6. EIC_PSG_SPC_RACKS-005.docx
7. SOW_BTP_BBA.docx
8. SOW_BTP_BPC.docx
9. SOW_BTP_DCCT_Assembly.docx
10. SOW_BTP_MCPCIC.docx
11. SOW_BTP_ALL_PDU.docx
12. SOW_BTP_PSC.docx

A.4 Design Documents

1. BBA
    a. BBA Calibration Procedure.docx
    b. Resistor_selection.xlsx
    c. Rev KP BBA Cables.xlsx
2. Corrector BPC
    a. EIC ESR Corrector Power Supply Design Report.pdf
    b. EIC ESR Corrector Power Supply Design_v6.pptx
3. Dipole Trim BPC
    a. Determining Induced Voltage in ESR Dipole Trim Coil.docx
    b. COTN.pdf (Transversely driven coherent beam oscillations and specifications for high-frequency ESR dipole power supply current ripple)

   c. DipolePSRippleTN 052323.pdf (ESR Dipole Power Supply Current Ripple and Noise Specifications)
   d. PS-design-calcs.xlsx
   e. EIC ESR Trim Dipole Power Supply Design_v5.pptx
4. PDU
   a. ESR PDU Design Report.pdf
5. ESR Sextupole Link Box design.docx
6. EIC ESR Main Dipole Circuit Analysis.pptx
7. Cables
   a. DC Cable Master List.xlsx
   b. EIC-SEG-STD-002 (EIC Tray Cable Guide Design Standard)
8. Accelerator Physics to Components Data Flow.pdf
9. Metrology Analysis.pptx
10. ESR PS Architecture Design v2.3.xlsm

A.5 Test Documents

1. Test Procedure – BPC-2CH-S-40V-10A.docx
2. Test Procedure – ESR Dipole Trim BTP.docx
3. COTS_Power_Supply_Test_Procedure.pdf
4. MCPCIC_Integration_Test_Procedure.pdf
5. PDU Universal Acceptance Test Procedure.docx
6. PDU Universal Power Up Procedure.docx
7. 4Ch PSC Check Sheet ver6.docx
8. BTP Power Supply Testing Steps ACL to 100% Testing.pptx
9. ESR Main Dipole Field Testing Doc.docx
10. PSC_ATE_UsersGuide_dib_Rev1.21.pdf
11. Rack System Testing.docx

A.6 Requirement Documents

1. EIC-SEG-RSI-110 (ESR Magnet String Design Configuration)
2. EIC-SEG-RSI-148 (ESR Magnet Power Supply Performance Requirement Document)

Glossary of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
AGS	Alternating Gradient Synchrotron
ALS-U	Advanced Light Source Upgrade
ARM	Advanced RISC Machine (processor architecture)
BBA	Beam-Based Alignment
BNL	Brookhaven National Laboratory
BPC	Bipolar Power Converter
BTP	Build-To-Print
CFM	Cubic Feet per Minute
COTS	Commercial Off-The-Shelf
DAC	Digital-to-Analog Converter
DC	Direct Current
DCCT	Direct Current Current Transformer
DI	Deionized (water)
DLO	Diesel Locomotive Cable
EMI	Electromagnetic Interference
EPICS	Experimental Physics and Industrial Control System
EIP	External Interface Panel (or Chassis)
EIC	Electron-Ion Collider
EIN	Electron Injection System
ESR	Electron Storage Ring
EVR	Event Receiver
FPGA	Field Programmable Gate Array
FFT	Fast Fourier Transform
FWHM	Full Width at Half Maximum
GPM	Gallons Per Minute
HMI	Human Machine Interface
HSR	Hadron Storage Ring
HVAC	Heating, Ventilation, and Air Conditioning
HX	Heat Exchanger
IOC	Input/Output Controller
IR 6	Interaction Region 6
I²C	Inter-Integrated Circuit (communication protocol)

kVA	Kilovolt-Ampere
LLRF	Low-Level Radio Frequency
LOTO	Lockout-Tagout
LSII	Light Source II
LVPS	Low Voltage Power Supply
MCM	Thousand Circular Mils
MCPCIC	Multi-Channel Power Converter Interface Card
MPS	Machine Protection System
NEC	National Electrical Code
NRTL	Nationally Recognized Testing Laboratory
NSLS-II	National Synchrotron Light Source II
PCB	Printed Circuit Board
PDU	Power Distribution Unit
PID	Proportional-Integral-Derivative
PLC	Programmable Logic Controller
PM	Phase Margin
PSC	Power Supply Controller
PSD	Power Spectral Density
PWM	Pulse Width Modulation
QA	Quality Assurance
QC	Quality Control
RCS	Rapid Cycling Synchrotron
RHIC	Relativistic Heavy Ion Collider
RMS	Root Mean Square
ROD	Record of Decision
RS-485	Recommended Standard 485 (serial communication)
RTD	Resistance Temperature Detector
SCCR	Short Circuit Current Rating
SEG	Systems Engineering Group
SFP	Small Form-factor Pluggable
SPI	Serial Peripheral Interface
SSR	Solid State Relay
TVS	Transient Voltage Suppression
UL	Underwriters Laboratories
UPS	Uninterruptible Power Supply

References

"ALS-U Bipolar Power Converters for Storage Ring", David Bergman et. al., BNL 2022

"High Precision Current Measurement in Power Converters", Miguel Cerqueira Bastos, CAS 2014